ECE4740: Digital VLSI Design

Lecture 22: Tree adders

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Recap

Carry-skip and carry-select adders

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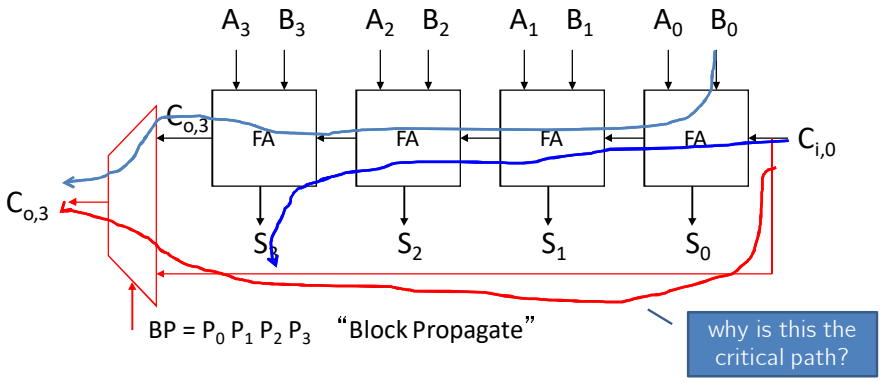
Carry-skip adder principle



- If $BP=P_0P_1P_2P_3=1$ then $C_{O,3}=C_{i,0}$, otherwise block itself generates (or kills) carry internally

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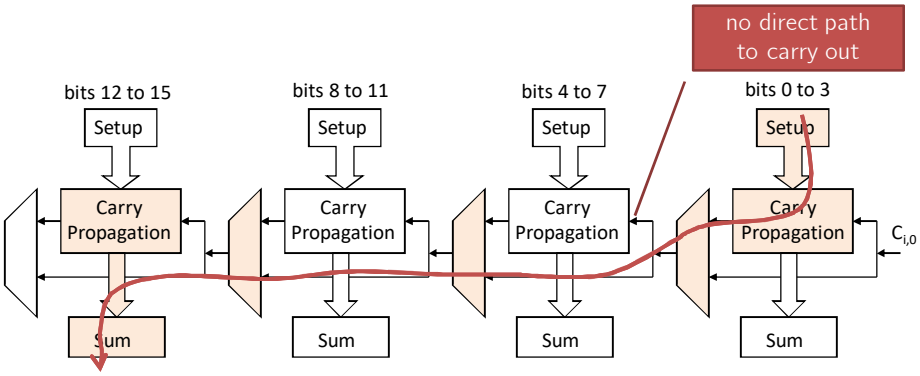
N-bit carry skip adder



- Set block size to B=sqrt(N/2)
- Delay grows only with sqrt(N)

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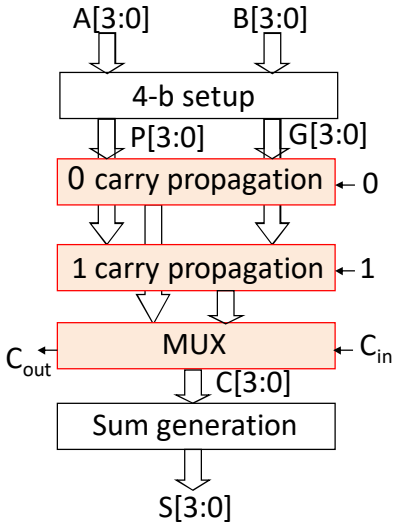
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Carry select adder (CSA)

- Pre-compute carry out for each block for C_{in}=0 and C_{in}=1
- Select correct outputs as soon as C_{in} is ready
- Only a MUX in the critical path!



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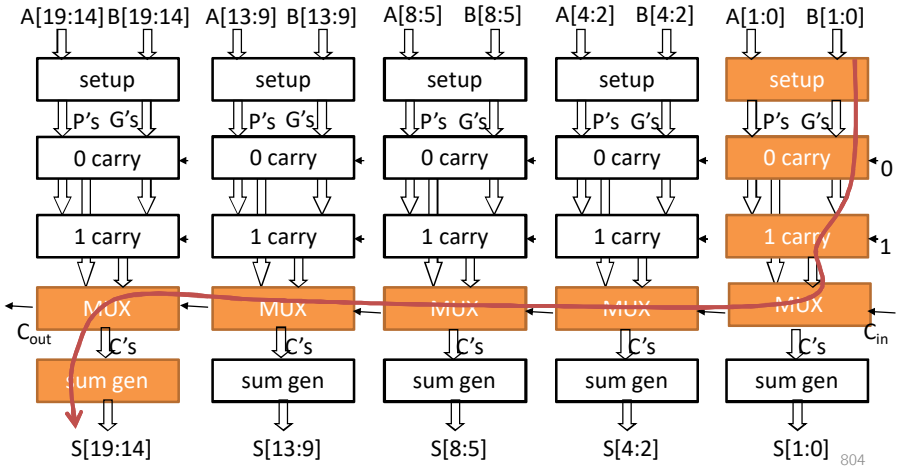
Square root carry select adder

- Linearly increasing group sizes: T grows in sqrt(N)



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Recap and more topologies

Tree adders

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The carry recurrence

- Remember: $C_{i+1}=G_i+P_iC_i$

  $C_1 = G_0 + P_0\ C_0$

- $C_2 = (G_1 + P_1G_0) + (P_1P_0)C_0$

  new group generate and group propagate signals

- Can be modeled as an operation on a tuple:
  $(G_i,P_i)\bullet(G_{i-1},P_{i-1})=(G_i+P_i*G_{i-1},P_i*P_{i-1})$

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PG diagram notation

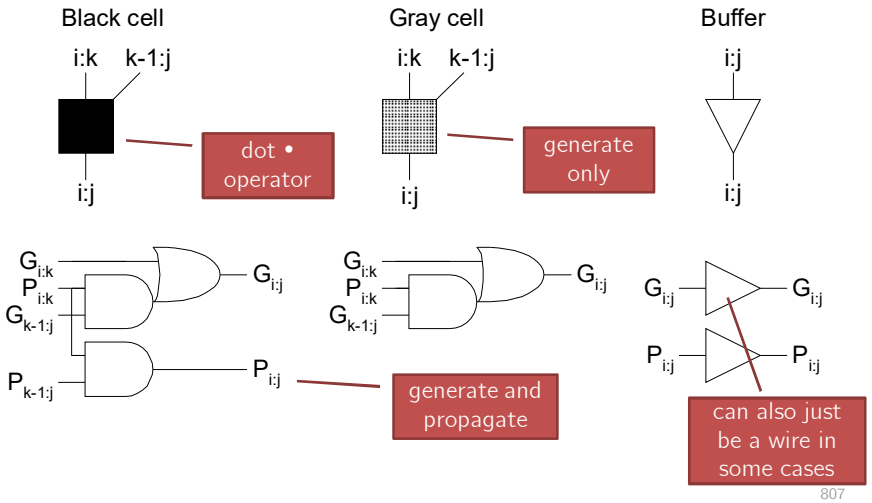

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Image Adapted From: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Brent-Kung adder (1982)

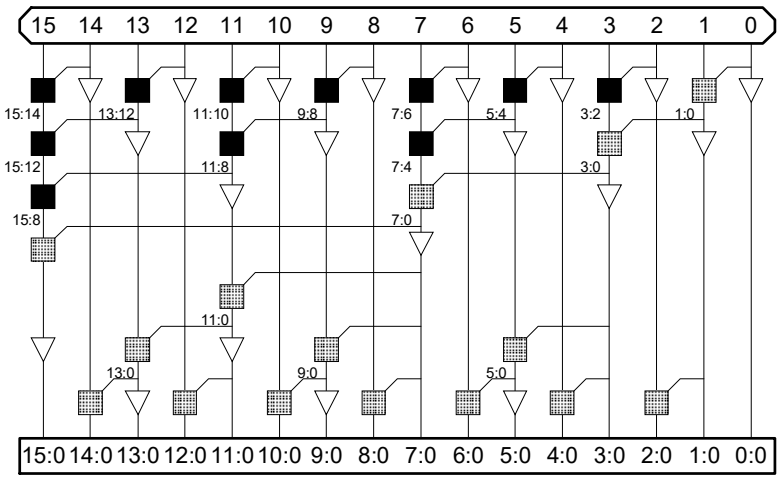

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Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Brent-Kung adder (cont'd)

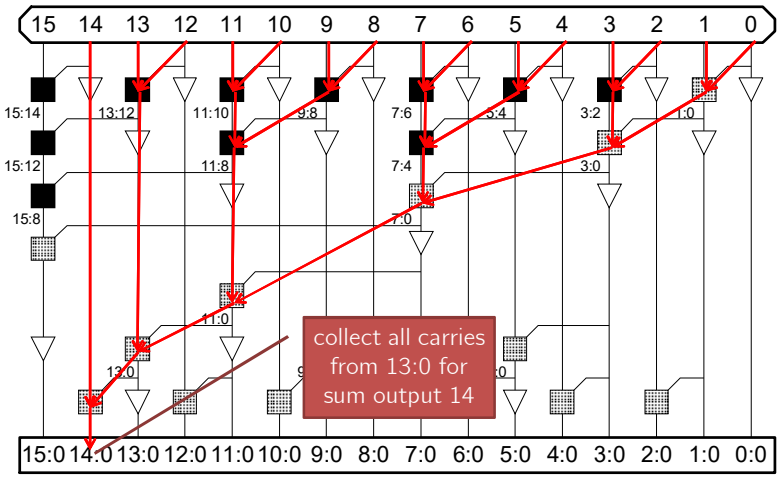

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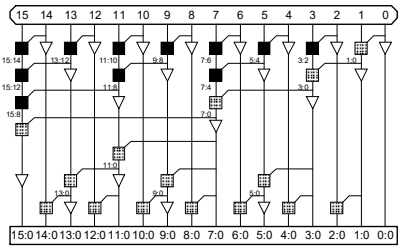
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Summary: Brent-Kung adder

- $A_. = 2N - \log(N) - 2$
- $T_. = 2\log(N) - 2$
- $FO_{max} = \log(N)$



- Pros:
  - regular structure (...really?)
  - limited fan-in for all gates
- Cons:
  - FO is an issue: grows log(N)
  - Power?

uneven path lengths → glitches

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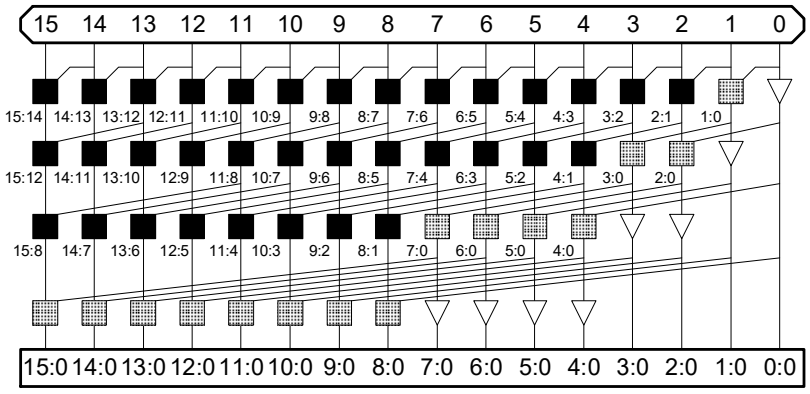
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Kogge-Stone adder (1973)



- $A_. = N\log N - N + 1$
- $T_. = \log(N)$
- $FO_{max} = 2$
- High wiring overhead

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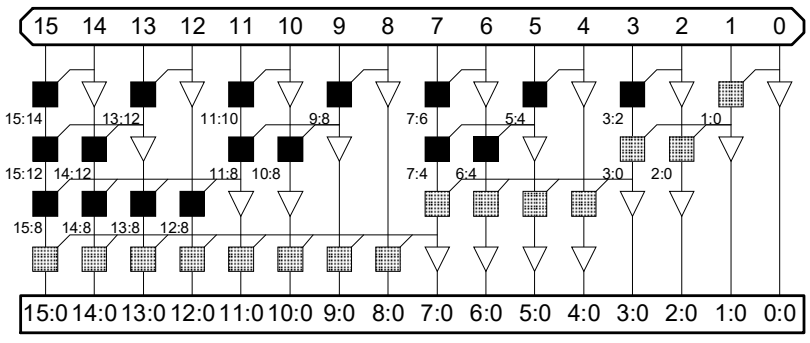
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Sklansky adder (1960)



- $A_. = 0.5N\log(N)$
- $T_. = \log(N)$
- $FO_{max} = N/2$

Jack Sklansky, UC Irvine

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Images taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris; https://www.the-scientist.com/?articles.view/articleNo/18705/title/New-Technology-Weighs-In-On-Mammography-Debate/

Which tree adder should I pick?

Name	Area [A.]	Time [T.]	Max. FO	Wiring
Ripple carry	N-1	N-1	2	☺☺
Sklansky	N/2*log(N)	log(N)	N/2	😐
Brent-Kung	2N-log(N)-2	2*log(N)-2	log(N)	☺
Kogge-Stone	N*log(N)-N+1	log(N)	2	☹☹
Carry increment	2N-sqrt(2N)	sqrt(2N)	sqrt(2N)	☺

- Trade-off between area, propagation delay, etc.
- For adders with a small number of bits, do not forget carry select and carry skip adders!

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What are CAD tools doing?

Adder design with Synopsys DC

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Synopsys design compiler (DC)

- One of the leading CAD tools for digital integrated circuits and FPGAs
- How do you use it?
  - You write hardware description language
  - You provide constraints and then compile it
  - The tool generates a gate-level netlist
- Automatic logic optimization, sizing, etc.

SYNOPSYS®

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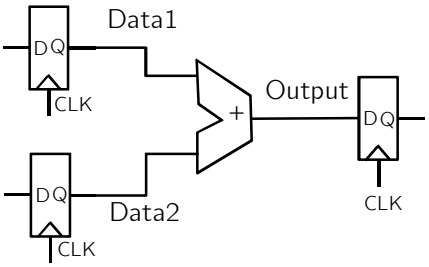
Simple example

- Faraday 90nm CMOS technology
- 16-bit adder design
  - 16 bit inputs (Data1 and Data2)
  - 17 bit outputs (Output)



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Synthesis script example

```
[...]

analyze -library WORK -format vhdl {chris_adder.vhd}

elaborate chris_adder -architecture arch1 -library WORK

create_clock -name "ClkxCI" -period 5 -waveform {0 2.5} {ClkxCI}

compile_ultra
```

set the clock period to 5ns = constraint

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Area results for T=5ns

WHY?

- 49 sequential cells (D-flip-flops)
- 18 combinational cells

- Combinational area = 463um^2
- Noncombinational area = 882um2

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```
****************************************
Report : area
Design : chris_adder
Version: [redacted]
Date   : Thu Apr  9 03:59:42 2015
****************************************

Library(s) Used:

[redacted]

Number of ports:                           51
Number of nets:                           116
Number of cells:                           67
Number of combinational cells:             18
Number of sequential cells:                49
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       4

Combinational area:               463.000000
Buf/Inv area:                       0.000000
Noncombinational area:            882.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 1345.000000
Total area:                 undefined

Hierarchical area distribution
------------------------------

                                  Global cell area          Local cell area
                                  ------------------  ----------------------------
Hierarchical cell                 Absolute   Percent  Combi-    Noncombi-  Black-
                                  Total      Total    national  national   boxes   Design
--------------------------------  ---------  -------  --------  ---------  ------  ---------
chris_adder                       1345.0000    100.0  463.0000   882.0000  0.0000  chris_adder
--------------------------------  ---------  -------  --------  ---------  ------  ---------
Total                                                 463.0000   882.0000  0.0000
```

how Synopsys reports the circuit area

usually comes without units → depends on library

Timing results for 5ns

- Critical path: t_{pdmax}=4.76ns
  - Startpoint: LSB of Data1
  - Endpoint: carry output (bit 16)
- Most likely a simple ripple carry adder
- Carry out (= bit 16) is critical!

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Part 1

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : chris_adder
Version: [redacted]
Date   : Thu Apr  9 03:59:42 2015
****************************************

Operating Conditions: TCCOM   Library: [redacted]
Wire Load Model Mode: enclosed

  Startpoint: Data1regxDR_reg[0]
              (rising edge-triggered flip-flop clocked by ClkxCI)
  Endpoint: OutputregxDR_reg[16]
            (rising edge-triggered flip-flop clocked by ClkxCI)
  Path Group: ClkxCI
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  chris_adder        enG5K                 [redacted]
```

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Part 2

AN2RLX1 = 2-input AND gate w/ drive strength 1

Point	Incr	Path
clock ClkxCI (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
Data1regxDR_reg[0]/CK (QDFFRBRLX1)	0.00	0.00 r
Data1regxDR_reg[0]/Q (QDFFRBRLX1)	0.33	0.33 f
U5/O (AN2RLX1)	0.16	0.49 f
intadd_0/U16/CO (FA1RLX1)	0.22	0.71 f
intadd_0/U15/CO (FA1RLX1)	0.23	0.93 f
intadd_0/U14/CO (FA1RLX1)	0.23	1.16 f
intadd_0/U13/CO (FA1RLX1)	0.23	1.38 f
intadd_0/U12/CO (FA1RLX1)	0.23	1.61 f
intadd_0/U11/CO (FA1RLX1)	0.23	1.84 f
intadd_0/U10/CO (FA1RLX1)	0.23	2.06 f
intadd_0/U9/CO (FA1RLX1)	0.23	2.29 f
intadd_0/U8/CO (FA1RLX1)	0.23	2.51 f
intadd_0/U7/CO (FA1RLX1)	0.23	2.74 f
intadd_0/U6/CO (FA1RLX1)	0.23	2.97 f
intadd_0/U5/CO (FA1RLX1)	0.23	3.19 f
intadd_0/U4/CO (FA1RLX1)	0.23	3.42 f
intadd_0/U3/CO (FA1RLX1)	0.23	3.64 f
intadd_0/U2/CO (FA1RLX1)	0.20	3.84 f
OutputregxDR_reg[16]/D (QDFFRBRLX1)	0.00	3.84 f
data arrival time		3.84
clock ClkxCI (rise edge)	5.00	5.00
clock network delay (ideal)	0.00	5.00
OutputregxDR_reg[16]/CK (QDFFRBRLX1)	0.00	5.00 r
library setup time	-0.24	4.76
data required time		4.76
data required time		4.76
data arrival time		-3.84
slack (MET)		0.92

4.76ns – 3.84ns = 0.92 ns

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The reason (VHDL ftw!)

```
architecture arch1 of chris_adder is

signal Data1regxDR: std_logic_vector(number_of_bits-1 downto 0);
signal Data2regxDR: std_logic_vector(number_of_bits-1 downto 0);
signal OutputregxDR: std_logic_vector(number_of_bits downto 0);

begin

process(ClkxCI, RstxCI)
begin

if RstxCI = '0' then
        Data1regxDR <= (others => '0');
        Data2regxDR <= (others => '0');
        OutputregxDR <= (others => '0');
elsif ClkxCI'event and ClkxCI = '1' then
        Data1regxDR <= Data1xDI;
        Data2regxDR <= Data2xDI;
        OutputregxDR <= std_logic_vector(unsigned('0' & Data1regxDR) + unsigned('0' & Data2regxDR));
end if;
end process;

OutputxDO <= OutputregxDR;

end arch1;
```

asynchronous reset

do not write data-path stuff in combinational blocks → bad practice

Can you see it now?

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What happens if we set T=1ns?

- Very aggressive delay constraint!
- Combinational area = 1323um^2
- Noncombinational area = 987um^2
- (Remember 463um^2, 882um^2 of ripple carry adder)

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Part 1

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : chris_adder
Version: [redacted]
Date   : Thu Apr  9 04:02:00 2015
****************************************

Operating Conditions: TCCOM   Library: [redacted]
Wire Load Model Mode: enclosed

  Startpoint: Data2regxDR_reg[5]
              (rising edge-triggered flip-flop clocked by ClkxCI)
  Endpoint: OutputregxDR_reg[13]
            (rising edge-triggered flip-flop clocked by ClkxCI)
  Path Group: ClkxCI
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  chris_adder        enG5K                 fsd0k_a_generic_core_1d0vtc
```

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Part 2

Point	Incr	Path
clock ClkxCI (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
Data2regxDR_reg[5]/CK (QDFFRBRLX3)	0.00	0.00 r
Data2regxDR_reg[5]/Q (QDFFRBRLX3)	0.28	0.28 f
U76/O (NR2RLX3)	0.09	0.37 r
U75/O (AOI12RLX2)	0.06	0.43 f
U96/O (AOI12RLX2)	0.18	0.61 r
U84/O (ND2RLX6)	0.13	0.74 f
U69/O (ND3RLX2)	0.07	0.82 r
U113/O (ND3RLX2)	0.07	0.89 f
U127/O (XOR2RLX1)	0.11	1.00 f
OutputregxDR_reg[13]/D (QDFFRBRLX1)	0.00	1.00 f
data arrival time		1.00
clock ClkxCI (rise edge)	1.00	1.00
clock network delay (ideal)	0.00	1.00
OutputregxDR_reg[13]/CK (QDFFRBRLX1)	0.00	1.00 r
library setup time	-0.24	0.76
data required time		0.76
data required time		0.76
data arrival time		-1.00
slack (VIOLATED)		-0.24

1.00ns – 0.76ns = -0.24 ns

☹

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Fastest design

- t_{pd} = 1.24ns (including flip-flop timing)
- t_{pd} = 720ps (without flip-flop timing)

- Old lab 4 constraints:
  - 500ps critical path
  - Area smaller than 800um^2 → 5pts

- Hand-design can be faster & smaller than tool-based design (but it's much more work)!

Note that we are comparing different processes here and in lab 4;
flip-flop timing: propagation delay = 280ps=propagation, setup time = 240ps

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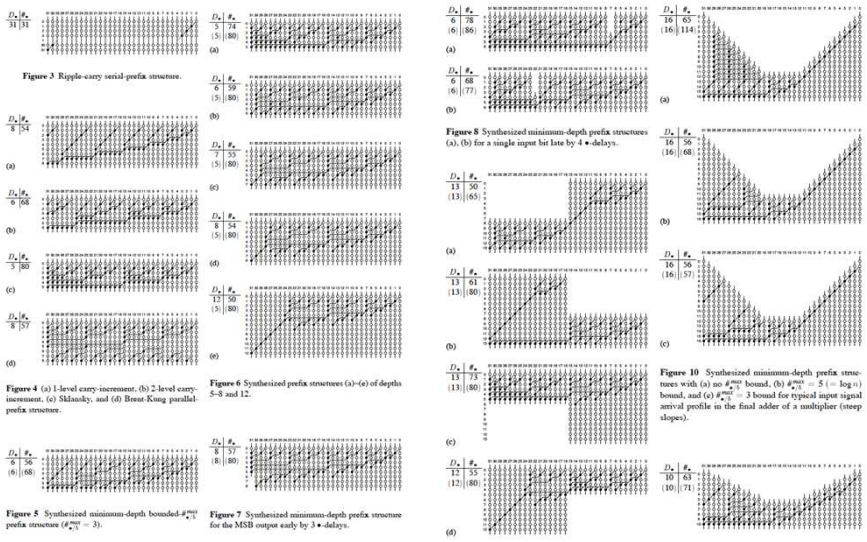
CAD tools are smart!



R. Zimmermann, "Non-Heuristic Optimization and Synthesis of Parallel-Prefix Adders," IWLAS 1996

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