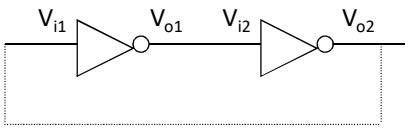
ECE4740: Digital VLSI Design

Lecture 18: Latches and flipflops

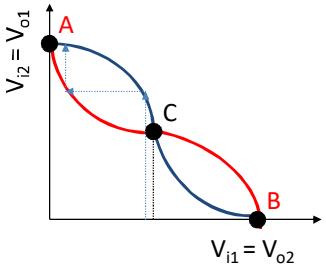
Simple static storage cells

Latches

Recap: regenerative property



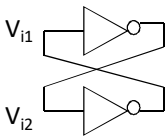
even number of cascaded inverters



- If the |gain| in the transient region is larger than 1, only A and B are stable operation points
- (C is a metastable operation point)

Bistable circuits

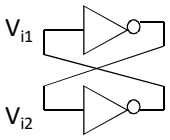
- Cross-coupling of two inverters results in bistable circuit (=two stable states)



- We want to change stored value
  - Apply a trigger pulse at V_{i1} or V_{i2}
  - Width of trigger pulse must be larger than the total propagation delay (2x inverter delay)

Bistable circuits (cont'd)

- Cross-coupling of two inverters results in bistable circuit (=two stable states)



- Mainly two approaches:
  - Cutting feedback loop → MUX based latch
  - Overpowering feedback loop → used in SRAMs

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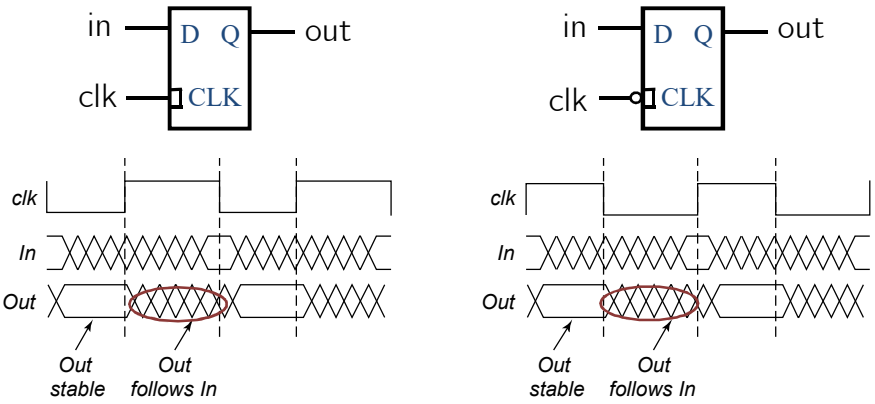
Positive & negative latches



- Positive latch: transparent high
- Negative latch: transparent low

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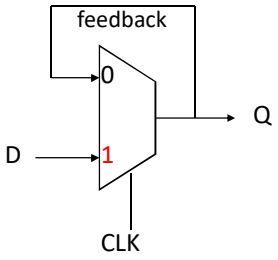
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

MUX–based latches

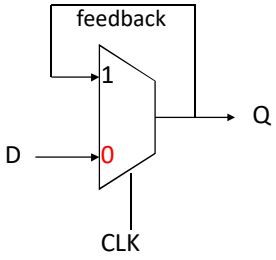
- Change stored value by cutting feedback



positive latch

Q = !CLK*Q + CLK*D

transparent when CLK is high



negative latch

Q = CLK*Q + !CLK*D

transparent when CLK is low

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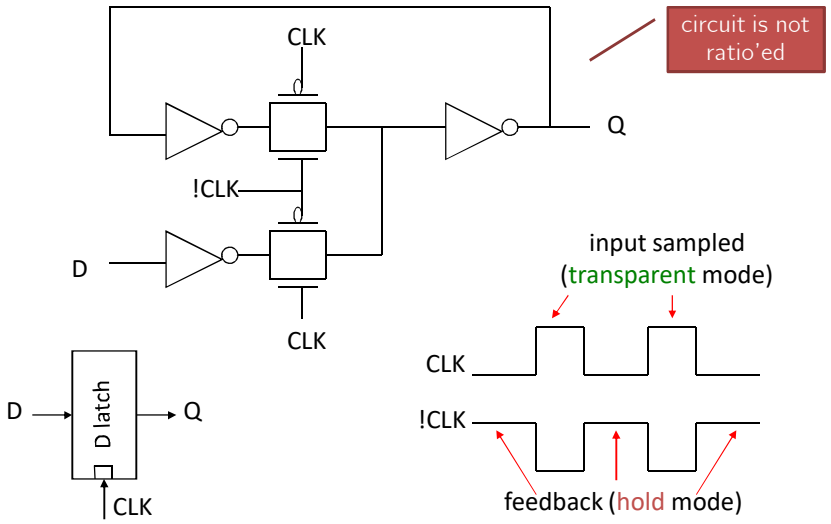
MUX latch with transmission gates



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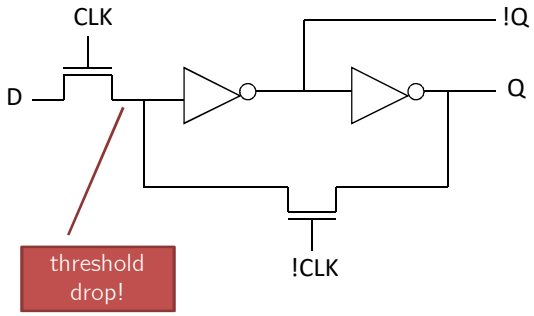
How to reduce the "clock load"

- Clock needs to drive 4 transistors (CL=4)
- Solution: pass transistors



- Reduced noise margin
- Higher leakage currents:
  → WHY?

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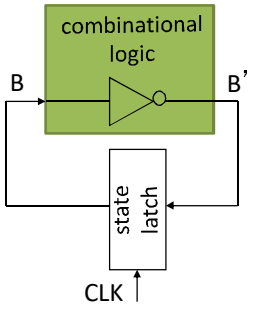
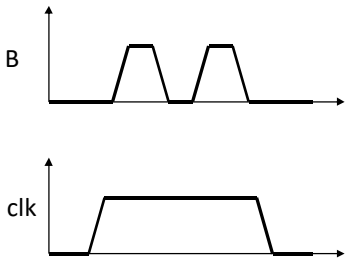
Latch race problem





which value of B is stored?

- Two-sided clock constraint:
  - $T \geq t_{pd,latch}+t_{pd,logic}+t_{su,latch}$
  - $T_{high} < t_{cd,latch}+t_{cd,logic}$

can be hard or impossible to meet both constraints

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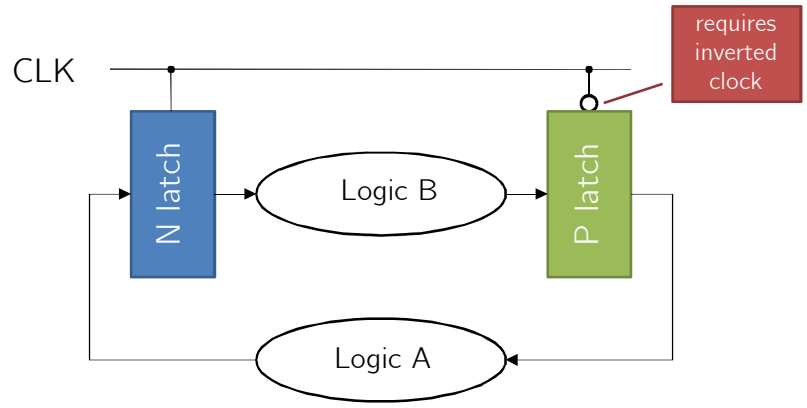
One solution: latch-based design



- What if we (re)move Logic B?

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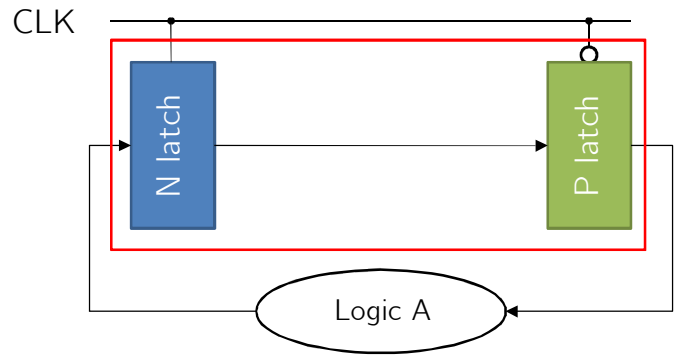
Often a better solution!



- This is a single-edge triggered flip-flop

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Edge-triggered bistables

Flip-flops

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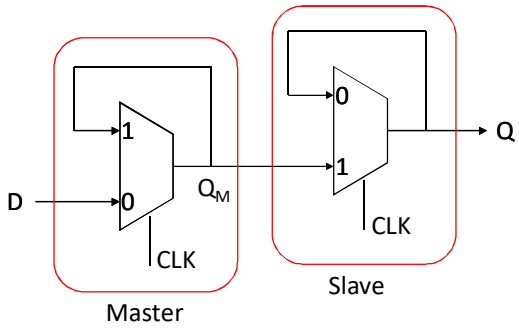
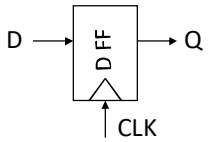
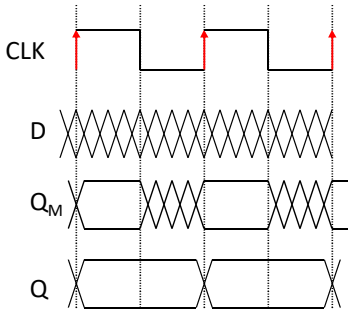
Master-slave edge-triggered flip-flop







CLK = 0 transparent hold

CLK = 0→1 hold transparent

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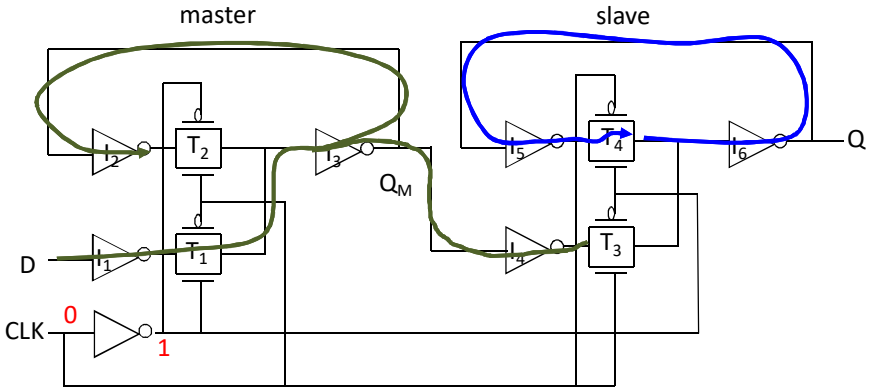
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

MS ET FF implementation



CLK=0 → master transparent; slave hold

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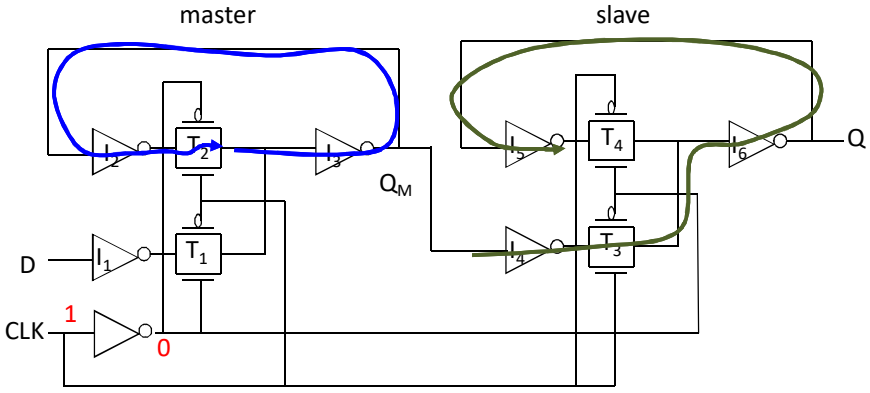
MS ET FF implementation (cont'd)



CLK=1 → master hold; slave transparent

clock load is 8!

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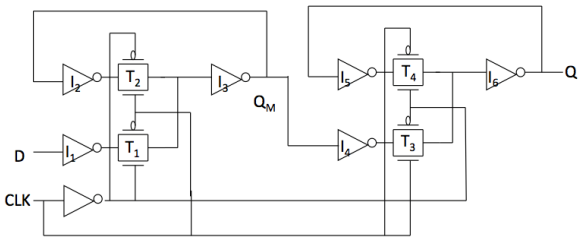
Timing properties of MS ET FF



- Assume propagation delays $t_{pd,inv}$ & $t_{pd,tg}$
- Assume contamination delays = 0
- Assume inverter delay for !CLK = 0

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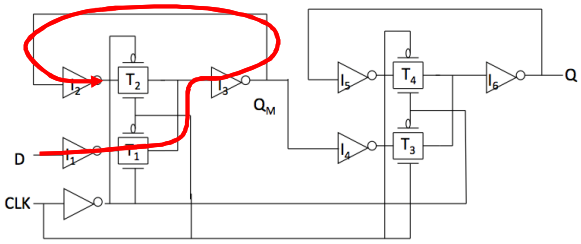
Setup time



- Time before rising edge of CLK that D must be valid

$$t_{setup} = 3 \cdot t_{pd,inv} + t_{pd,tg}$$

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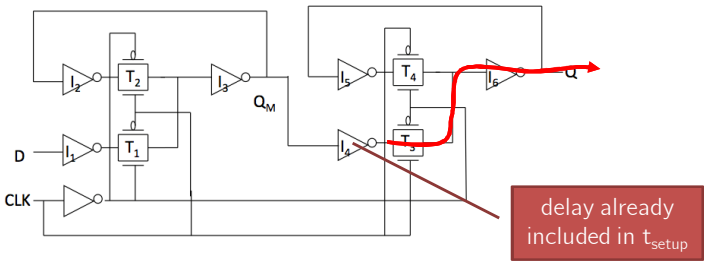
Propagation delay



- Time for Q_M to reach Q (output)

$$t_{pd,ff} = t_{pd,inv} + t_{pd,tg}$$

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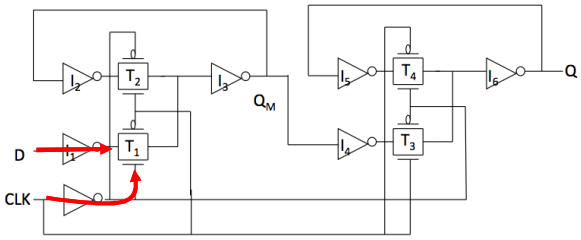
Hold time can be negative



- Time D must be stable after rising edge of CLK signal

$$t_{hold} = -t_{pd,inv}$$

If assuming that CLK inverter has t_{pd}=0

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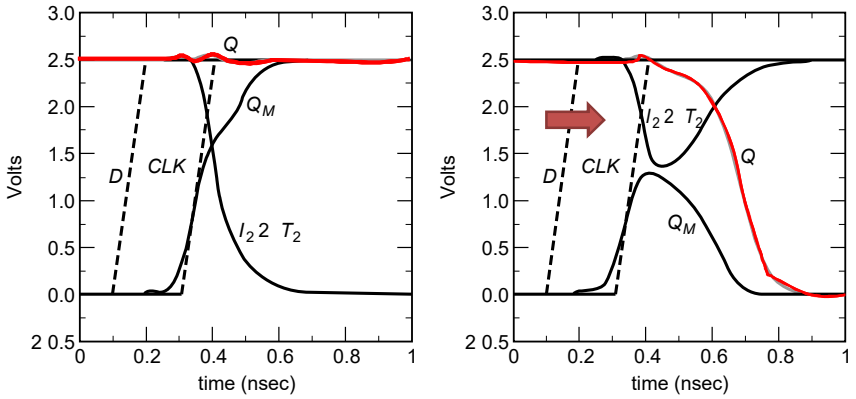
How to simulate setup time



- Shift input D closer to rising CLK signal until Q output is incorrect

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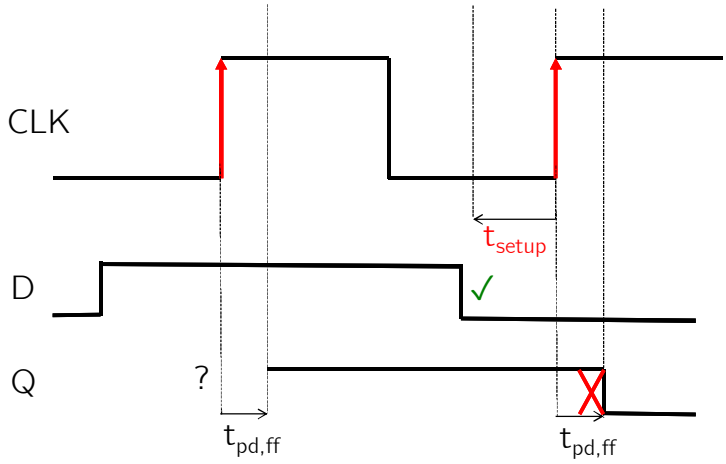
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

How to simulate setup time (cont'd)



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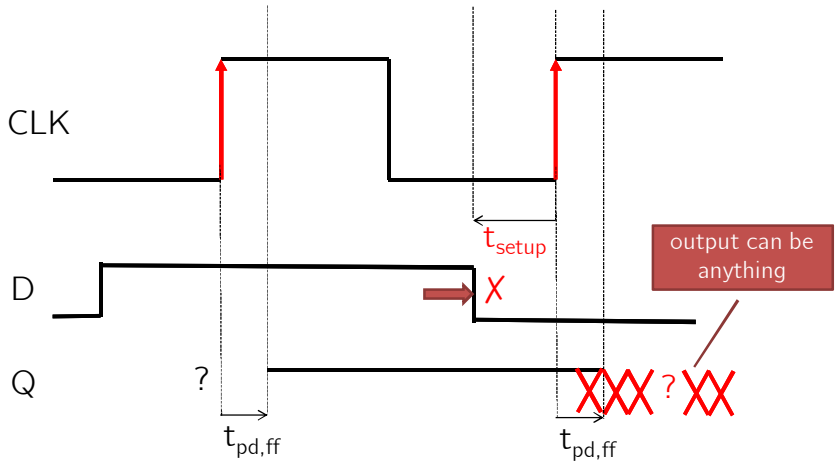
How to simulate setup time (cont'd)



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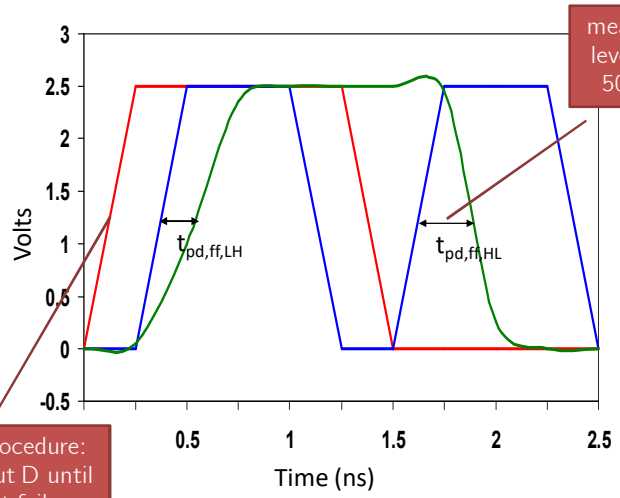
Propagation delay simulation



measured at 50% level of CLK and 50% Q output

same procedure: shift input D until circuit fails

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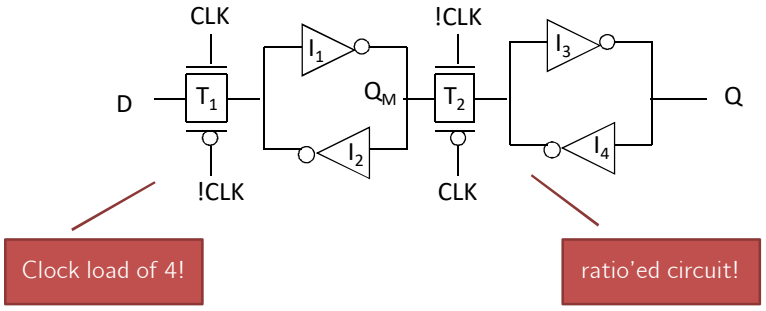
How to reduce the clock load?

- Clock load per flip-flop important: directly affects power dissipation of clock network
- Can reduce clock load at cost of robustness



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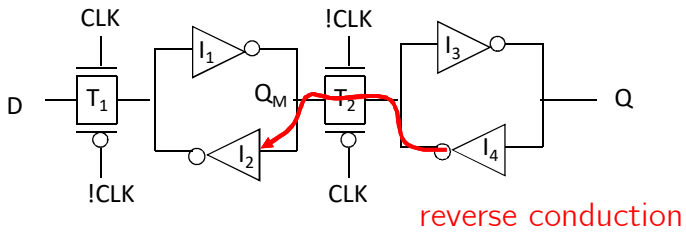
Sizing of reduced clock-load MS FF



- To switch state of master, T_1 must be sized to overpower I_2 (source driver must be strong too)
- To avoid reverse conduction, I_4 must be weaker than I_1 → how can we build a weak inverter?

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For latches and flip-flops

More clock-skew issues

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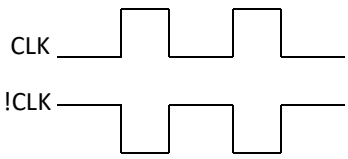
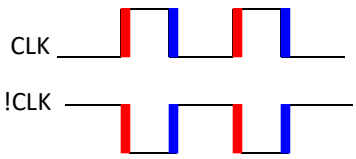
Non-ideal clocks: clock skew



ideal clocks



Non-ideal clocks

clock skew

1-1 overlap

0-0 overlap

clock skew can happen due to uneven wire lengths, capacitances, different fan-outs, etc.

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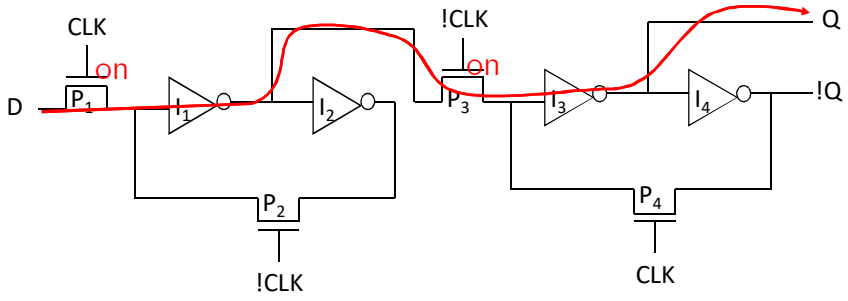
Issue 1: race condition



- Direct path from D to Q during short time when both CLK and !CLK are high (1-1 overlap)

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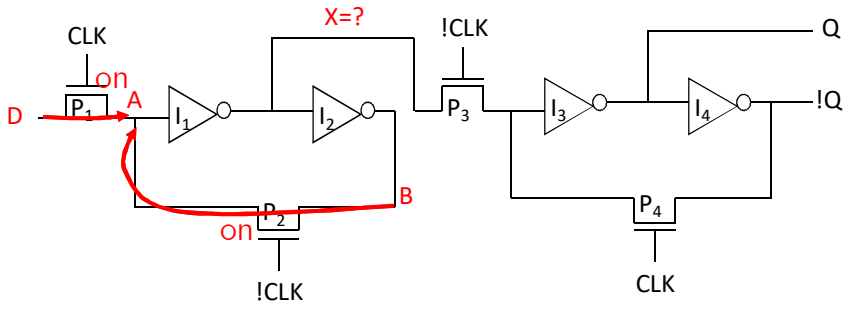
Issue 2: undefined state



- Both B and D are driving A when CLK and !CLK are both high (1-1 overlap)

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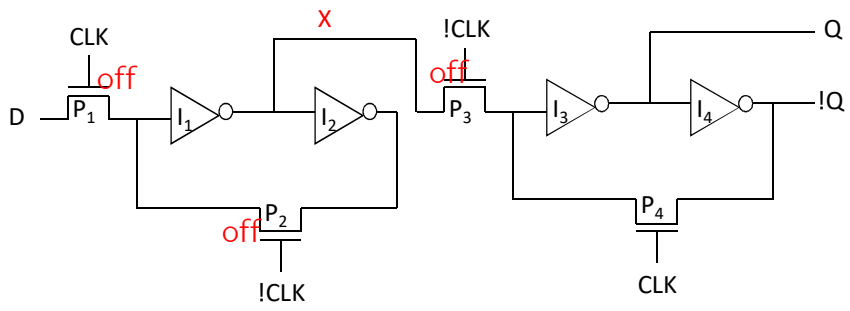
Issue 3: dynamic storage



- When CLK and !CLK are both low (0-0 overlap) level of X stored on parasitic capacitances (might discharge)

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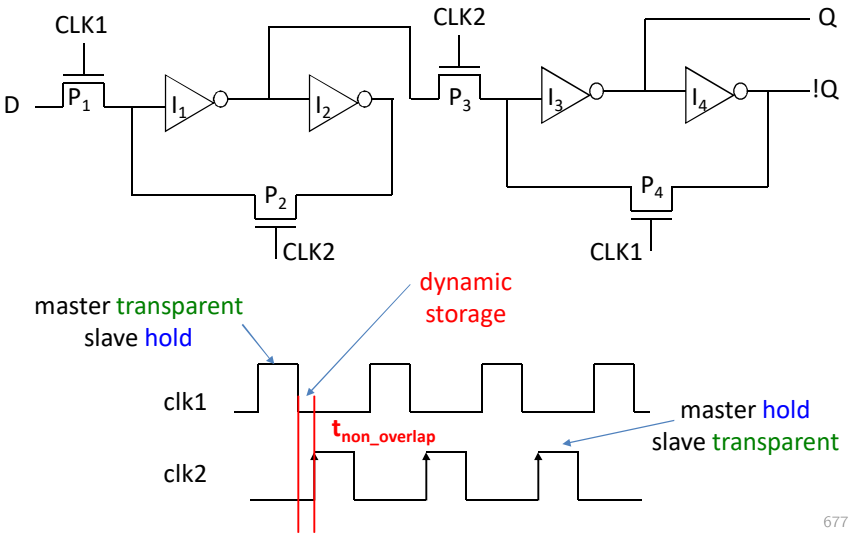
Pseudo-static two-phase ET FF



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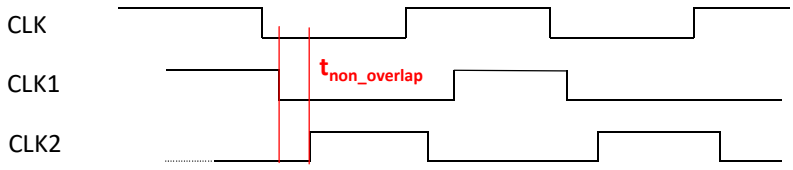
Generating a non-1-1-overlapping clock

- To completely avoid overlapping clocks 1-1 (the 0-0 case is not that critical) we need
  - tools for accurate timing analysis OR
  - non-overlapping clock signals



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Useful for generating non-overlapping clocks

Set-reset (SR) latch

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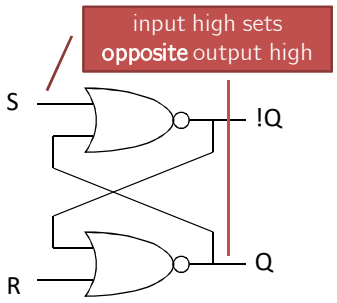
SR latch basics



S	R	Q	!Q	
0	0	Q	!Q	memory
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

- Similar to cross-coupled inverter pair
- Input S and R can force outputs Q and !Q in desired state

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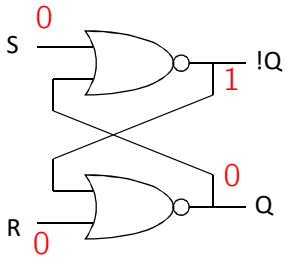
SR latch basics (cont'd)



S	R	Q	!Q	
0	0	Q	!Q	memory
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

- Assume Q=0 and !Q=1
- Assume S=0 and R=0

A	B	!(A+B)
0	0	1
0	1	0
1	0	0
1	1	0

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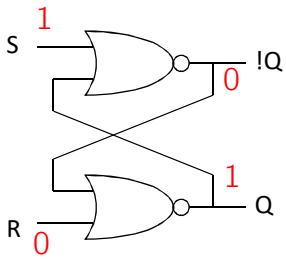
SR latch basics (cont'd)



S	R	Q	!Q	
0	0	Q	!Q	memory
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

- Set S=1 and keep R=0
- Then Q=1 and !Q=0

A	B	!(A+B)
0	0	1
0	1	0
1	0	0
1	1	0

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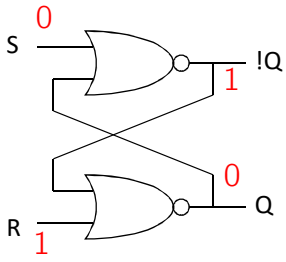
SR latch basics (cont'd)



S	R	Q	!Q	
0	0	Q	!Q	memory
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

- Set R=1 and keep S=0
- Then Q=0 and !Q=1

A	B	!(A+B)
0	0	1
0	1	0
1	0	0
1	1	0

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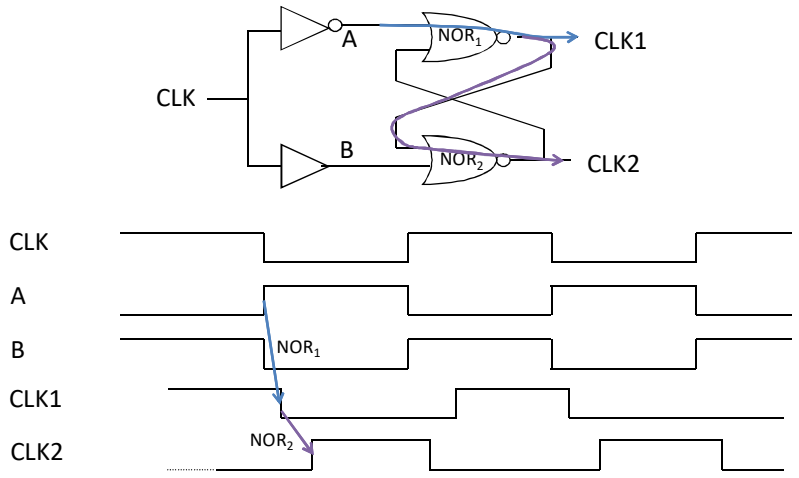
Two-phase non-overlapping clock generator



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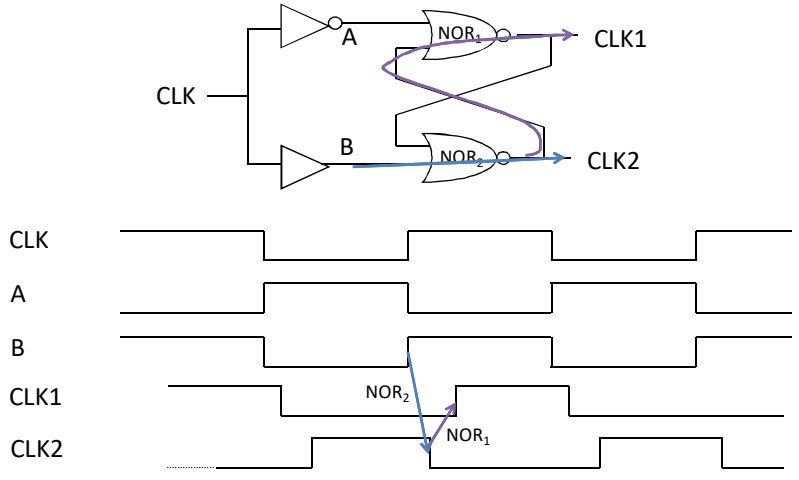
Two-phase non-overlapping clock generator



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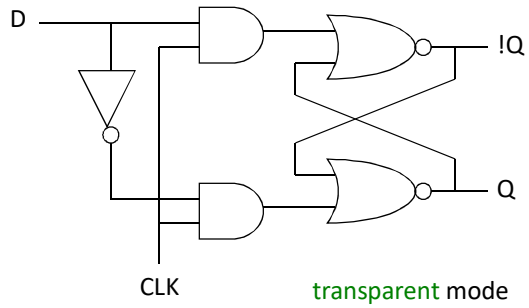
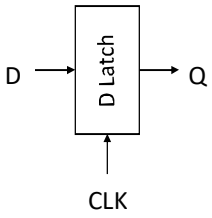
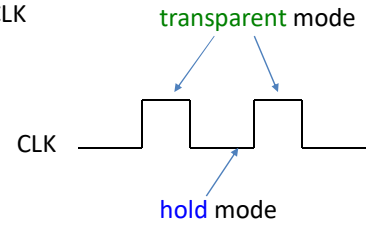
Another storage cell: Clocked D latch







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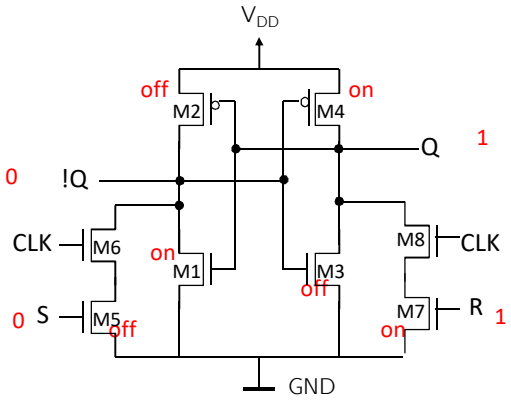
Ratio'ed clocked SR latch



- Can be used in static RAMs (SRAMs)

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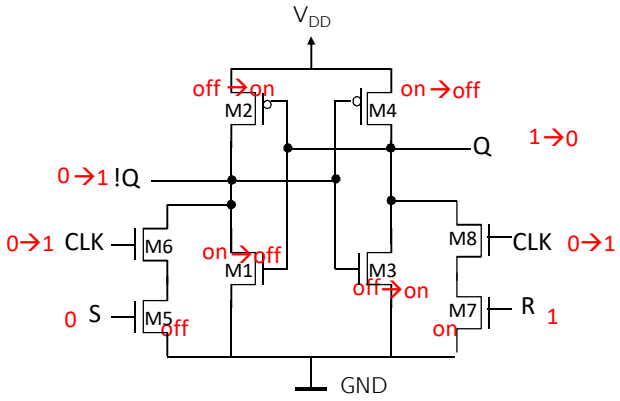
Ratio'ed clocked SR latch (cont'd)



- Ratio'ed → M7 and M8 must succeed in bringing Q low (overcoming M4)

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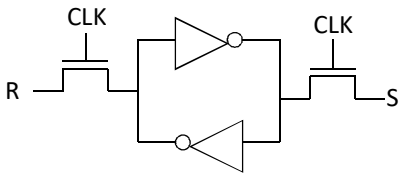
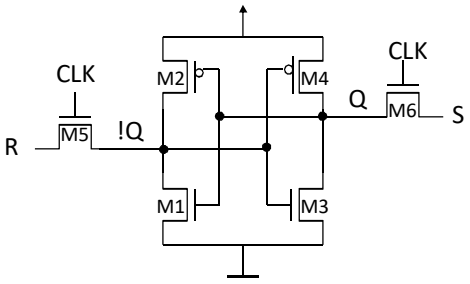
6T CMOS SR Latch



issues with noise margins and static power consumption due to threshold drop across PTs

we will see this structure again when talking about SRAMs



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