ECE4740: Digital VLSI Design

Lecture 15: Dynamic logic

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Recap

Pseudo NMOS and pass-transistor logic

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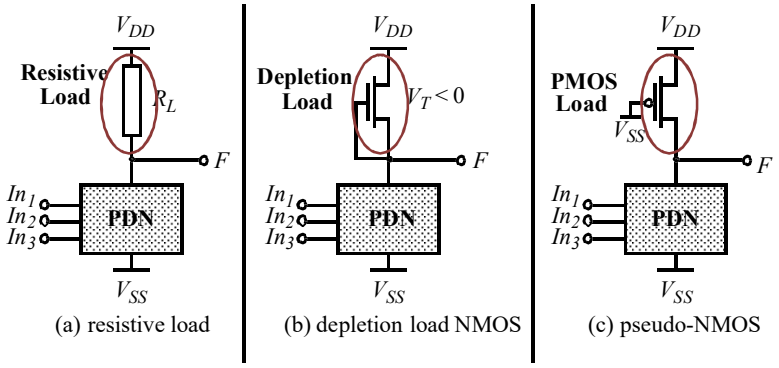
Ratio'ed logic



- Goal: Reduce # of transistors over CMOS
- Ratio'ed = functionality depends on ratios!
- Static power → When exactly?

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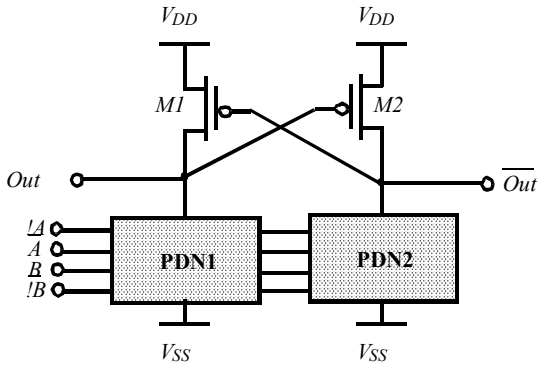
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Improving loads is critical



- Differential cascode voltage switch logic (DCVSL)
- No static power consumption but more routing
- Gates keep state → why could this be useful?

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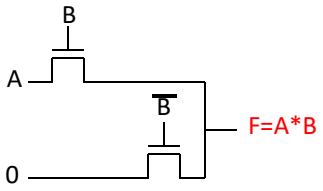
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Pass transistor logic: AND gate



A	B	F=A*B
0	0	0
0	1	0
1	0	0
1	1	1

- Requires 4 logic gates (needs an inverter)
- CMOS logic would require 6 logic gates
- The gate has no rail-to-rail swing
- Non-inverting logic

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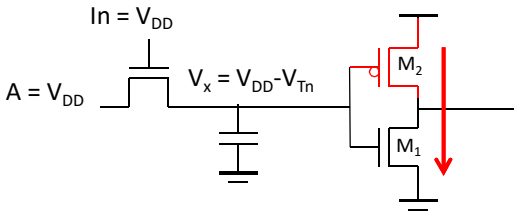
Key issue: static power



- Pass transistor suffers from body effect
- M_2 may be weakly conducting forming a path from V_{DD} to GND
- Can fix with level-restorer transistor

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We can go faster

Dynamic logic

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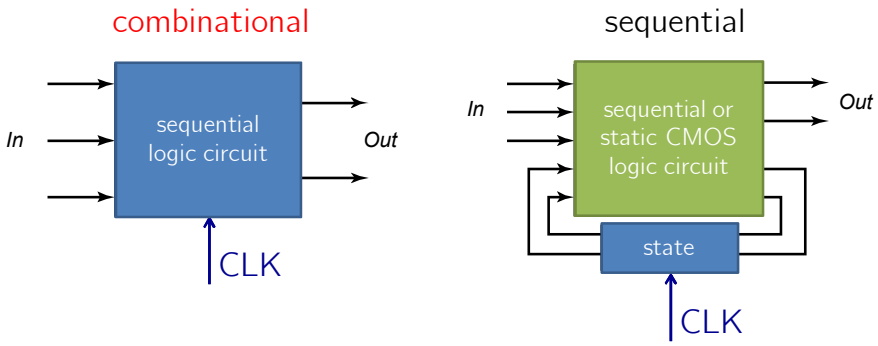
Do not confuse with sequential logic



- Sequential logic circuit considers input history
- Dynamic logic may also have a clock input!

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What is dynamic CMOS?

- Static CMOS circuits:
  - Output is (except during switching) connected to GND or V_{DD} via low-resistance path
  - N-input gate requires at least 2N transistors
- Dynamic circuits:
  - Circuits rely on temporary storage of signal values on capacitance of high impedance nodes
  - N-input gate requires (at least) N+2 transistors

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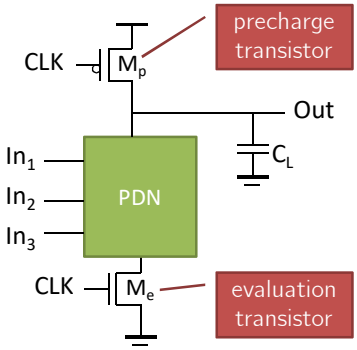
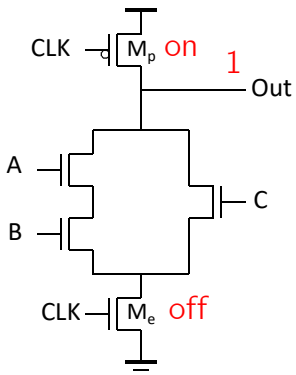
Principle of dynamic gate



- Two-phase operation:
  - Precharge → CLK=0
  - Evaluation → CLK=1



precharge

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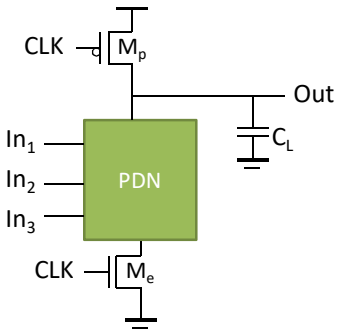
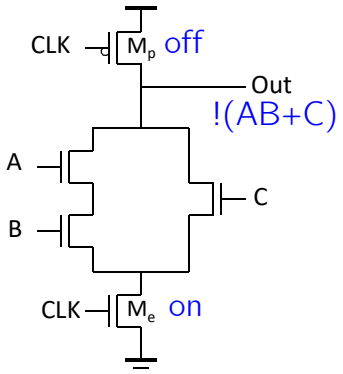
Principle of dynamic gate (cont'd)





evaluation

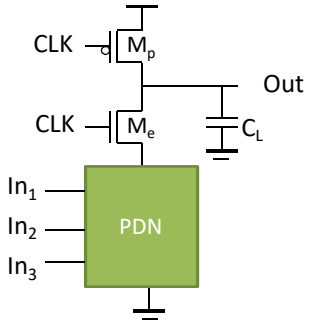
- Two-phase operation:
  - Precharge → CLK=0
  - Evaluation → CLK=1

Conditions on output

- Once output of dynamic gate is discharged, it cannot be charged again until next cycle
- Inputs to gate can make at most one transition during evaluation: no glitches
- Output can be in high-impedance state during and after evaluation (PDN off)
  - State is temporarily stored on C_L

Why not this?

- Clock signal needs to have higher voltage to enable evaluation transistor → slower
- Body effect increases V_T even further
- Worse clock feed-through → I will talk about that today



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Properties of dynamic gates

- Logic function implemented by PDN only
  - # of transistors is N+2 (vs. 2N for CMOS)
  - Smaller area than static CMOS
- Full swing outputs (V_{OL}=GND, V_{OH}=V_{DD})
- Unratio'ed*: sizing only for performance
- No cross-over current: all current provided by PDN goes into discharging C_L

*ignoring parasitic effects

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Properties of dynamic gates (cont'd)

- Faster switching speeds
  - Reduced load capacitance due to lower number of transistors per gate → lower logical effort
  - Reduced C_L due to smaller fan-out
- Power dissipation should be better?
  - Consumes only dynamic power, no cross-over (or short circuit power)
  - Lower C_L: C_{int} and C_{ext}
  - No glitching

FREE LUNCH!?

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What are the disadvantages?

- Power usually much higher than CMOS
  - Higher transition probabilities (due to precharge)
  - Extra load on clock signal
  - Clock signal switches every cycle
  - Every gate needs a clock input
- PDN starts to work as soon as input signals exceed V_{Tn}: $V_M=V_{IH}=V_{IL}=V_{Tn}$
  - Low noise margin (NM_L)
- Needs a precharge/evaluate clock

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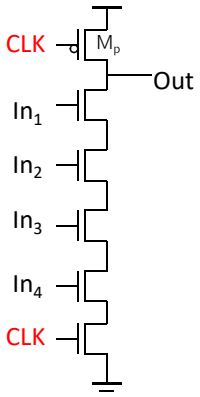
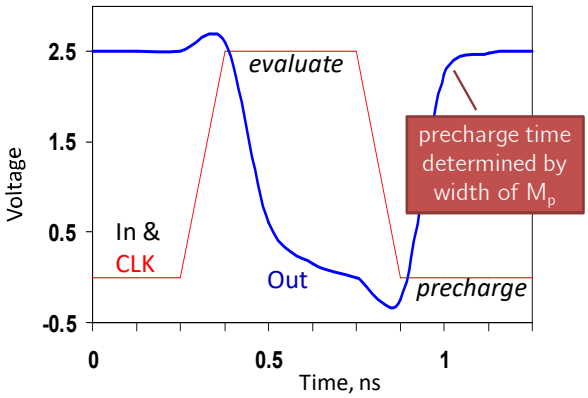
Dynamic behavior





#Trns	V_{OH}	V_{OL}	V_M	NM_H	NM_L	t_{pHL}	t_{pLH}	t_{pre}
6	2.5V	0V	V_{Tn}	2.5-V_{Tn}	V_{Tn}	110ps	0ns	83ps

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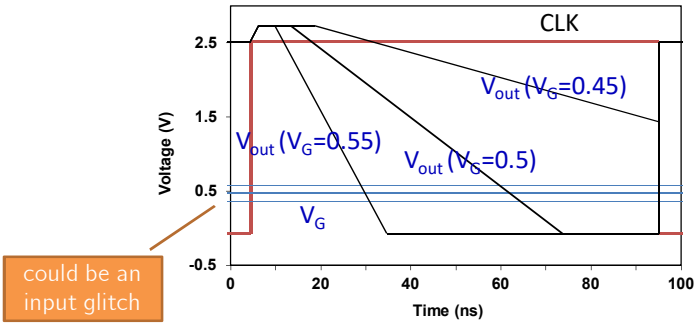
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Gate parameters are time dependent

- Amount of output voltage drop depends on
  - Input voltage
  - Available evaluation time (short is better)



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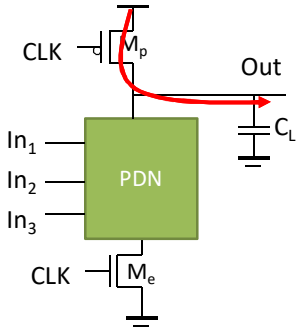
Power consumption



- Power only dissipated when previous Out=0
- Switching activity can be higher than static CMOS
  - Activity does not depend on previous state
  - Activity depends on signal probabilities only

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Dynamic logic

Issues and solutions

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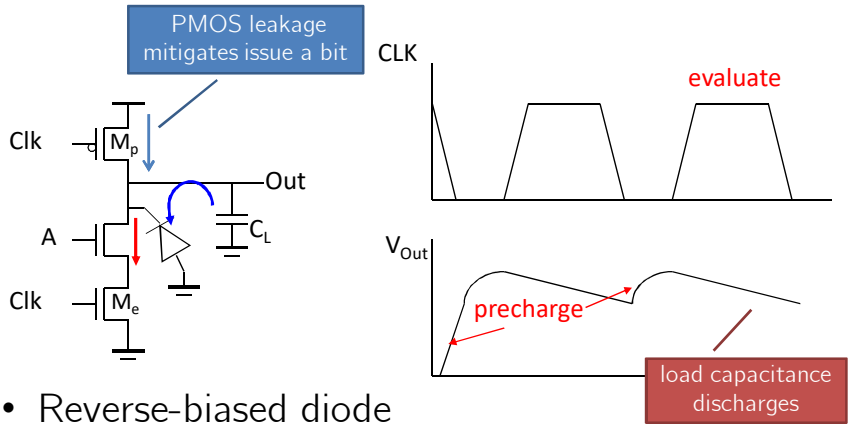
Issue 1: charge leakage



- Reverse-biased diode
- Subthreshold current (dominant)
- Limits **minimum** clock frequency

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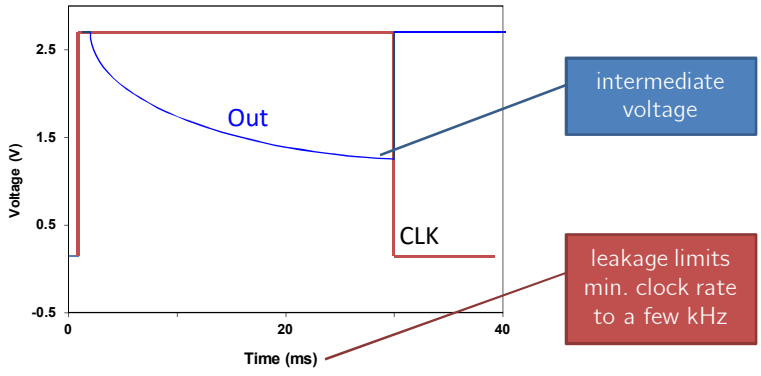
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Issue 1: charge leakage (cont'd)

- Output settles at voltage determined by resistive divider of PMOS & NMOS



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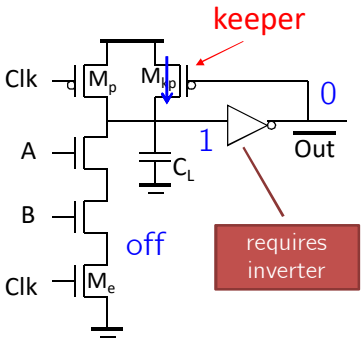
Solution to charge leakage



similar idea as for pass-transistor logic

- During precharge
  - Out=V_{DD} and !Out=GND
- During evaluation
  - PDN off: keeper helps to retain charge
  - PDN on: if M_{kp} is weak, PDN wins → ratio'ed logic!

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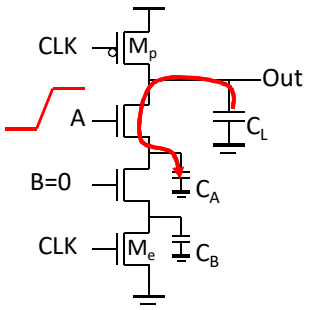
Issue 2: charge sharing



- Charge stored originally on C_L is redistributed (shared) over C_L and C_A
- Leads to static power consumption by downstream gates and possible malfunction

- When $\Delta V_{out} = -V_{DD}(C_A/(C_A+C_L))$ drop in V_{out} is below the threshold of driving gate → malfunction

"capacitive voltage divider"

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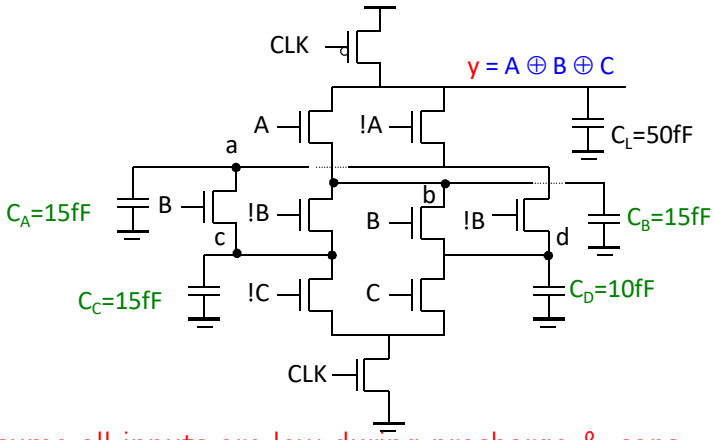
Charge sharing example: XOR3

- What is worst-case voltage drop on node y?



Assume all inputs are low during precharge & caps = 0V

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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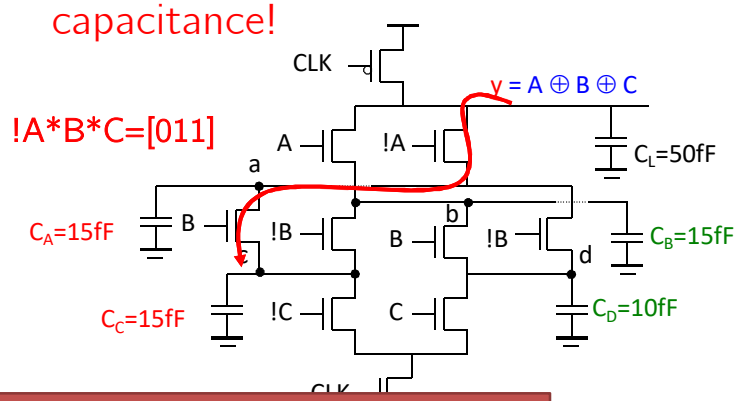
Worst-case charge sharing

- Expose maximum amount of internal capacitance!



$$\Delta V_{out} = -V_{DD}((C_A+C_C)/(C_A+C_C+C_L))$$

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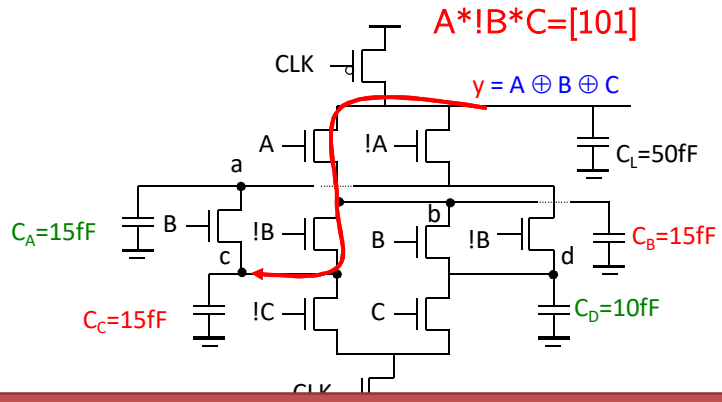
Worst-case charge sharing (cont'd)

- 2nd solution:



$$\Delta V_{out} = -V_{DD}((C_B+C_C)/(C_B+C_C+C_L))=-V_{DD}(30/80)$$

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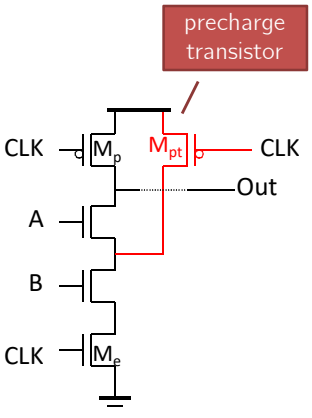
("Solution" to charge sharing)



- Precharge all internal (and critical) nodes using PMOS
  - Increases area
  - Increases power (larger capacitance)
  - Reduces speed (larger capacitance)

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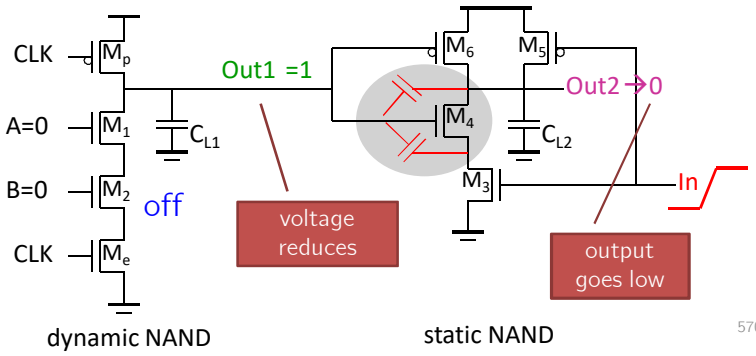
Issue 3: capacitive & backgate coupling

- Susceptible to crosstalk
  - High-impedance output node
  - Capacitive coupling from neighboring node
- Backgate coupling:



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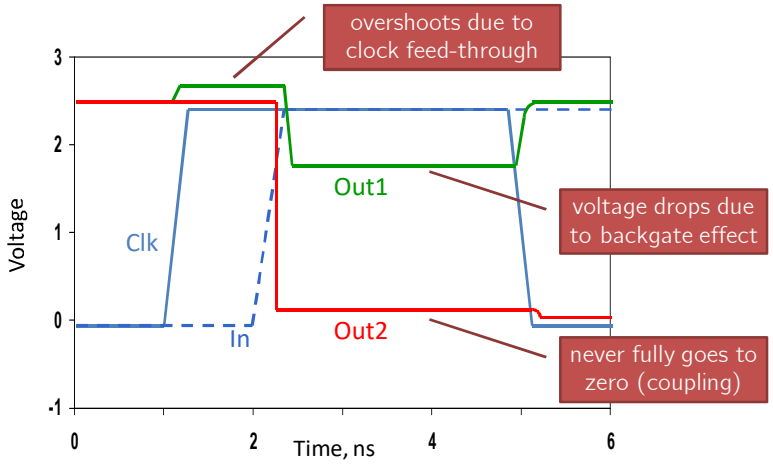
Backgate coupling effect



If Out1 drops too much → incorrect behavior → careful with layout!

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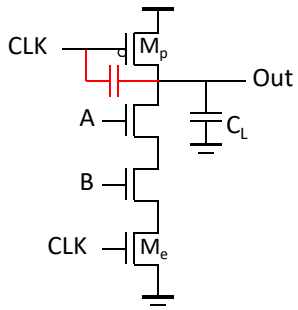
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Issue 4: Clock feedthrough

- Capacitive coupling between CLK input of precharge transistor and dynamic node



- Coupling between Out and CLK input of precharge device due to C_{GD}
- Voltage of Out can rise above V_{DD}
- Fast rising (falling edges) of clock couple to Out

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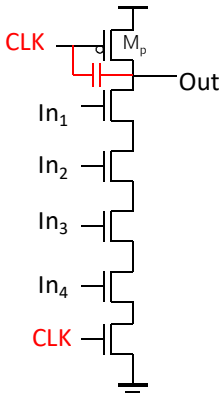
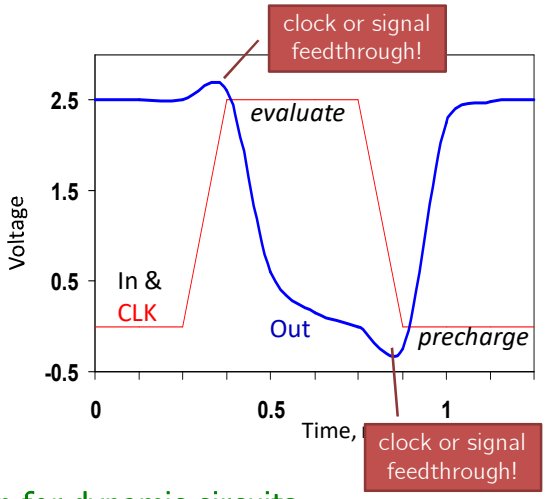
Remember? dynamic behavior





Does not only happen for dynamic circuits

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It's not that easy

Problem with cascading dynamic gates

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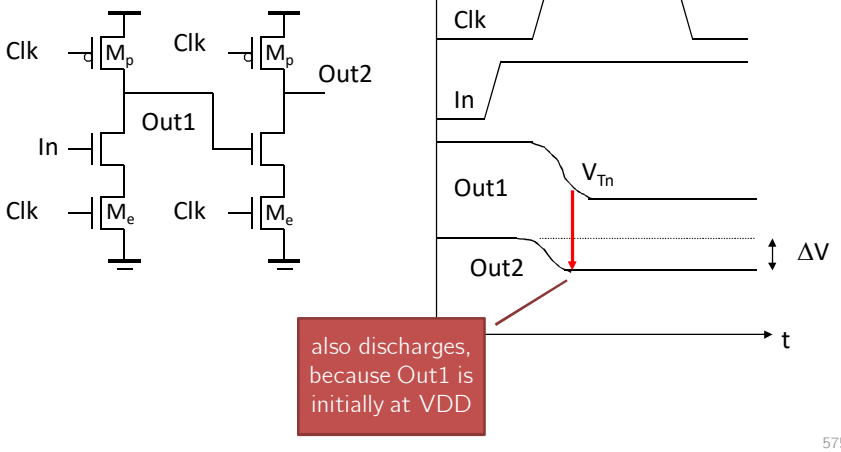
Cascading causes problems

Two inverters:



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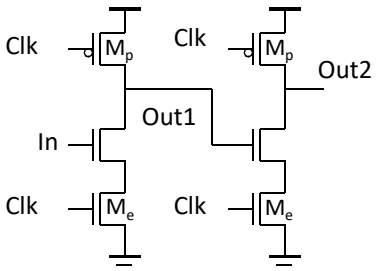
Cascading causes problems (cont'd)



- As nodes are charged to 1, they may cause unwanted discharge
- Setting all inputs to 0 during precharge would fix the problem

- Only a single 0 → 1 transition allowed at inputs during the evaluation period!

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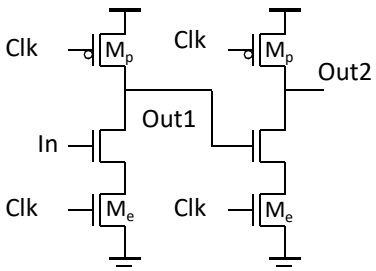
Cascading causes problems (cont'd)



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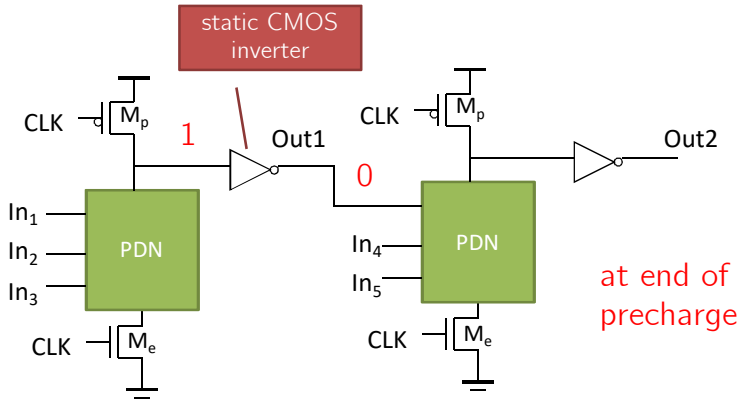
Solution: domino logic



- Inputs to domino gate are set to 0 at end of precharge period

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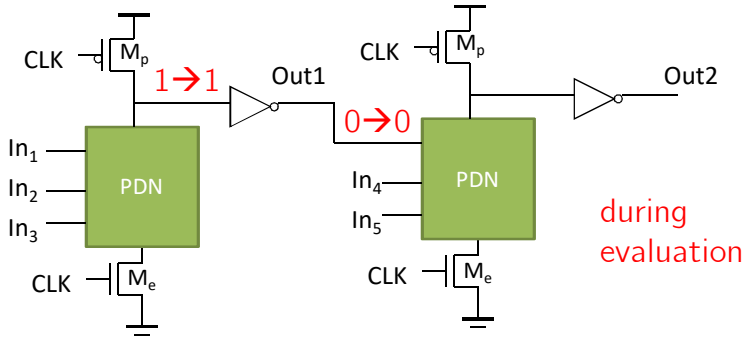
Solution: domino logic (cont'd)



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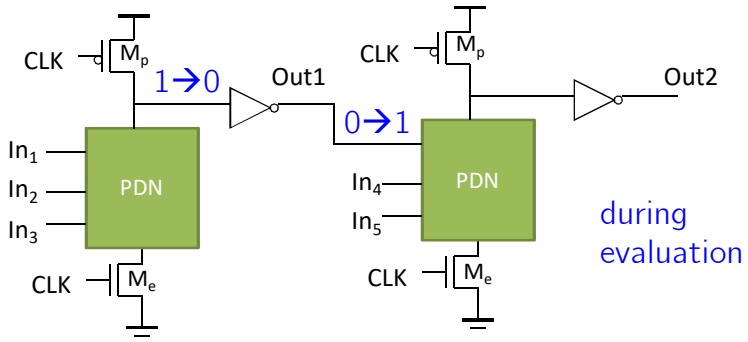
Solution: domino logic (cont'd)



- Only possible transition is 0→1, which guarantees signal integrity

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