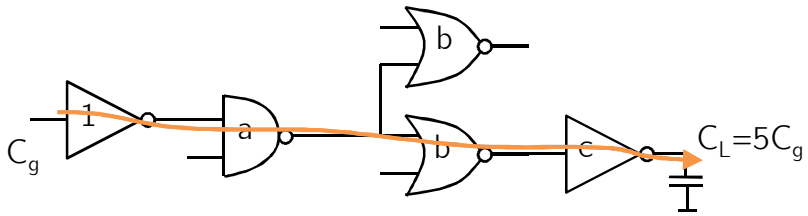
ECE4740: Digital VLSI Design

Lecture 13: Worst-case and best-case delays

Another one

Sizing example

Start with a simple digital circuit



- Compute min. propagation delay
- Assume inverter PMOS:NMOS ratio of 2:1

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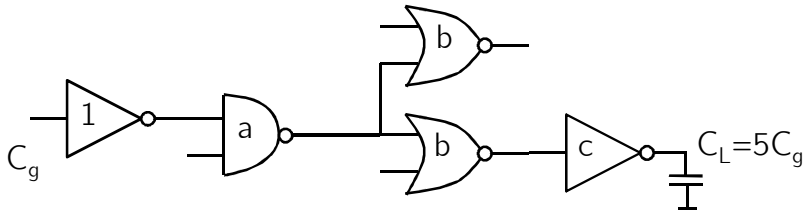
Compute key quantities



- Effective fan-out: H=5
- Path logical effort: G=1*(4/3)*(5/3)*1
- Path branching effort: B=1*2*1*1
- Total path effort: F=H*G*B=22.22
- Optimal gate effort: $f_{opt}=F^{1/4}=2.1712$

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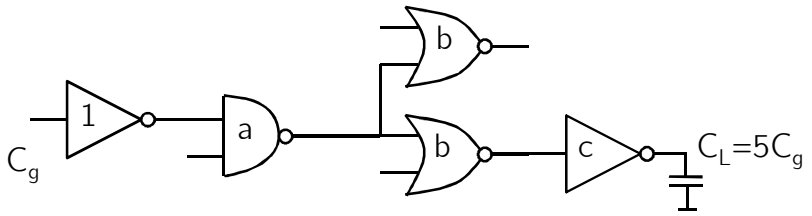
Calculate min. propagation delay



- Min. propagation delay:

$$t_p = t_{p0}\left(P + N\sqrt[N]{F}\right)$$

- P=1+2+2+1=6
- N*f_{opt}=8.6847

sizing not required for min. delay!

$$t_p = t_{p0}14.68$$

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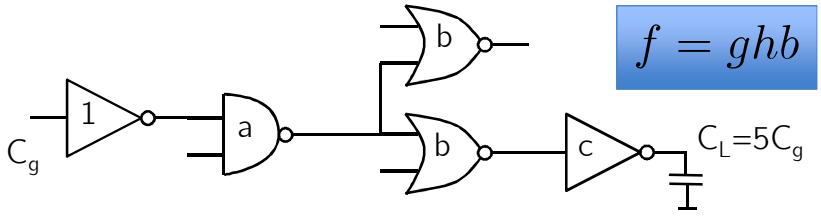
Write down fan-outs



$f = ghb$

- f_{opt}=1*a*1 → a=2.17
- f_{opt}=(4/3)*(b/a)*2 → b=1.76
- f_{opt}=(5/3)*(c/b)*1 → c=2.3
- Final check: $C_L/c=f_{opt}$ → YES

simpler gates are used to drive more capacitance!!!

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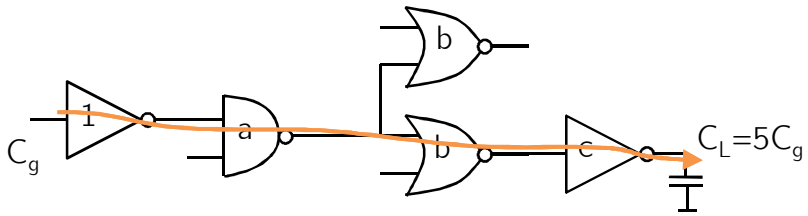
Size transistors



- Size transistors (PMOS/NMOS=2)
  - Hint: Use recursive formula from slide 606:

$$g_{i+1}s_{i+1} = \frac{h_i}{b_i} g_i s_i$$

sizing factor

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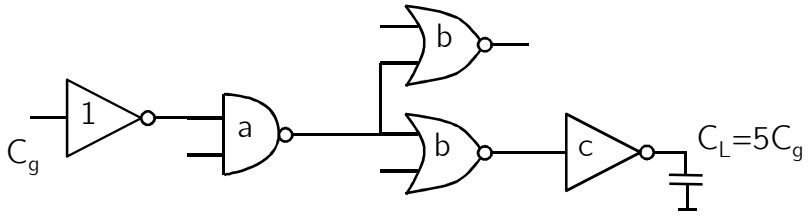
Size transistors (cont'd)



- Begin from start to end and size iteratively

$$g_{i+1}s_{i+1} = \frac{h_i}{b_i} g_i s_i$$

sizing factor

- Here $s_1=1$ → proceed from left-to-right

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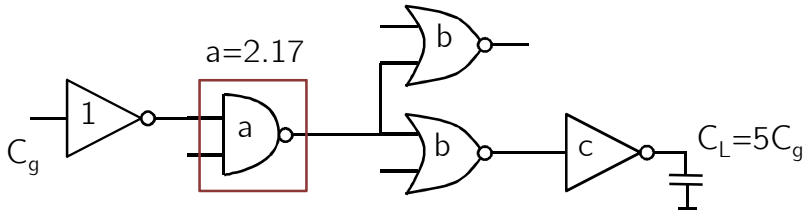
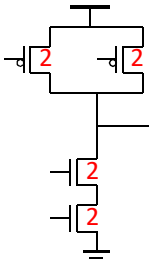
Size transistors (cont'd)



$$g_{i+1}s_{i+1} = \frac{h_i}{b_i} g_i s_i$$

remove own gate effort

- PMOS
  - (W_p=2 to match inv.)*a/g_2=3.25
- NMOS
  - (W_n=2 to match inv.)*a/g_2=3.25



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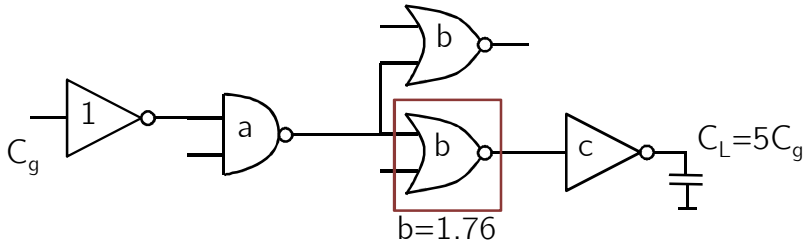
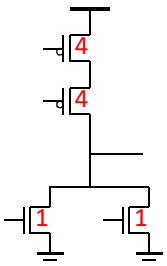
Size transistors (cont'd)



- PMOS
  - (W_p=4 to match inv.)*b/(g_3)=4.22
- NMOS
  - (W_n=1 to match inv.)*b/(g_3)=1.01



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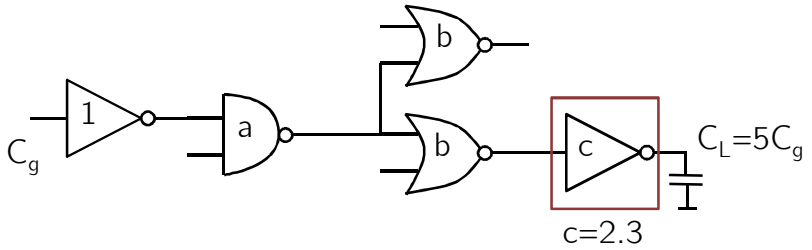
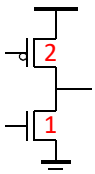
Size transistors (cont'd)



- PMOS
  - (W_p=2 to match inv.)*c/g_4=4.6
- NMOS
  - (W_n=1 to match inv.)*c/g_4=2.3



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This time for CMOS gates

Optimal number of stages

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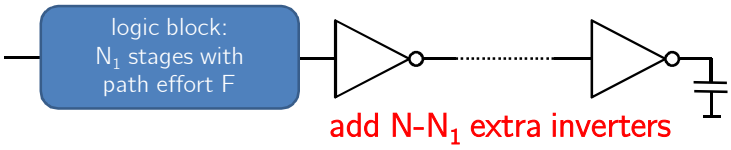
Optimal number of stages



- Total (normalized) delay:

$$D = N\sqrt[N]{F} + \sum_{i=1}^{N_1} p_i + (N - N_1)p_{inv}$$

- Take derivative and set to zero:

$$p_{inv} + \rho(1 - \log(\rho)) = 0 \Leftarrow \rho = \sqrt[N^*]{F}$$

N^* = best # of stages

optimal stage effort

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"Good" number of stages

- Formula has no closed-form solution
- Neglecting parasitics, e.g., p_{inv}
  - Optimal stage effort $\rho \approx 3.59$
- $2.4 < \rho < 6$ → delays within 15% of optimal
- $\rho = 4$ is usually a good pick
  - Rule of thumb for good number of stages:

$$\widehat{N} = \log_4(F)$$

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Recipe for sizing

1. Compute total path effort: F=GHB
2. Estimate "good" number of stages:

$$\widehat{N} = \log_4(F)$$

if you are allowed to add inverters!

3. Estimate (normalized) delay

$$D = \widehat{N}\sqrt[\widehat{N}]{F} + P$$

4. Sketch logic + additional inverters
5. Compute stage effort and size transistors

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Limitations of logical effort approach

- Chicken-or-egg problem
  - Estimating delay depends on logic, which depends on minimum delay you actually want
- Simplistic model
  - Neglects effects of input slopes etc.
  - Optimizes for speed only
  - Not accurate (Cadence sweeps still required)
- But: helps to make quick design decisions!
  - Decisions can be made without actually sizing it

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Important for timing analysis

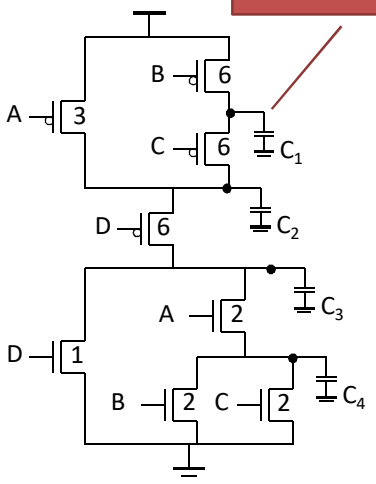
Worst-case and best-case delays

Worst-case delays

just consider node capacitances

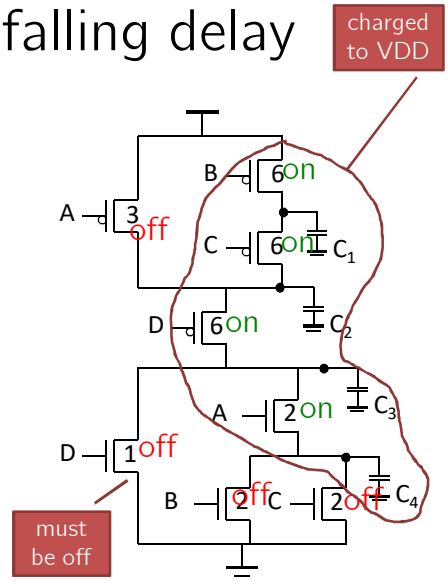
- Worst-case delays depend on how many nodes are charged and how many need to be discharged
- Consider this gate:

$$\text{out} = \overline{D + A(B + C)}$$



Worst-case falling delay

- Output must be 1
- Charge as many capacitances as you can to VDD
  - depends on sizing!
- [ABCD]=[1000]
- Total node caps at VDD: 6+6+6+2



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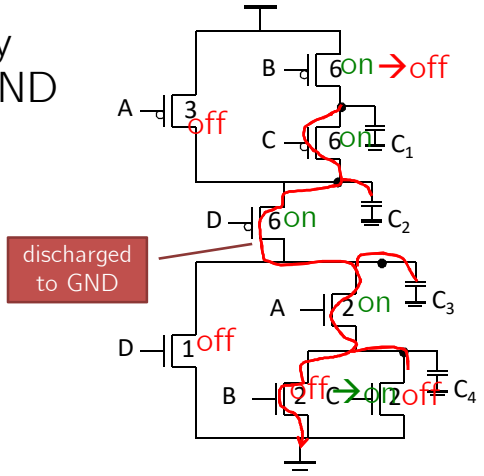
Worst-case falling delay (cont'd)

- Discharge as many capacitances to GND as you can
- Also discharge through weakest transistor!
- Initial state: [ABCD]=[1000]
- End state: [ABCD]=[1100]



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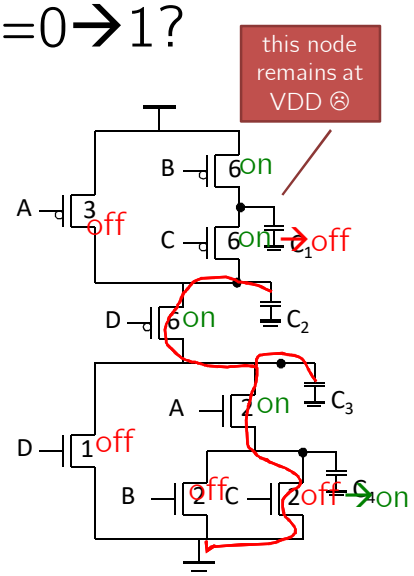
Why not C=0→1?

- Initial state: [ABCD]=[1000]
- End state: [ABCD]=[1010]
- Not the worst case: fewer node caps discharged!



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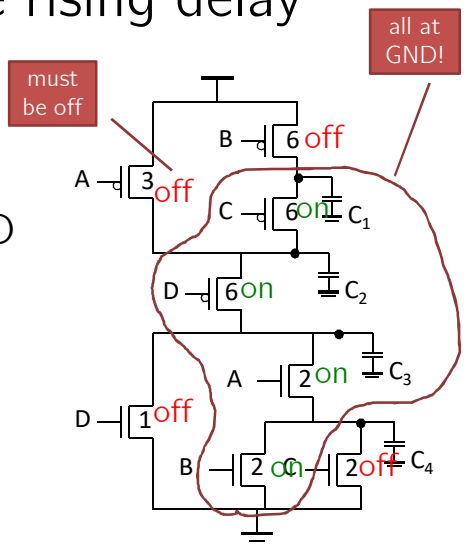
Worst-case rising delay

- Output must be 0
- Discharge as many capacitances to GND as you can
- [ABCD]=[1100]
- Total discharged nodes: 6+6+2+2



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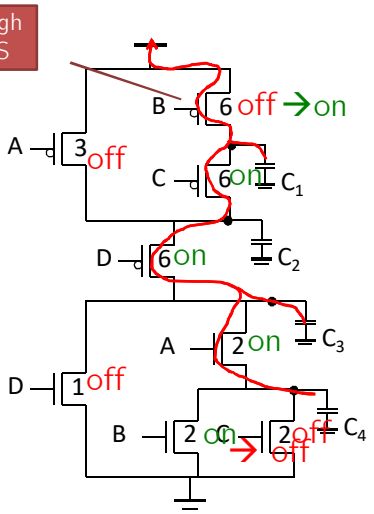
Worst-case rising delay (cont'd)

- Output must go to 1
- Charge as many capacitances as you can
- Initial state: [ABCD]=[1100]
- Final state: [ABCD]=[1000]



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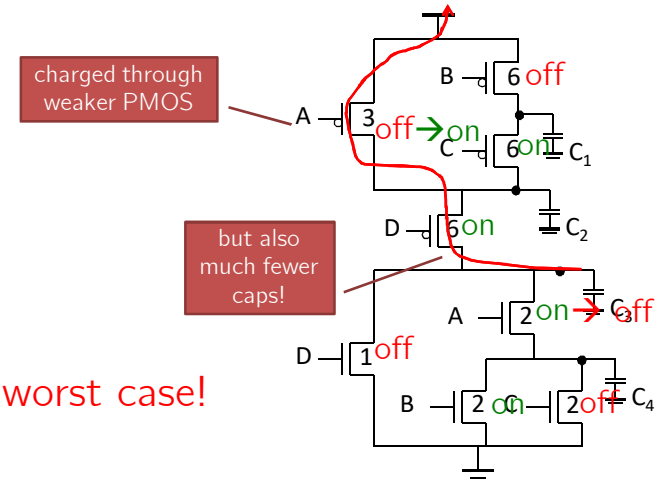
How about A=1→0?



- Not the worst case!

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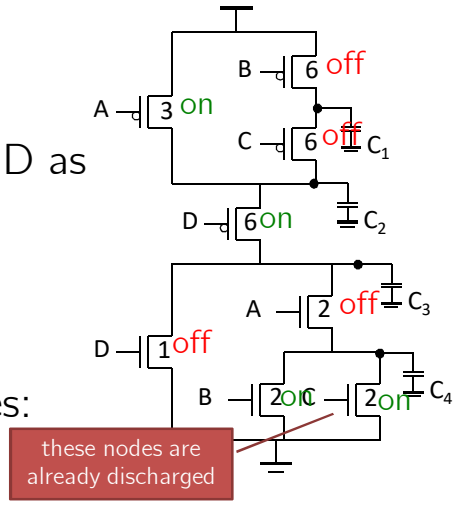
Best-case falling delay

- Output must be 1
- Discharge as many capacitances to GND as you can
- [ABCD]=[0110]
- Total charged nodes: only 3+6



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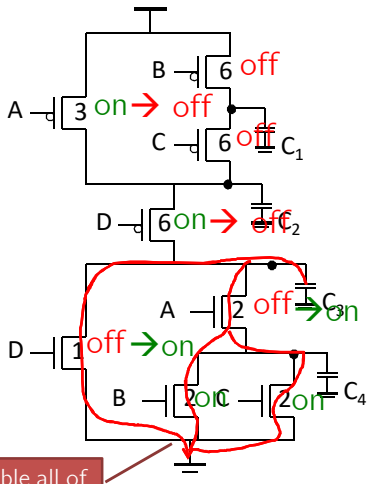
Best-case falling delay (cont'd)

- Discharge as few capacitances as you can
- Discharge through strongest NMOS
- Initial state:[ABCD]=[0110]
- Final state: [ABCD]=[1111]



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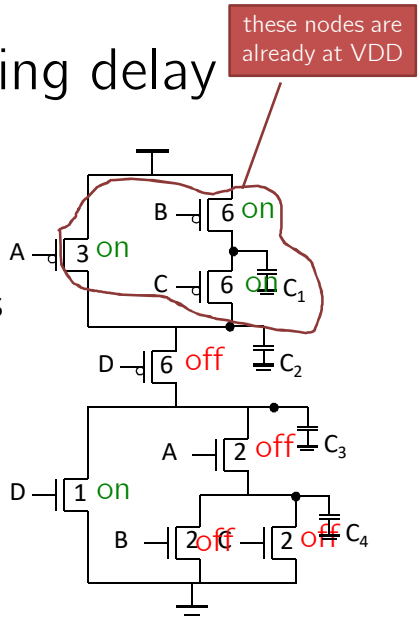
Best-case rising delay

- Output must be 0
- Charge as many capacitances to VDD as you can
- [ABCD]=[0001]



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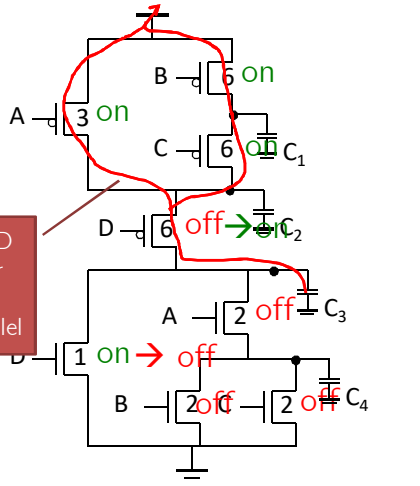
Best-case rising delay (cont'd)

- Output must go to 1
- Charge as few capacitances as you can
- Initial state: [ABCD]=[0001]
- Final state: [ABCD]=[0000]



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