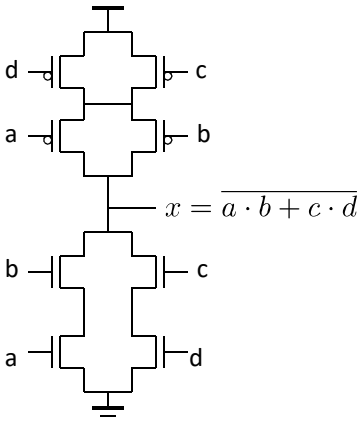
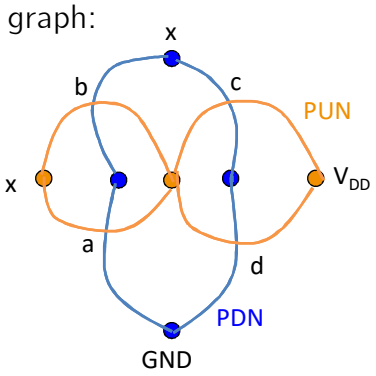
ECE4740: Digital VLSI Design

Lecture 11: More CMOS logic

Example: $x = \overline{a \cdot b + c \cdot d}$



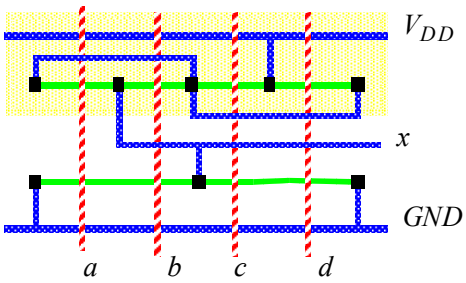
logic graph:

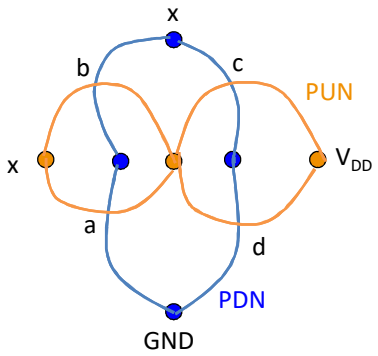


a→b→c→d is a consistent Euler path!

Example: $x = \overline{a \cdot b + c \cdot d}$

stick diagram for {a,b,c,d}





a→b→c→d is a consistent Euler path

412

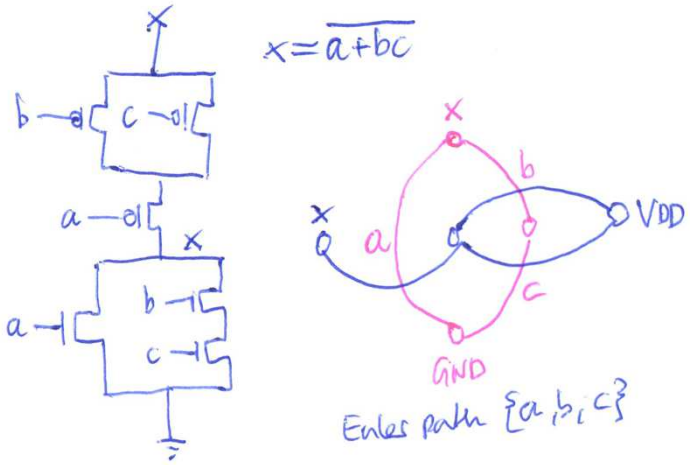
Your turn: $x = \overline{a + b \cdot c}$

- Find truth table
- Draw PUN, PDN, and logic gate
- Draw logic graph
- Find consistent Euler paths
- Draw stick diagram

a	b	c	x
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

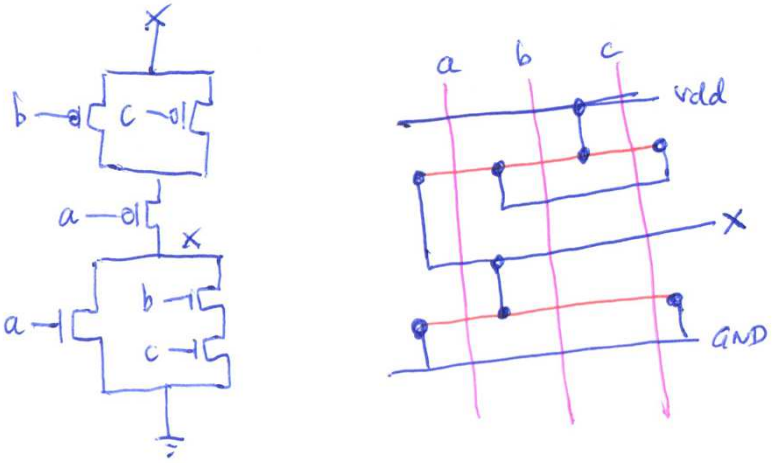
413

Solution: $x = \overline{a + b \cdot c}$



414

Solution: $x = \overline{a + b \cdot c}$



415

Static CMOS gates summary

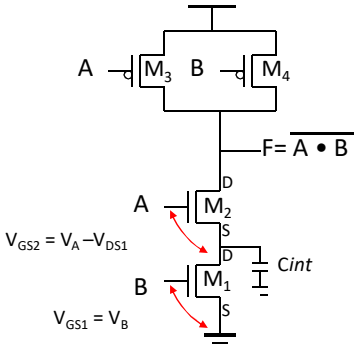
- Essentially behave like a CMOS inverter
- Full rail-to-rail swing; high noise margins
- Logic levels don't depend on device sizes
- Always path to VDD or GND in steady state; low output impedance
- Very high input resistance; nearly-zero steady-state input current (can drive infinite fan-out)
- (almost) no direct path in steady state between power and ground; low static power

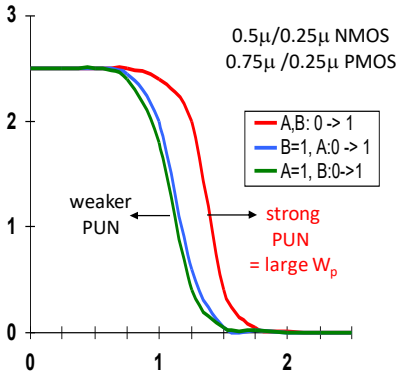
DC characteristics and propagation delay

Static & dynamic properties

DC properties of CMOS gates

- VTC depends on input data applied to gate





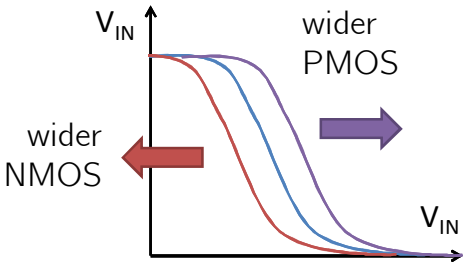
418

Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter6.pdf

Remember the switching threshold?

$$V_M \approx \frac{rV_{DD}}{1+r}$$

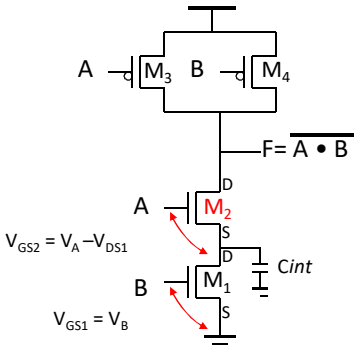
$$r = \frac{\nu_{SATp} W_p}{\nu_{SATn} W_n}$$

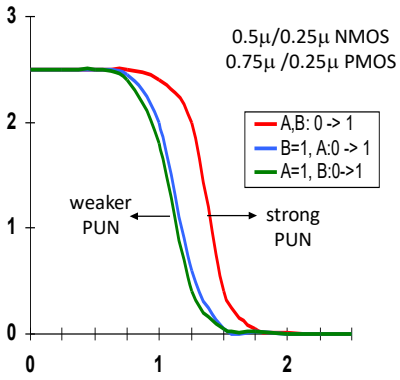


- For A=B=0, both PMOS are simultaneously on
- Parallel PMOS lead to larger effective W_p

419

The other two cases



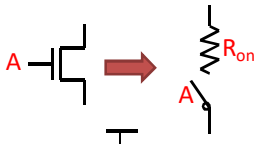


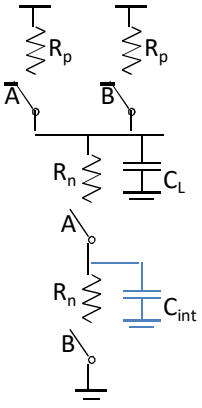
- Threshold of M_2 is higher due to body effect: $V_T = V_{T_0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$

420

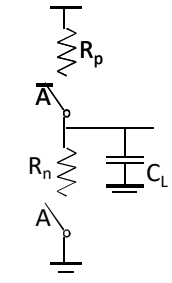
Propagation delay of CMOS logic

- Use RC model for logic gate:

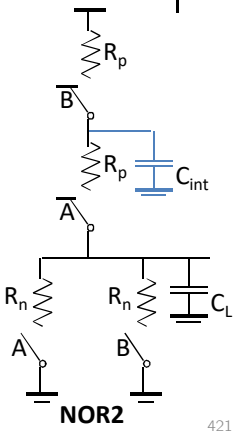




NAND2



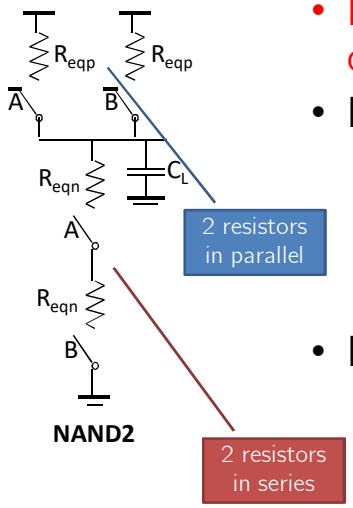
NOT



NOR2

421

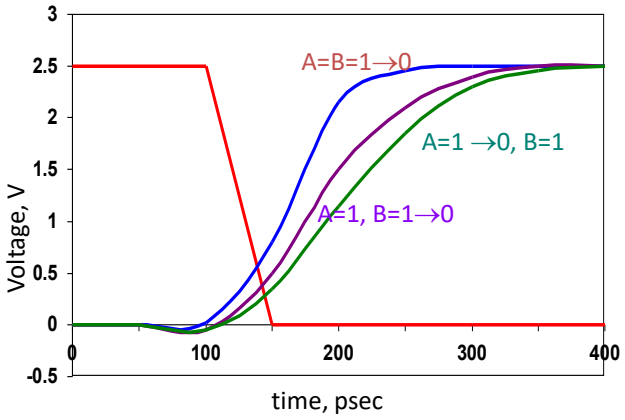
Input data affects propagation delay



- Propagation delay depends on input pattern
- Low-to-high output
  - Both inputs go low
    - $t_{LH} = 0.69\ R_{eqp}/2\ C_L$
  - One input goes low
    - $t_{LH} = 0.69\ R_{eqp}\ C_L$
- High-to-low output
  - Both inputs go high
    - $t_{HL} = 0.69\ 2R_{eqn}\ C_L$

422

Delay dependence on input patterns



Input Data Pattern	Delay (psec)
A=B=0→1	67
A=1, B=0→1	64
A= 0→1, B=1	61
A=B=1→0	45
A=1, B=1→0	80
A= 1→0, B=1	81

NMOS = 0.5µm/0.25 µm, PMOS = 0.75µm/0.25 µm, C_L = 100 fF

423

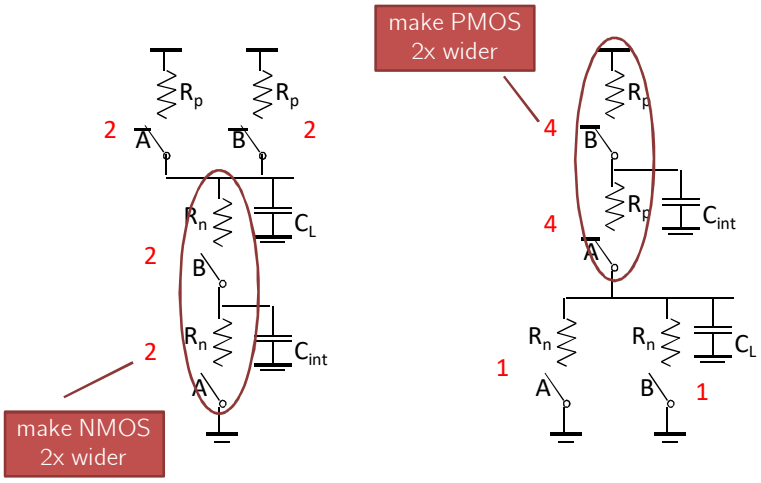
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Similar to that of the CMOS inverter

Static CMOS gate sizing

424

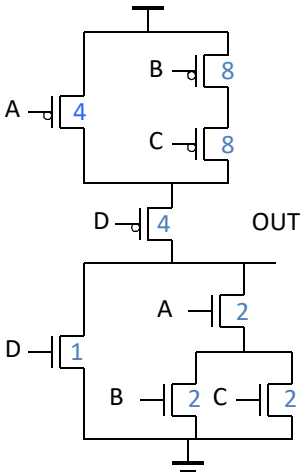
Design goal: reduce max. delay



Assume initial NMOS/PMOS width ratio $W_p = 2W_n$

425

Sizing of a (more) complex gate

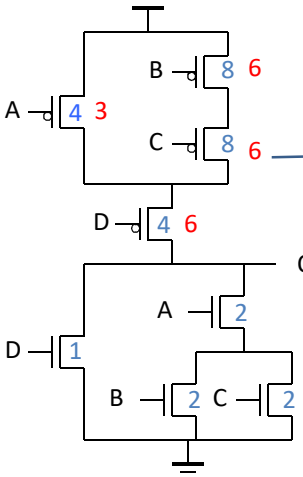


$OUT = \overline{D + A \bullet (B + C)}$

- Assume PMOS/NMOS width ratio of 2:1
- Assume negligible capacitive self loading

426

Multiple solutions possible!



1/6+1/6+1/6 = 1/2
1/8+1/8+1/4 =1/2

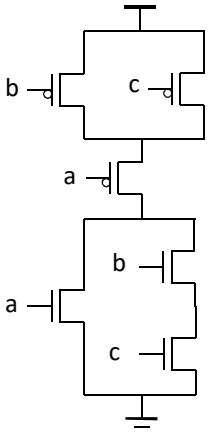
which one is better?

$OUT = \overline{D + A \bullet (B + C)}$

- Assume PMOS/NMOS width ratio of 2
- Assume negligible capacitive self loading

427

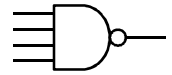
Size this gate: $x = \overline{a + b \cdot c}$

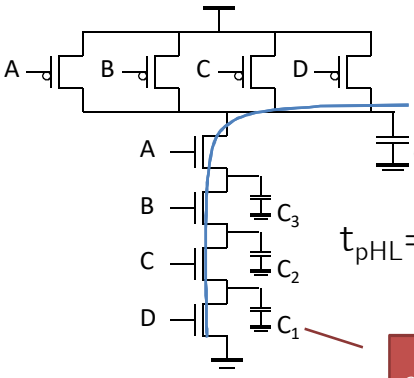


- Assume PMOS:NMOS ratio 2:1 for symmetric VTC
- Are there multiple sizing solutions?

428

Gates with large fan-ins





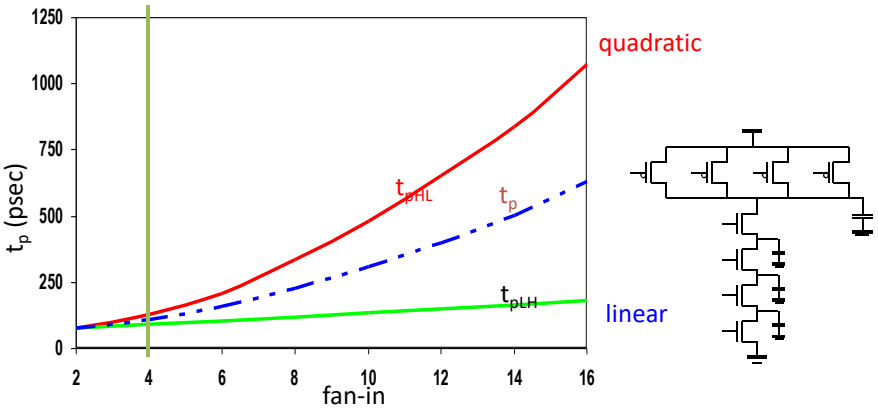
- How can we compute t_{pHL}?
- Use Elmore delay!

$$t_{pHL}=0.69R_{neq}(C_1+2C_2+3C_3+4C_L)$$

junction capacitances and C_{GS}, C_{GD} (Miller effect)

429

Delay t_p as function of fan-in

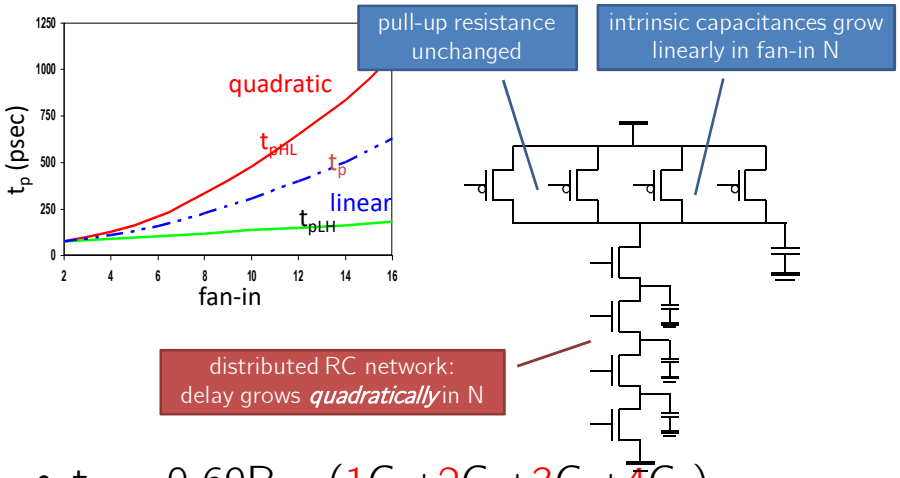


- Gates with fan-in > 4 should be avoided

430

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Delay as function of fan-in (cont'd)



- $t_{pHL}=0.69R_{neq}\,(1C_1+2C_2+3C_3+4C_L)$

431

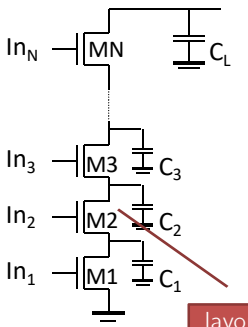
Design techniques

Fast complex gates

Method 1: Transistor sizing

- As long as fan-out capacitance dominates
- Progressive sizing:

careful with self loading



layout difficult for varying sizes!

Recall distributed RC line

M1 > M2 > M3 > ... > MN

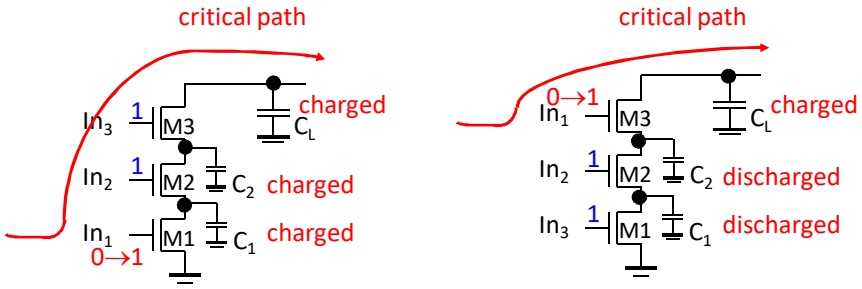
(the FET closest to the output should be the smallest)

Can reduce delay by more than 20%; decreasing gains as technology shrinks

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Method 2: Input re-ordering

- Latest signal should be closest to output



delay determined by time to discharge C_L, C_1, and C_2

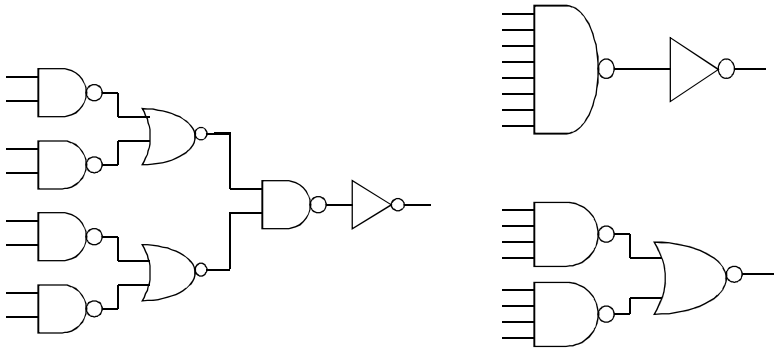
delay only determined by time to discharge C_L

434

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Method 3: Use alternative logic

- F = A•B•C•D•E•F•G•H



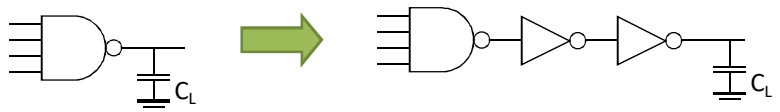
- Called logic restructuring
- See supplementary material for an example

435

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Method 4: Isolate fan-in from fan-out

- Buffer insertion



Large C_L from fan-out

- Important: optimizing propagation delay of an isolated gate is often misguided

436

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

(Method 5: Reduce voltage swing)

- Linear reduction in propagation delay

$$t_{pHL} \approx 0.69 \frac{3}{4} \frac{C_L V_{DD}}{I_{DSATn}} \approx 0.69 \frac{3}{4} \frac{C_L V_{swing}}{I_{DSATn}}$$

- Also reduces power consumption
- But following gate will be much slower
  - requires "sense amplifier" to restore signal level (used in memory design or serial interconnects)

437