ECE4740: Digital VLSI Design

Lecture 10: Static CMOS design

Quick review

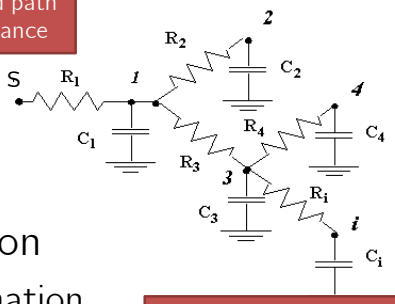
Elmore delay

Elmore delay will be used later!

- Elmore delay at node i is given by

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

shared path resistance



- First-order approximation
  - so-called Padé approximation

best approximation of a function by a rational function of given order

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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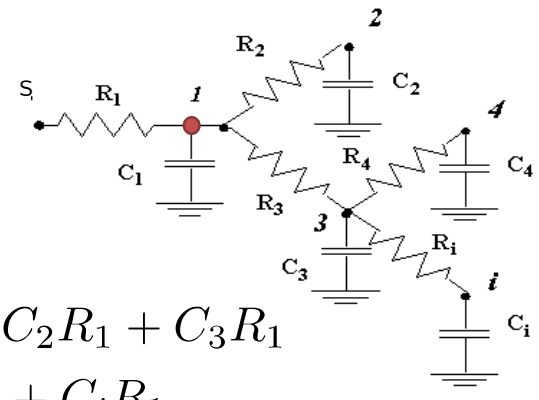
Example 1: Elmore delay

- Elmore delay τ_{D1} for node 1?



$$\tau_{D1} = C_1 R_1 + C_2 R_1 + C_3 R_1 + C_4 R_1 + C_i R_1$$

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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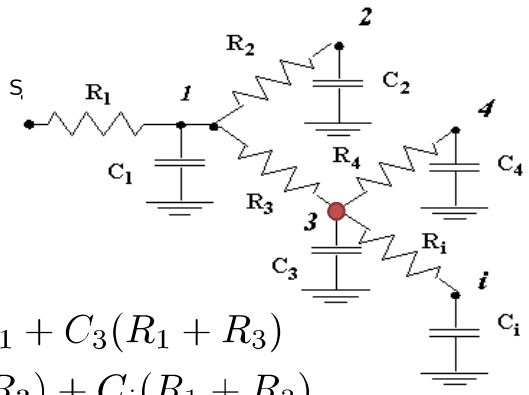
Example 2: Elmore delay

- Elmore delay τ_{D3} for node 3?



$$\tau_{D3} = C_1R_1 + C_2R_1 + C_3(R_1 + R_3) + C_4(R_1 + R_3) + C_i(R_1 + R_3)$$

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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Another wire model

Distributed RC wire

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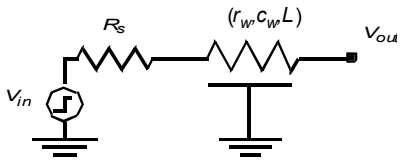
Putting it all together



$$\tau_D = R_s C_w + \frac{R_w C_w}{2}$$
$$= R_s C_w + \frac{1}{2} r_w c_w L^2$$

- With $R_w = r_w L$ and $C_w = c_w L$
- Propagation delay is

use Elmore!

$$t_p \approx 0.69 R_s C_w + 0.35 R_w C_w$$

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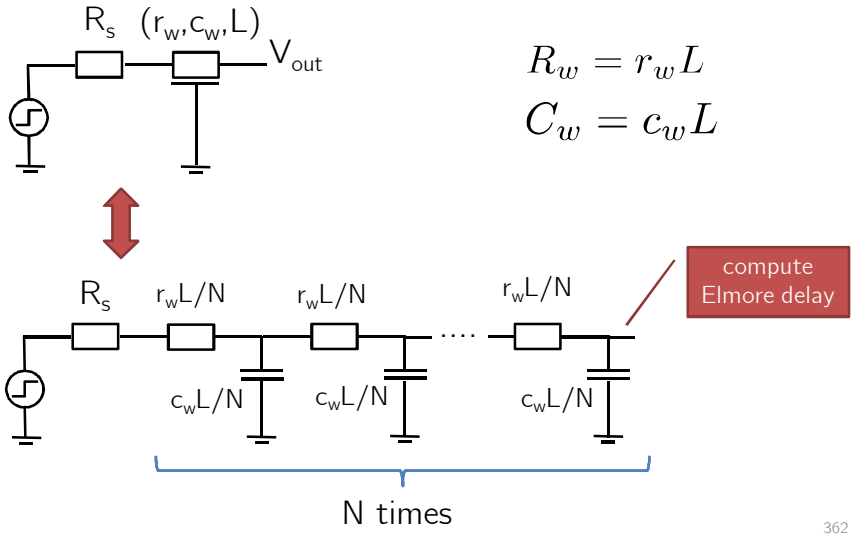
Image taken from: Dr. Sachin Pable Matoshri, College of Engineering and Research Centre

Why is that?



$$R_w = r_w L$$
$$C_w = c_w L$$

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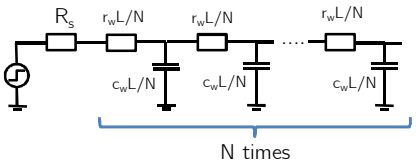
Why is that? (math alert)



$$R_w = r_w L$$
$$C_w = c_w L$$

- Elmore delay:

$$\tau = \left(R_s + \frac{r_w L}{N}\right)\frac{c_w L}{N} + \left(R_s + \frac{r_w L}{N} + \frac{r_w L}{N}\right)\frac{c_w L}{N} + \cdots + \left(R_s + N\frac{r_w L}{N}\right)\frac{c_w L}{N}$$
$$= \frac{N R_s c_w L}{N} + \left(\frac{L}{N}\right)^2 (r_w c_w + 2 r_w c_w + \cdots + N r_w c_w)$$
$$= R_s C_w + (r_w c_w)\left(\frac{L}{N}\right)^2 (1 + 2 + \cdots + N) = R_s C_w + (r_w c_w)\left(\frac{L}{N}\right)^2 \frac{N(N+1)}{2}$$
$$= R_s C_w + r_w L c_w L \frac{N+1}{N2} \xrightarrow{N\to\infty} R_s C_w + r_w L c_w L \frac{1}{2} = R_s C_w + R_w C_w \frac{1}{2}$$

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Putting it all together (cont'd)

$$t_p \approx 0.69 R_s C_w + 0.35 R_w C_w$$

- The delay introduced by wire resistance will be dominant as soon as

$$\frac{R_w C_w}{2} \geq R_s C_w \quad \xrightarrow{R_w = r_w L} \quad L \geq \frac{2R_s}{r_w}$$

- For R_s=1kΩ driving 1μm Al1 wire: L_{crit}=2.67cm → very long

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Rules of thumb: RC or just C?

- RC delays should be considered if t_{pRC} is comparable or larger than t_{pgate}

$$L_{crit} = \sqrt{\frac{t_{pgate}}{0.38 r_w c_w}}$$

- RC delays should be considered if rise/fall time at line input is smaller than RC (rise/fall time of the line):

$$t_{rise} < RC$$

total resistance and capacitance of wire

- When not met, change in signal is slower than propagation delay of wire

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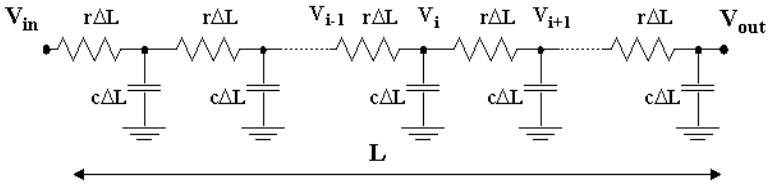
Distributed RC-line



- Diffusion equation:

$$rc\frac{\delta V}{\delta t} = \frac{\delta^2}{\delta x^2}$$

can be solved numerically

(r, c, L)

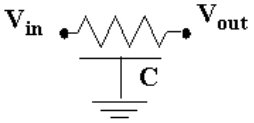


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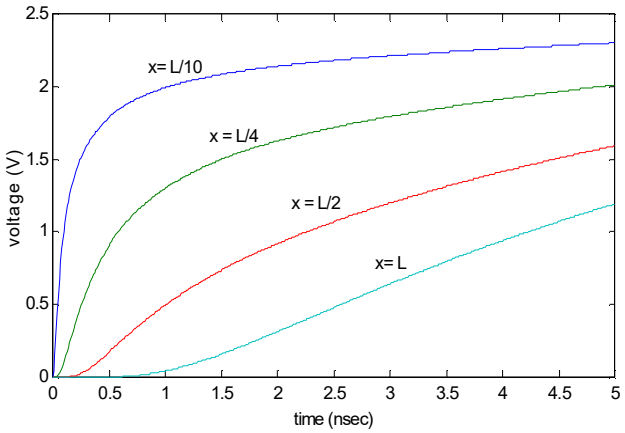
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Step response of RC wire



- Simulated at different spatial locations on wire

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

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If rise/fall times comparable to time-of-flight

(Transmission line)

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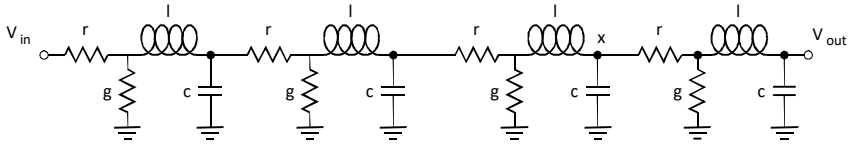
(Lossy) transmission line



- (Damped) wave propagation equation:

$$\frac{\delta^2 V}{\delta x^2} = rc\frac{\delta V}{\delta t} + lc\frac{\delta^2 V}{\delta t^2}$$

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When should I care?

$t_{r/f} << 2.5 t_{flight}$

- If rise/fall times of signal comparable to time-of-flight, then inductance dominates
- Must consider transmission line effects when signal propagates over wire as a wave
- Transmission line on PCB (low R)
- RLC (lossy) model must be considered for very high-frequency circuits

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Lossless transmission line

- If R is small: lossless transmission line

$$\frac{\delta^2 V}{\delta x^2} = lc\frac{\delta^2 V}{\delta t^2}$$

- Step input propagates with speed ν

$$\nu = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

speed of light (in vacuum)

permittivity

permeability

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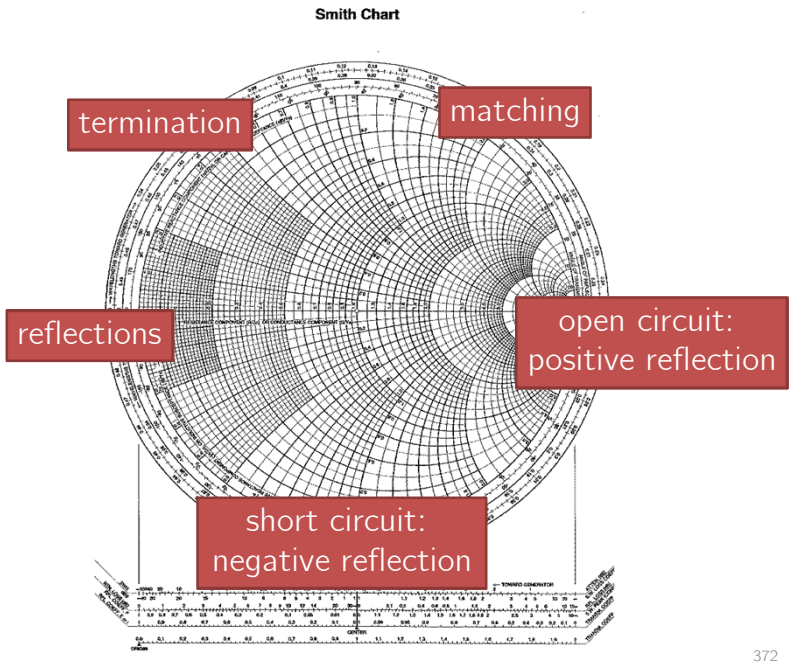

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Image taken from: http://www.antenna-theory.com/tutorial/smith/chart.php

Future challenges & solutions?

- After introduction of copper, not many improvements can be expected
  - superconductors, carbon nanotubes, waveguides, optical, wireless?
- Design solutions
  - Fat/tall wires
  - Bypasses (using better conductors: metal)
  - Repeaters (power/area issues)
  - Efficient floor-planning
- Networks on chip?

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Some tricks

How to reduce wire delays

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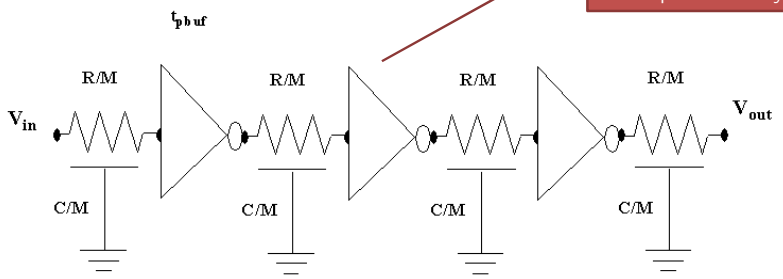
What can we do?

- Use *M* repeaters

don't forget *M* times repeater delay



- Repeaters have delay too: $M = \sqrt{\frac{0.38 r_w c_w L^2}{t_{p,buf}}}$

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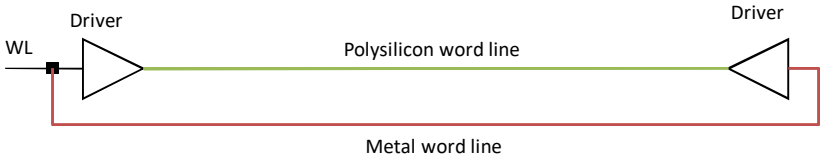
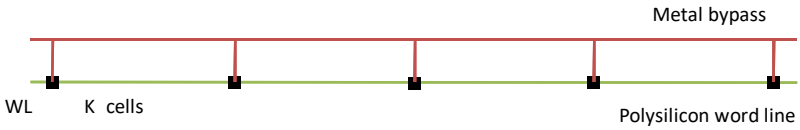
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

What else can we do?

- Use bypasses (e.g., in memories)
  - Drive polysilicon wires from both sides



  - Use metal bypass (better interconnect material)



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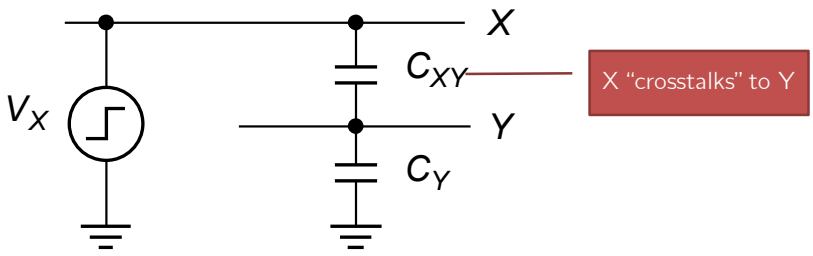
And countermeasures!

Capacitive crosstalk

What is capacitive crosstalk?

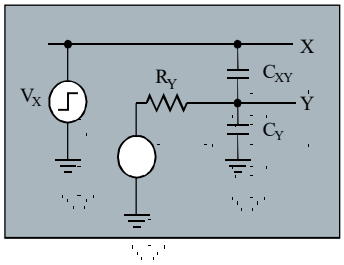


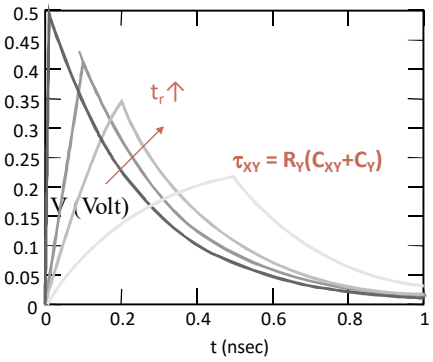
$$\Delta V_Y = \frac{C_{XY}}{C_Y + C_{XY}} \Delta V_X$$

capacitive voltage divider

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Effect on driver node rise time





- Keep time-constant smaller than rise time

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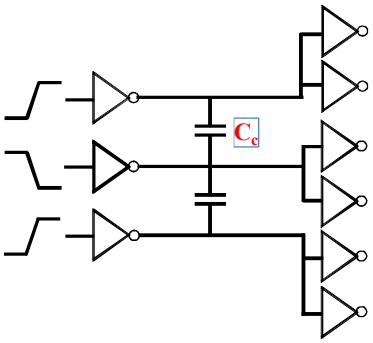
Images taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Crosstalk and Miller effect

- Neighboring lines switch in opposite direction of victim line
- Delay suddenly depends on activity in neighboring wires!



- Miller effect:
  - both terminals of capacitor switched in opposite direction
  - effective voltage doubles, requires additional charge

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Dealing with capacitive crosstalk

- Avoid floating nodes
- Protect sensitive nodes
- (Maximize rise and fall times)
- Differential signaling
- Do not have parallel wires for long distance
- Use shielding wires
- Use shielding layers

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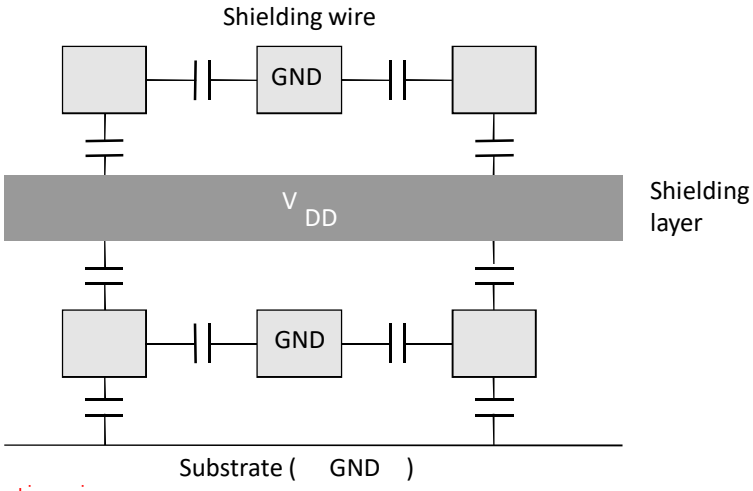
Wire shielding*



*cross-section view

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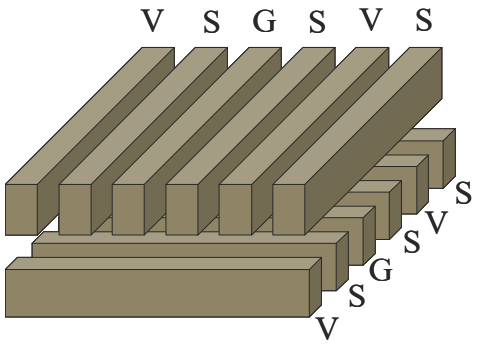
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Structured interconnect



- Trade-off
  - Cross coupling capacitance 40x lower and 2% delay variation
  - Increase in area and overall capacitance

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Wire resistance affects power supply

IR drop & voltage variations

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Impacts of wire resistance: V=IR

- Impact of wire resistance usually seen in power distribution (VDD and GND)
  - Switching causes voltage variation on supply
  - IR drop (from I*R=V)
  - Causes supply voltage variations
- Power supply should minimize…
  - …IR drop and change in current due
  - …current due to simultaneous switching gates

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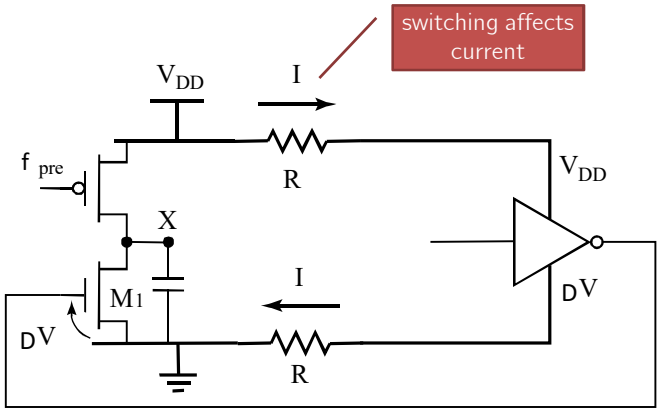
IR switching noise



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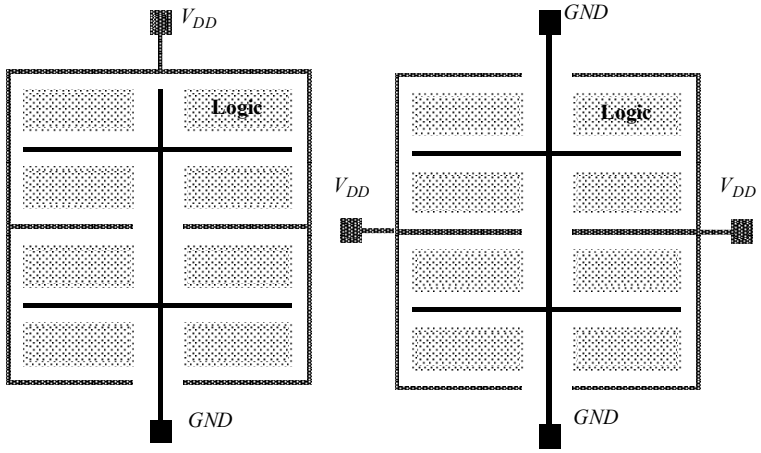
VDD and GND distribution



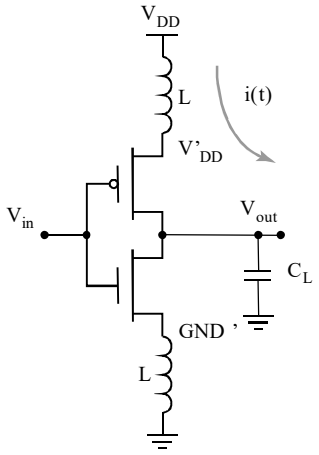
(a) Finger-shaped network (b) Network with multiple supply pins

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic and F. Brewer 387

Inductance effects

- Impact of inductance on supply voltages
  - Change in current induces change in voltage
  - Longer supply lines have larger inductance L

$$V = L\frac{\mathrm{d}i}{\mathrm{d}t}$$



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Dealing with inductance effects

- Separate power pins for I/O and core
- Multiple VDD and GND supplies (!)
- Careful selection of position of VDD and GND pins on the package
- Increase rise and fall times of off-chip signals (to the maximum allowed)
- Schedule current-consuming transitions
- Add decoupling capacitances on board/chip

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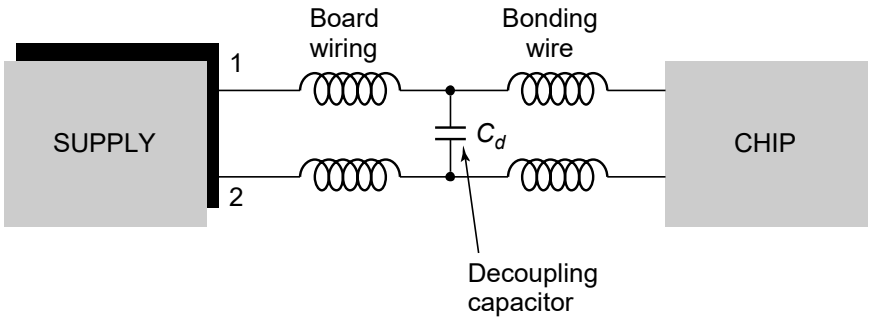
Decoupling capacitors



- On board: right next to supply pins
- On chip: under supply straps, near large buffers, in so-called "filler cells"

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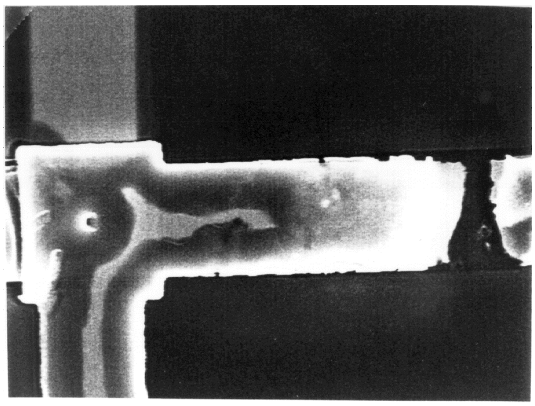
Happens with high current densities

Electromigration

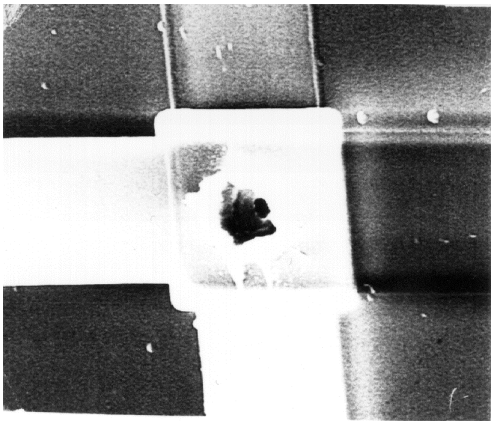
Electromigration



- Limits DC current density to 0.5 to 1mA/μm

Image courtesy of: N. Cheung and A. Tao, UC Berkeley

Electromigration (cont'd)



- Usually happens if device is in use for long time

Image courtesy of: N. Cheung and A. Tao, UC Berkeley

Finally!!!

Static CMOS circuits

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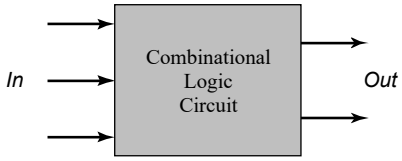
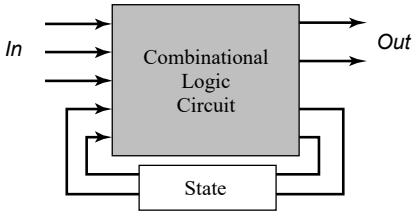
Image taken from: https://www.improgrammer.net/android-nandroid-notdroid-ordroid/

Combinational vs. sequential logic





combinational

$out = f(in)$

sequential

$out = f(in, previous\ in)$

- Sequential logic circuit considers input history

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Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Different logic styles

- Numerous circuit/logic styles exist
- Differ in various metrics
  - Switching speed (propagation delay)
  - Energy dissipation
  - Reliability and robustness against interference
- Most widely used one:

what does the C in CMOS stand for?

"Static complementary CMOS"

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Static CMOS circuits

- At every point in time (except during switching), gate outputs are connected to either VDD or GND via low-resistance path
- Gate outputs assume always (except during switching) value of a Boolean function
- Dynamic CMOS differs:
  - Temporary storage of signal values
  - Storage on C of high impedance nodes

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Properties of static CMOS

- Just a more complicated CMOS inverter
- Robustness against interference and noise
  - Full rail-to-rail swing
  - VOH and VOL are VDD and GND, respectively
- Low static power dissipation (leakage only)
- Low output impedance, high input impedance
- Delay function of C_L and transistor resistance
- Easier to design large circuits for
  - Timing well understood
  - Sizing etc. well understood
  - Excellent CAD tools support

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History

- Invented by Frank M. Wanlass
- Patent in 1963: "Low stand-by power complementary field effect circuitry" (Fairchild)

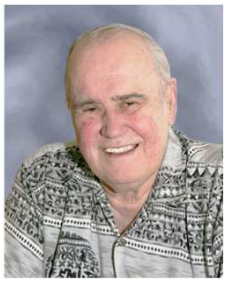

Fig. 5

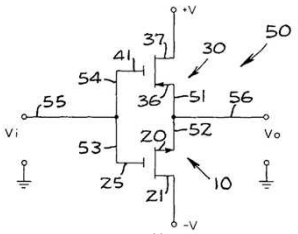

Fig. 6

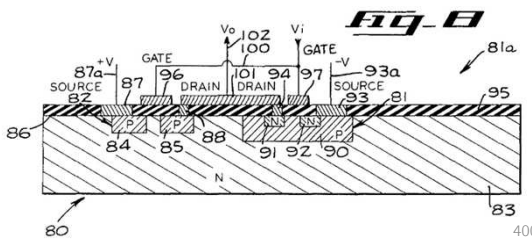

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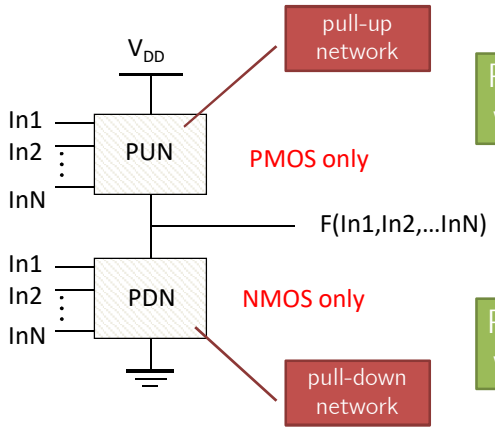
Image taken from: http://www.ithistory.org/honor-roll/dr-frank-marion-wanlass

Static complementary MOS



PUN connect to VDD when F(In1,In2,…)=1

PDN connect to GND when F(In1,In2,…)=0

PUN and PDN are dual logic networks

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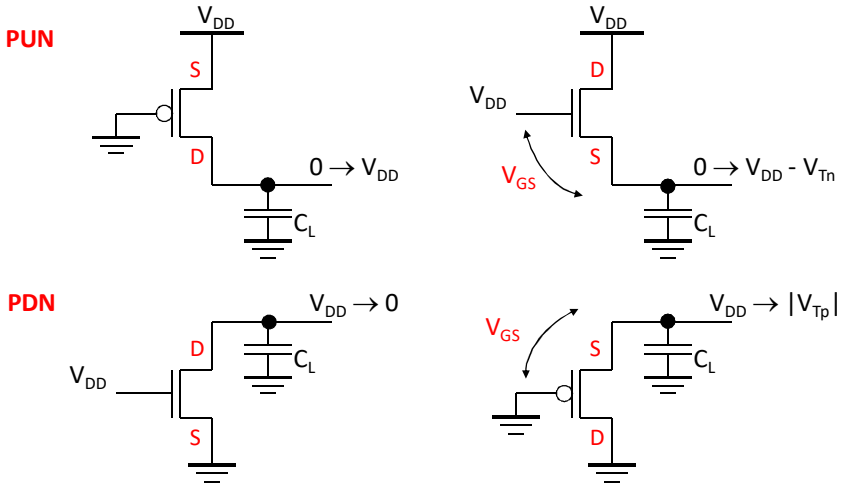
Good/bad pull-up/down (remember?)



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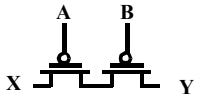
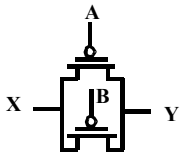
How to construct PUN?

- PMOS in serial/parallel connection
- PMOS switch closes when input is low



$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$



$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

- PMOS pass strong 1 but weak 0

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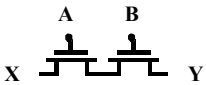
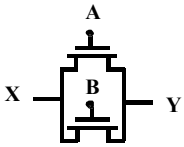
How to construct PDN?

- NMOS in serial/parallel connection
- NMOS switch closes when input is high



$Y = X$ if A and B



$Y = X$ if A OR B

- NMOS pass strong 0 but weak 1

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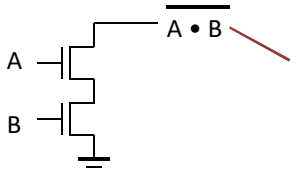
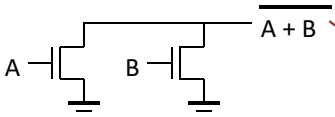
How to construct PDN? (cont'd)

- NMOS devices in series implement NAND



both inputs 1
then output 0
= conducting

- NMOS in parallel implement NOR



at least one input 1
then output 0
= conducting

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PUN and PDN are dual networks

- De Morgan's laws (theorem)

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Augustus de Morgan
1806-1871

- Implications:
  - parallel connection in PUN
    → series connection in PDN
  - and vice versa!

important for the synthesis of logic gates

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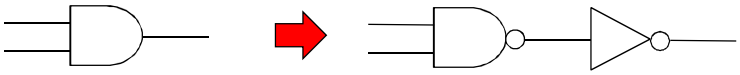
Image taken from: https://en.wikipedia.org/wiki/Augustus_De_Morgan

Complementary gate is inverting

- CMOS is inverting: NAND, NOR, INV



AND = NAND + INV

- Number of transistors to implement N-input logic gate is at least 2N!

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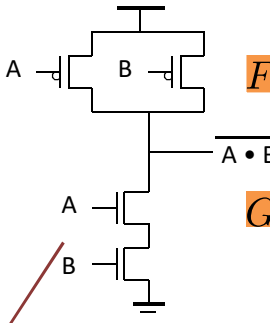
CMOS NAND gate

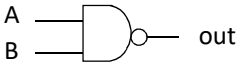


$F = \overline{A} + \overline{B}$

$G = \overline{A \cdot B}$

A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

only if both inputs are 1 both NMOS are conducting → 0



Remember the symbol: looks like a D and the letter D can be found in NAND

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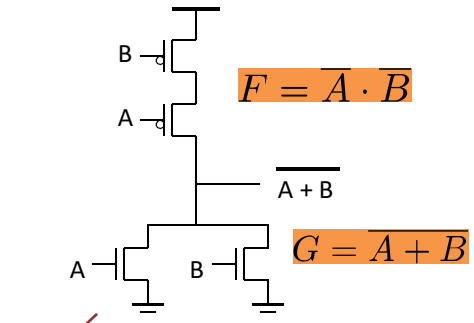
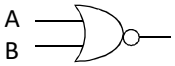
CMOS NOR gate



$$F = \overline{A} \cdot \overline{B}$$

$$G = \overline{A + B}$$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0



only one of inputs is 1 then output 0

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