ECE4740: Digital VLSI Design

Lecture 9: Wire models

Should I even care?

Wire basics

Interconnect parasitics

- Wiring in today's circuits will
  - increase the propagation delay
  - have an impact on power consumption
  - cause extra noise/interference (reliability)
  - affect the density of your chip
- Classes of parasitic effects
  - Capacitive → cross talk
  - Resistive → IR drop
  - Inductive → inductive peaking

less important...

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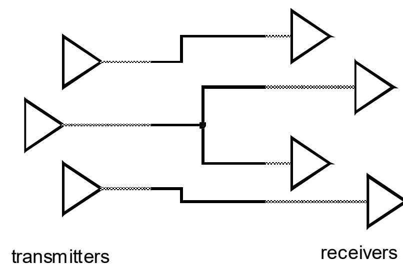
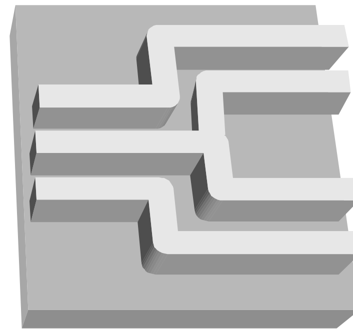
Example



schematic view



physical view

Images taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

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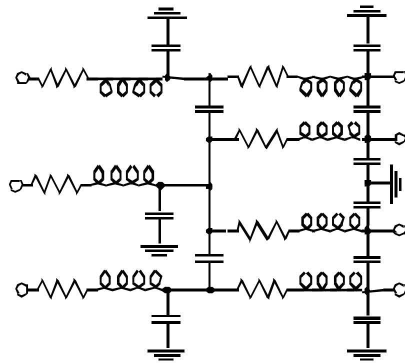
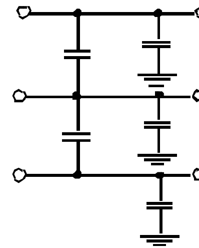
Example (cont'd)





"all-inclusive" model capacitance model

Images taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

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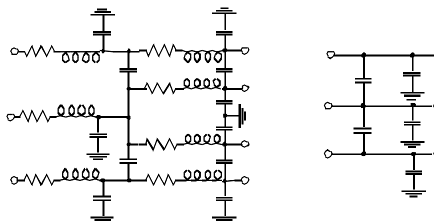
Wire model: simplifications

- Inductive effects can be ignored if resistance is large enough or transients are slow
- Short wires: resistivity can be ignored
- If separation between wires is large, inter-wire capacitance can be ignored



Images taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

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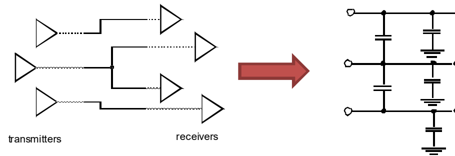
Wire models

- "All-inclusive" models too complicated for manual analysis; we need simpler models:
  - Lumped C
  - Lumped RC
  - Distributed RC
  - Lumped RL
  - Distributed RL
  - Distributed LC
  - Transmission lines
  - Lossy TL



when to use which model?

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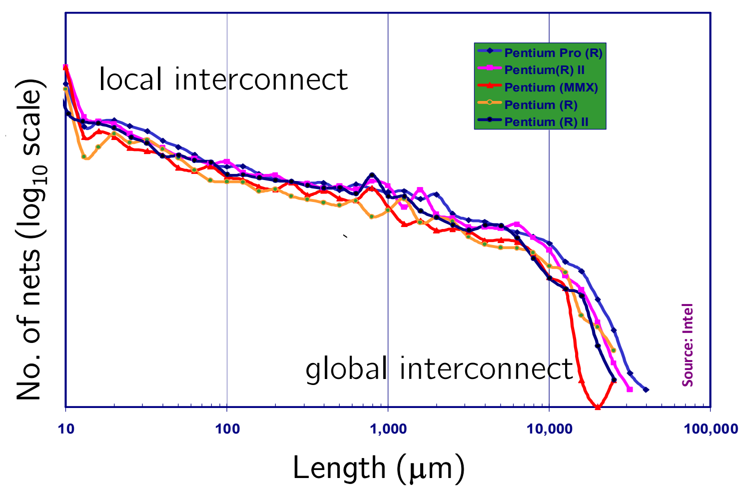
Length distribution



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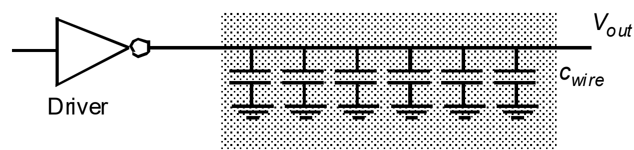
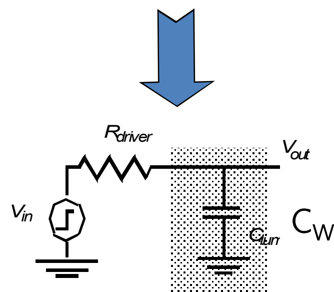
The basic model

Wire capacitance

Lumped capacitance



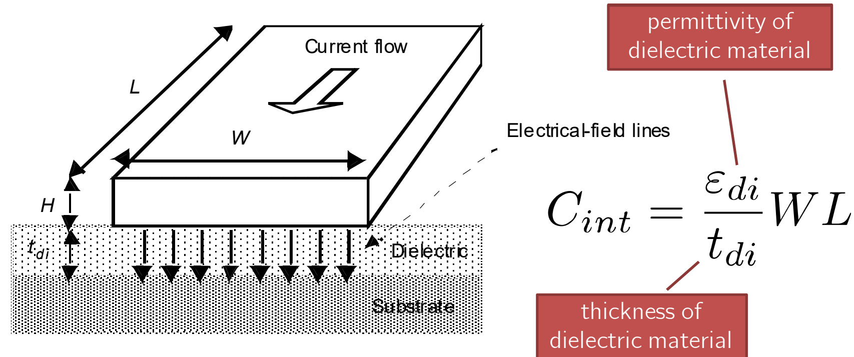


- Valid if
  - short wires
  - low resistivity
  - low frequency

Images taken from: ECE424 – Fall 2014 Introduction to VLSI Design, by Emre Yengel

Parallel plate model

- Width of wire much larger than thickness of insulating material → area capacitance



permittivity of dielectric material

$$C_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

thickness of dielectric material

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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Permittivity of dielectrics

$$\varepsilon_{di} = \varepsilon_0 \varepsilon_r$$

relative permittivity

free-space permittivity

$$\varepsilon_0 \approx 8.854 \cdot 10^{-12} \mathrm{F/m}$$

Material	Relative Permittivity ε_r
Free space	1
Aerogels	1.5
Low-K SiO_2 (porous)	1.5 – 2
Polyimides (organic)	3 – 4
Silicon Dioxide (SiO_2)	3.9 – 4.5
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7 - 9
Alumina (package, Al_2O_3)	9.5
Silicon	11.7

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Height of wire does matter

- Previous model is too simplistic
- Current designs:
  - cross section WxH as large as possible
  - denser wiring led to increase in H/W ratio (>1)
- Parallel plate model not accurate anymore

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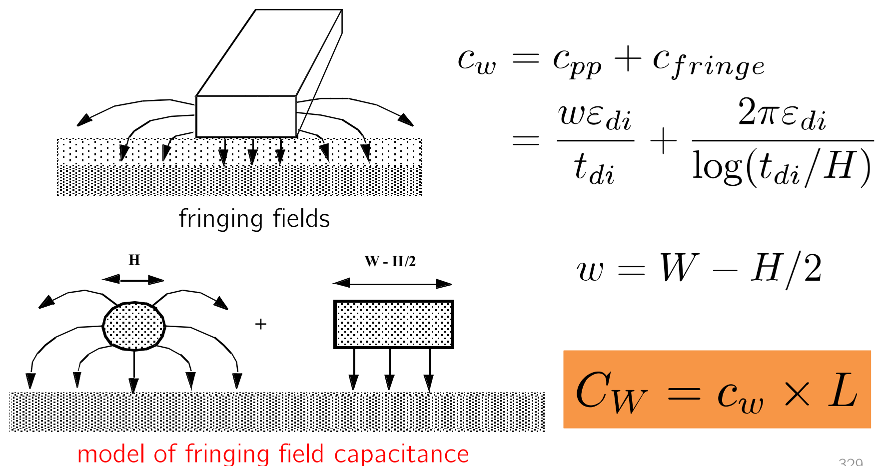
Fringing capacitance

- Capacitance between wire sides & substrate



$$c_w = c_{pp} + c_{fringe}$$

$$= \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

$$w = W - H/2$$

$$C_W = c_w \times L$$

model of fringing field capacitance

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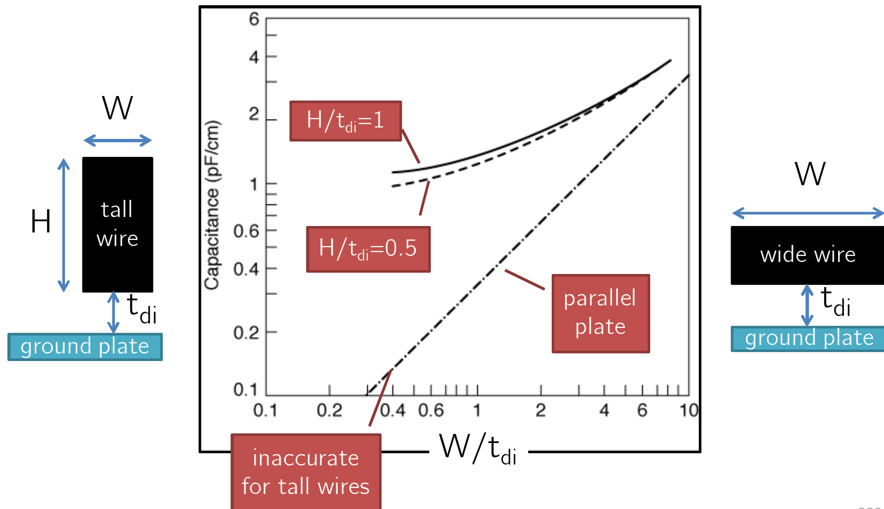
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Fringing capacitance (cont'd)



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Example: Capacitances in 250nm

bottom plate of capacitor

top plate of capacitor

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

area capacitance aF/μm^2

fringe capacitance aF/μm

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Inter-wire capacitance

- Wires are coupled to GND and to neighboring wires (same or different layer)
- Floating capacitors cause cross-talk

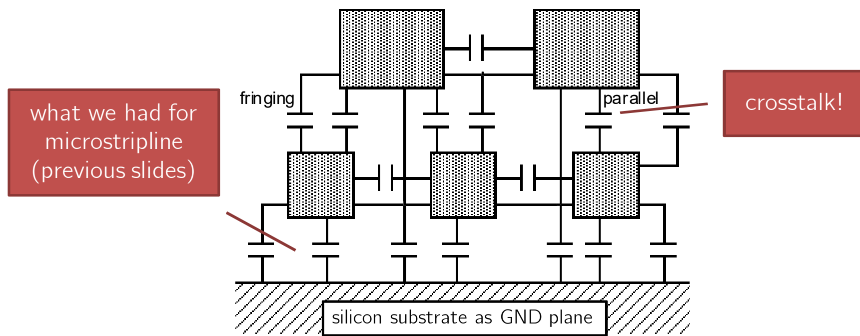

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

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Inter-wire capacitance

- Growing problem
  - multilayer structures
  - decreasing feature sizes

wires are getting closer and closer

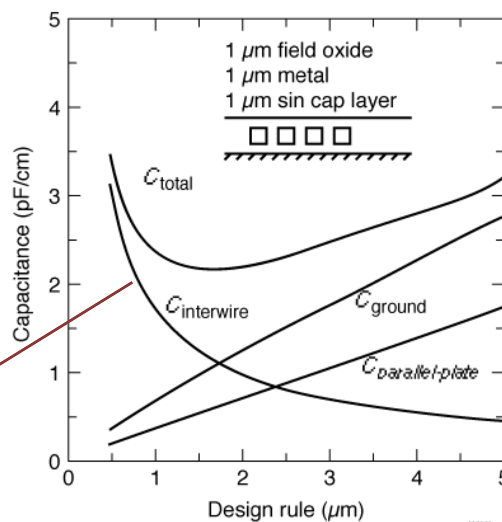

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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Example: Capacitances in 250nm

- Inter-wire capacitances (minimum spacing)

Layer	Poly	Al1	Al2	Al3	Al4	Al5
Capacitance [aF/µm]	40	95	85	85	85	115

- Use top layers for
  - supply: large caps. are good = tiny "batteries"
  - if used for signals, separate more than minimum
  - careful: vias are going to add resistance!

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Dealing with capacitance

- Use low capacitance (low-k) dielectrics (=insulators) such as polyamide or even air
  - must be robust (thermal and mechanical stress)
  - must be compatible with interconnect
- Copper interconnect allows wires to be thinner without increasing their resistance
- Silicon on insulator (SOI) to reduce junction capacitance

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Important for not-so-short wires

Wire resistance

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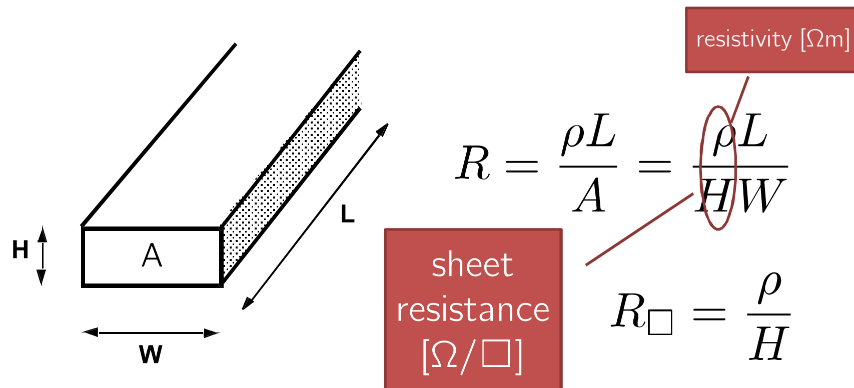
Basics and definitions

- Resistance proportional to length L
- Inversely proportional to cross section A



$$R = \frac{\rho L}{A} = \frac{\rho L}{HW}$$

$$R_{\square} = \frac{\rho}{H}$$

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Resistivity of common conductors

- ρ at 20°C

Material	Resistivity (Ωm)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Copper: more popular recently (low resistivity)

Aluminum: low cost and good in manufacturing

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Fun fact: AudioQuest K2 Cable

- 2.44m audio speaker cable
- Silver connectors and cables
- "Optimized for full range"
- Price: 1 used from $13,099.00

471 of 488 people found the following review helpful

★☆☆☆☆ **Thanks a lot.**

By Daniel A. Garcia on December 30, 2010

My cats chewed on this cable and now they can both speak.

12 Comments | Was this review helpful to you? Yes No

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Sheet resistance in 250nm

Material	Sheet resistance (Ω/□)
n- or p-well diffusion	1000-1500
n+, p+ diffusion	50-150
n+, p+ polysilicon	150-200
aluminum (Al)	0.05-0.1

only good for local interconnect

$$R_{\square} = \frac{\rho}{H}$$

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Dealing with wire resistance

- Selective technology scaling (less scaling of wire thickness)
- Use better interconnect materials
  - Use copper in metal layers and silicides close to silicon (active and poly gate)
- More interconnect layers
  - Reduces average wire length

remember: contacts (vias) add resistance (contact resistance)

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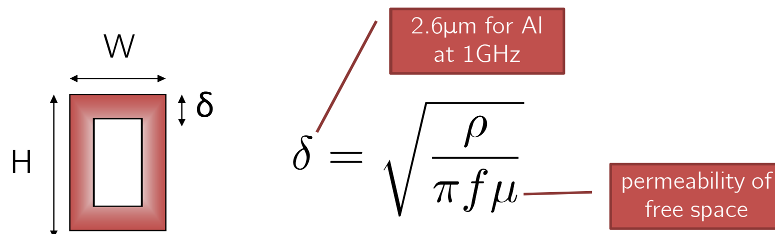
Skin effect

- For high frequencies *f*, currents tend to flow mostly on surface of conductor
- Skin depth δ: depth where current is $e^{-1} \approx 0.368$ times less than nominal



$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

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Skin effect (cont'd)

- Effective area lower → resistance increases!
- For $f > f_s$, the resistance gets

resistance per unit length

$$r(f) = \frac{\sqrt{\pi f \mu \rho}}{2(H+W)}$$

frequency where skin depth is equal to half the largest dimension of the conductor

$$f_s = \frac{4\rho}{\pi\mu(\max\{W,H\})^2}$$

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Really?

Wire inductance

Should we even care?

- Inductance plays a role in multi GHz range
- Useful relation:

$$l \times c = \varepsilon\mu$$

inductance per unit length | capacitance per unit length | permittivity | permeability

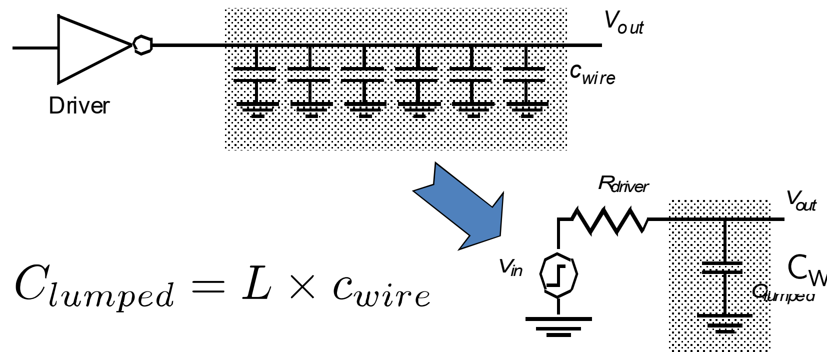
- The larger the capacitance, the smaller the inductance, and vice versa!
- Depends on the wire thickness

Useful for back-of-the-envelope calculations

Lumped wire model

Lumped wire model revisited

- Ignore inductive effects and assume small resistive component

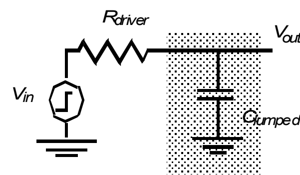


$$C_{lumped} = L \times c_{wire}$$

Images taken from: ECE424 – Fall 2014 Introduction to VLSI Design, by Emre Yengel

Example: long wire

- Source resistance: 10kΩ
- Al1 wire: 10cm long, 1μm wide: 11pF
- Compute transient response time (50% point reached; V_{in} goes from GND to VDD)



$$t = \ln(2)\tau \approx 0.69\tau$$

what is τ?

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Image taken from: ECE424 – Fall 2014 Introduction to VLSI Design, by Emre Yengel

Lumped RC model

- RC tree
- Properties:
  - Single input s
  - Capacitors between node and ground
  - Network contains no resistive loops

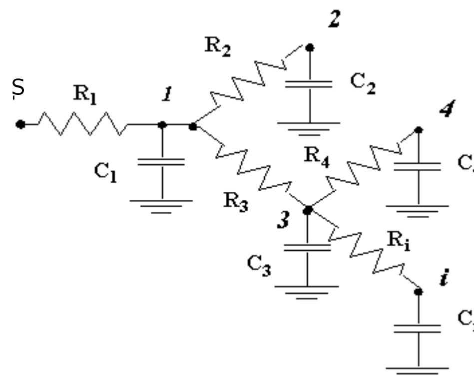

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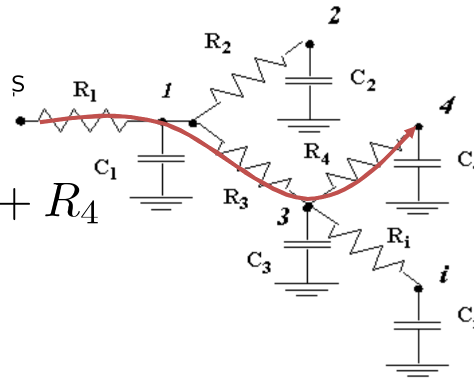
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

(Shared) path resistance (R_{ik}) R_{ii}

- Resistance between source s and node 4: R_{44}



$$R_{44} = R_1 + R_3 + R_4$$

- Shared path resistance R_{ik}

$$R_{ik} = \left\{ \sum R_j : j \in \{\text{path}(s \to i) \cap \text{path}(s \to k)\} \right\}$$

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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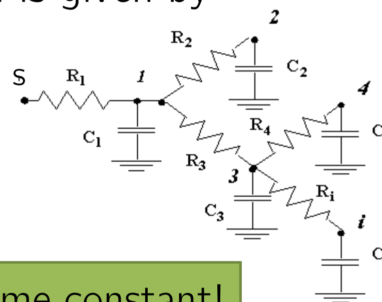
Elmore delay

- Assume all nodes are discharged to GND
- Step input applied at node s at t=0
- Elmore delay at node i is given by

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$



equivalent to first-order time constant!

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

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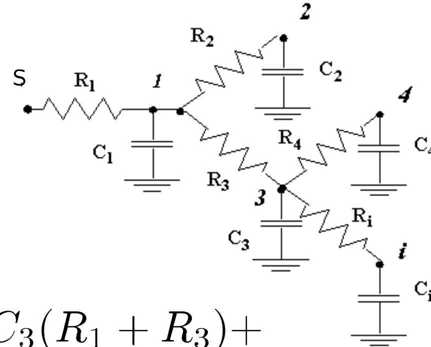
Example: Elmore delay

- Elmore delay τ_{Di} for node i?

sum over every cap.

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$



$$\tau_{Di} = C_1 R_1 + C_2 R_1 + C_3(R_1 + R_3) + C_4(R_1 + R_3) + C_i(R_1 + R_3 + R_i)$$

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Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Resistive capacitive wire

- Partition wire of length L in N segments
  - Resistance of segment rL/N (with R=rL)
  - Capacitance of segment cL/N (with C=cL)
- Use Elmore delay formula

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc)$$

$$\tau_{DN} = RC\frac{N+1}{2N} \rightarrow \frac{RC}{2} = \frac{rcL^2}{2}$$

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Resistive capacitive wire (cont'd)

- Implications of

$$\tau_{DN} = RC\frac{N+1}{2N} \rightarrow \frac{RC}{2} = \frac{rcL^2}{2}$$

- Doubling wire length L quadruples delay
- Lumped RC model overestimates the delay by a factor of 2 (pessimistic estimate)

remember: it is only a 1st order approximation

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