ECE4740: Digital VLSI Design

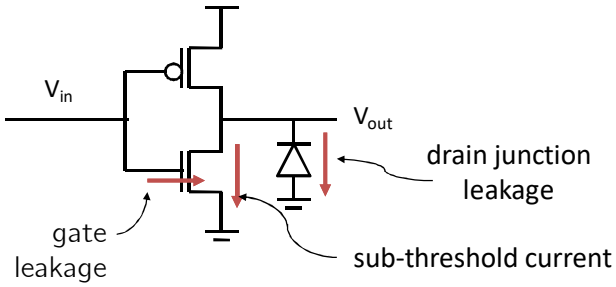
Lecture 8: Static power consumption and CMOS fabrication

Increasingly important!

Static power consumption

Causes: leakage currents*

- Static power consumption: $P_{stat} = I_{stat} V_{DD}$

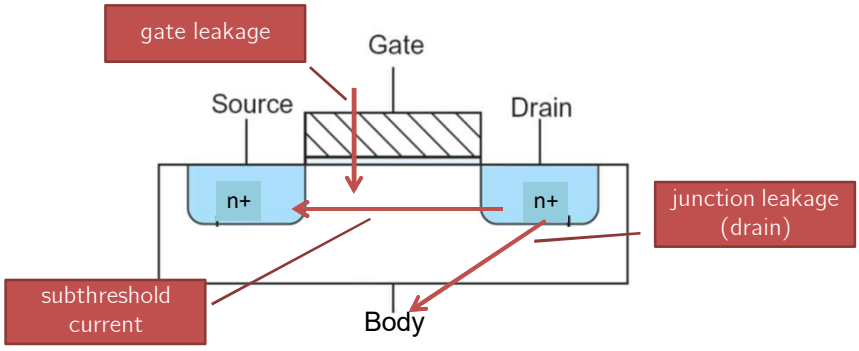


*result of simple power formula P=V*I

253

Causes: leakage currents (cont'd)

- Static power consumption: $P_{stat} = I_{stat} V_{DD}$



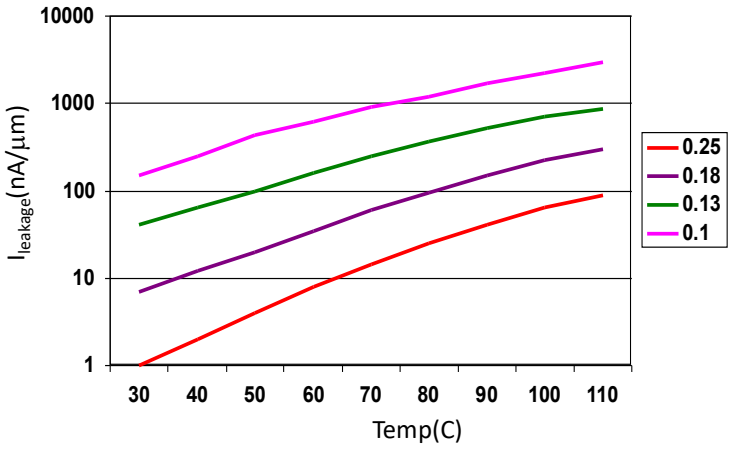
254

Leakage and temperature

- All three leakage currents increase exponentially with temperature
  - heat removal is crucial
  - whenever you write a paper/report with power measurement results, state the temperature!
- (Current doubles for every ~9K)

255

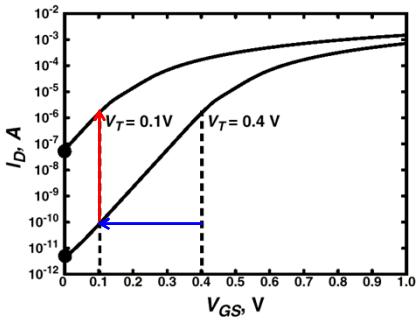
Leakage and temperature (cont'd)



From De, 1999

256

Subtreshold leakage is dominating



- Remember: $I_{DS}>0$ even if $V_{GS}<V_T$
- Reducing V_T increases I_{DS}
- Trend to lower V_{DD} demands reduction of V_T

we are in trouble!

257

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Putting the pieces together

Summary: power consumption

258

Three sources of power consumption

$P_{dyn} \sim V_{DD}^2 C_L f_{0\to1}$
90% today and increasing

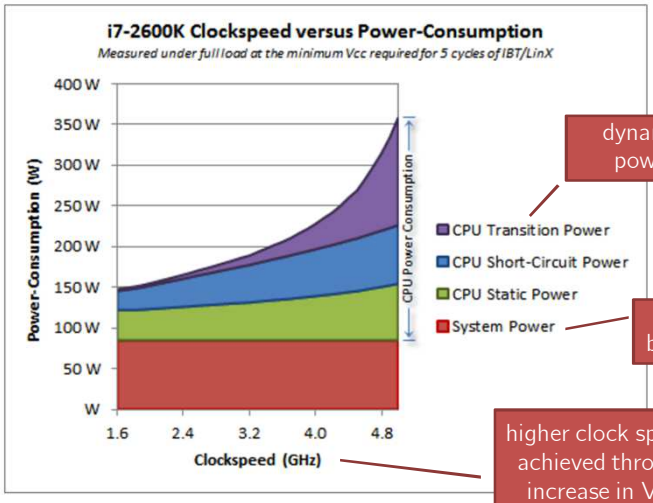
$P_{stat} = V_{DD} I_{stat}$
5% today and increasing

$$P = P_{dyn} + P_{dp} + P_{stat}$$

$P_{dp} \approx \frac{\beta}{12}(V_{DD} - 2V_T)^2 t_r f_{0\to1}$
5% today and decreasing

259

An example: Intel i7-2600K



http://forums.anandtech.com/showthread.php?t=2195927

260

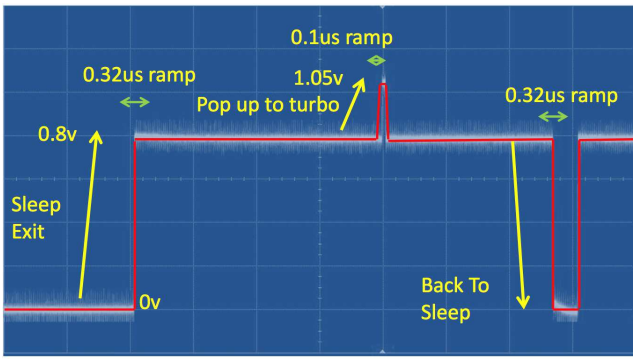
Principles for power reduction

- Reduce supply voltage (main goal)
  - quadratic impact on power
  - problematic for subthreshold currents
- Reduce switching activity and/or #of gates required for a given task → universal!
  - requires new algorithms, suitable architectures, and VLSI circuit tricks → my research area
- Reduce physical capacitances (use tools)
  - device sizing, good place & route of gates
- Reduce temperature (packaging, heat removal)

261

Example: Power gating (ISSCC '14)

- Intel Haswell (22nm) memory controller leakage currents reduced by 100x with new power gate



[Intel, ISSCC 2014]

262

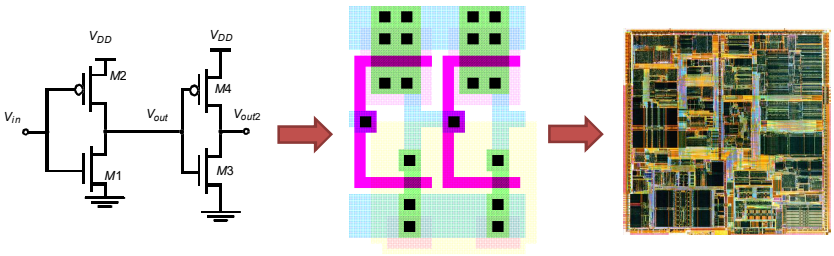
Just a short overview

Manufacturing process

263

CMOS fabrication

- Layout = mask design



schematic view circuit layout fabricated chip

264

n-well CMOS fabrication

- Start with blank wafer and build integrated circuit from the bottom up
  - cut from a single-crystalline lightly doped wafer
  - diameter 10cm-30cm, 0.4mm-1mm thick

growing the silicon ingot

wafer cut

265

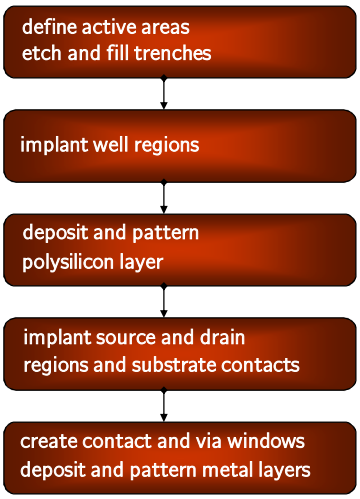
Image taken from: http://www.tomshardware.com/reviews/semiconductor-production-101,1590-3.html

Wafer doping

- p-type silicon: impurities (acceptors; Boron) introduced during crystal growth
- Boron p-type doping concentrations of $10^{15}/cm^3$ to $10^{16}/cm^3$ gives resistivity of about $25\Omega cm^2$ to $2\Omega cm^2$
- Design metric: defect density
  - High defect density leads to larger fraction of non-functional circuits (low yield)

266

CMOS process overview

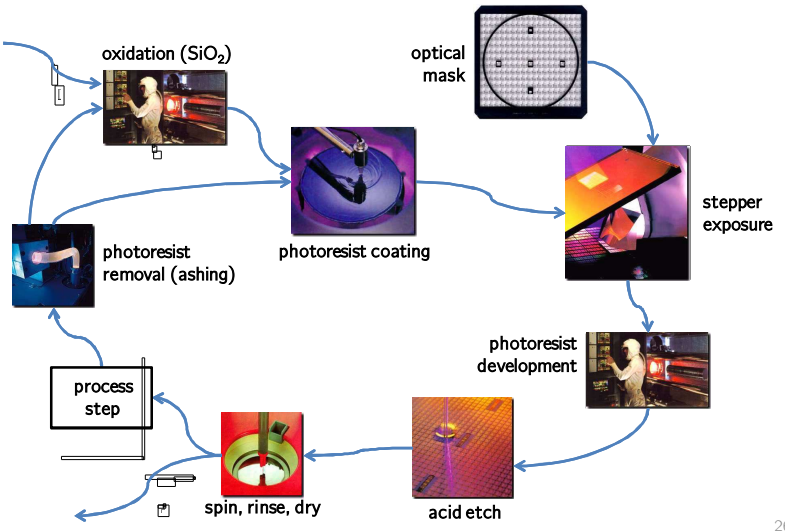


- One full photolithography sequence per layer (mask)

5 – metal 2
4 – metal 1
3 – polysilicon
2 – source/drain diffusion
1 – wells (active areas)

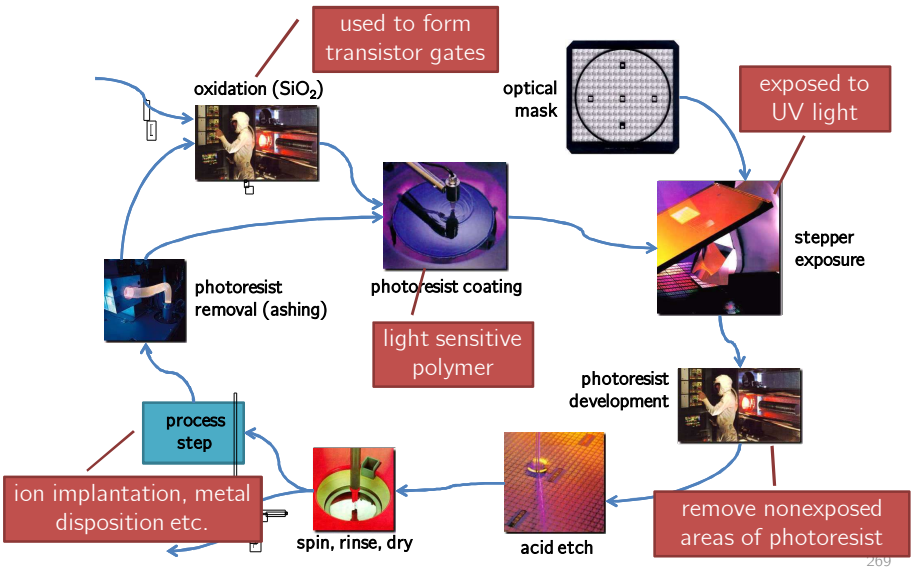
267

Photolithographic process



268

Photolithographic process



269

The steps in detail

Example: CMOS inverter

270

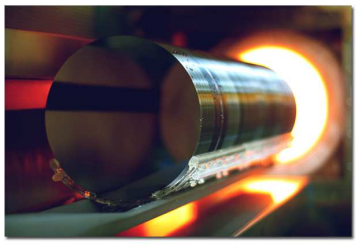
Silicon (p-type) base material

- Start with Boron doped wafer
- Forms the p-type substrate (base)

271

Oxidation step

- Silicon dioxide SiO_2 layer is grown over wafer surface (e.g., for transistor gate)
  - about 1μm tdhick
  - 900°C-1200°C with mixture of H_2O and O_2 in oxidation furnace



272

Oxidation step (cont'd)

- Protects surface
- Acts as barrier to dopants during subsequent processing steps
- Provides insulating substrate onto which other layers may be deposited & patterned

273

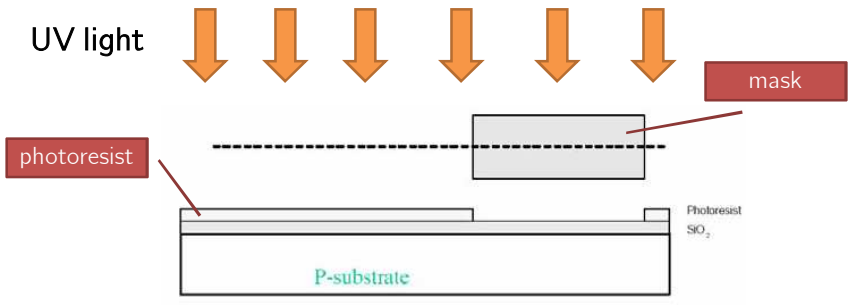
Photoresist (PR) patterning

- Photoresist (polymer) deposited onto surface of wafer
  - approximately 1μm thick
  - spun for even distribution

274

Lithography: define PR patterns

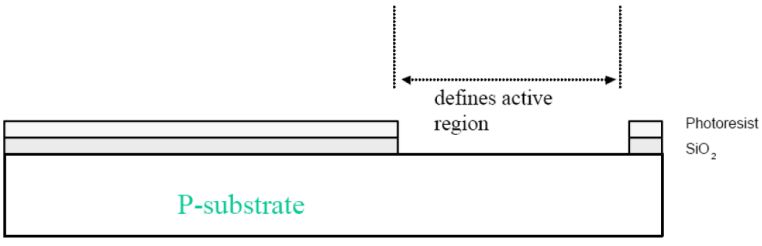
- Expose photoresist through n-well mask
- Strip off unexposed photoresist



275

Etching

- Exposed oxide areas are etched away with hydrofluoric acid (HF)
- Only etches regions oxide where resist has been exposed



276

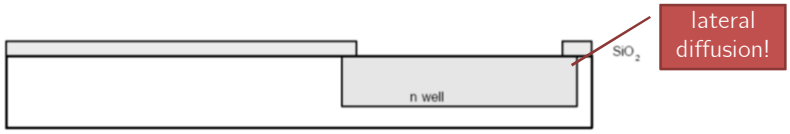
Spin, rinse, and dry

- Strip off/remove remaining photoresist
- Must be ultra-clean to avoid contamination of subsequent steps

277

Form n-well

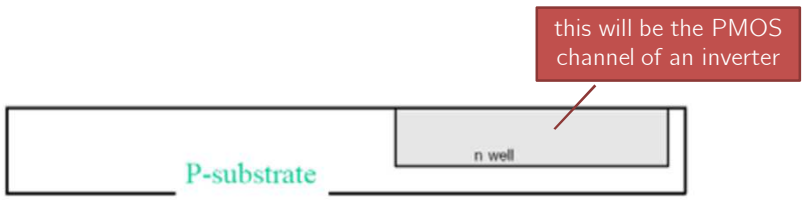
- Diffusion or ion implantation to form n-well
- Diffusion
  - place wafer in furnace with arsenic gas
  - heat until As (donors) diffuse into exposed Si
- Ion implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2 only enter exposed Si



278

Strip oxide layer

- Strip off remaining oxide using HF acid
- Back to bare wafer with n-well
- Subsequent process steps are similar



279

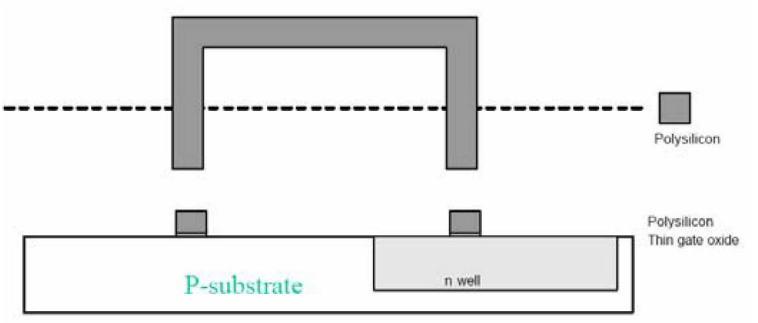
Deposit polysilicon gate

- Deposit very thin layer of gate oxide
  - around 2nm (only 6-7 atomic layers!)
- Heavily doped polysilicon deposited by chemical vapor deposition (CVP)
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor

280

Polisilicon gate patterning

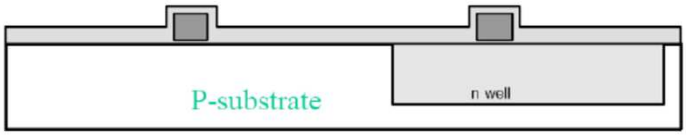
- Use same lithography process to pattern polysilicon



281

Form n-type diffusion

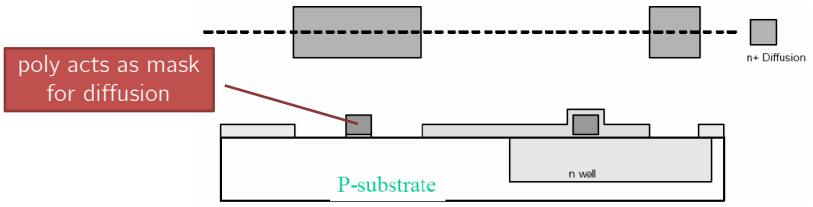
- NMOS source, drain, and n-well contact
  - Use oxide and masking to expose where n^+ dopants should be diffused or implanted
- First deposit oxide to entire area



282

n-type diffusion formation

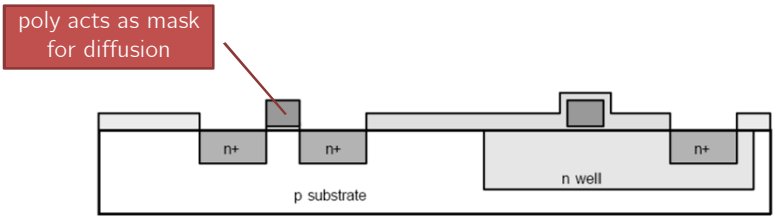
- Pattern oxide and form n+ regions
  - Self-aligned process where gate blocks diffusion
  - Polysilicon better than metal as it does not melt or expand during later processing



283

N-type diffusion doping

- Diffusion was used around 1985
- Nowadays: ion implantation



284

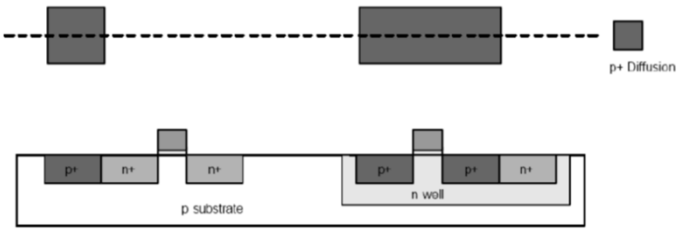
Etching again

- Strip off oxide to complete patterning step

285

P-type diffusion formation

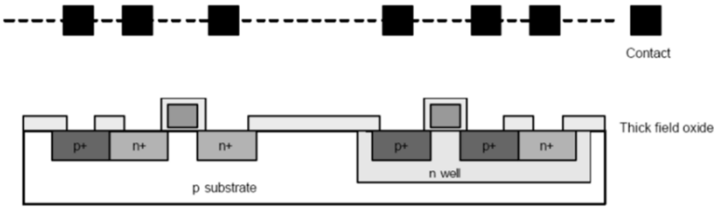
- Similar steps for p^+ diffusion regions for PMOS source, drain, and substrate



286

Contacts

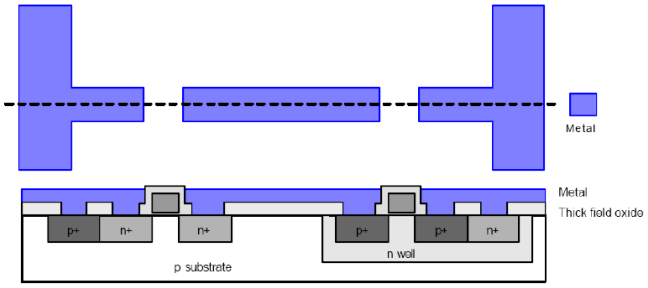
- Now, wires needed to contact devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



287

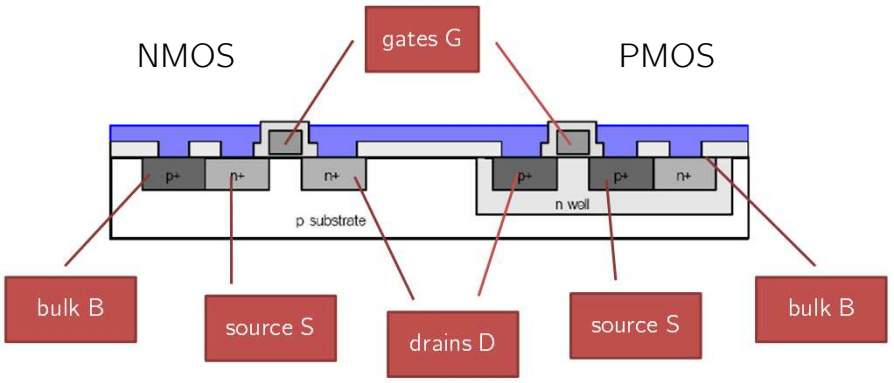
Metallization

- Sputter aluminum or tungsten over wafer
  - Silicides used to decrease contact resistance
  - Pattern to remove excess metal, leaving wires



288

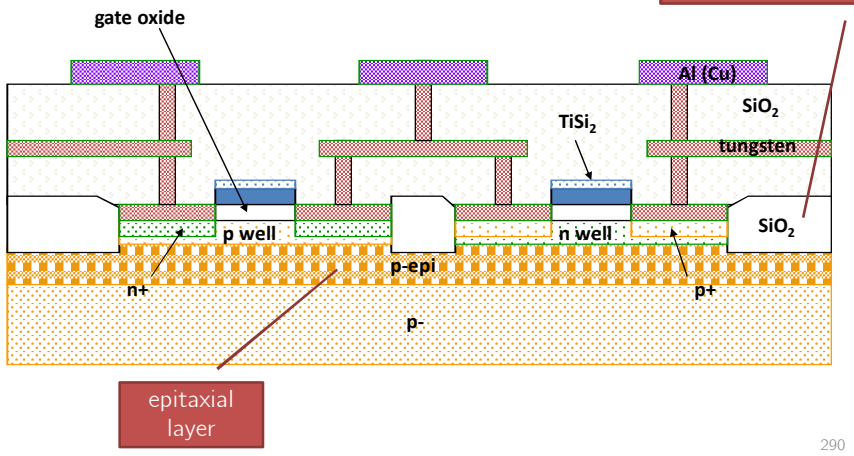
Et voilà: inverter



289

Modern CMOS process

- Dual-well trench-isolated CMOS

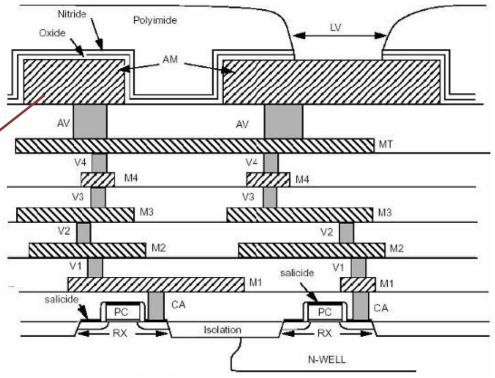


290

Connecting gates: metallization

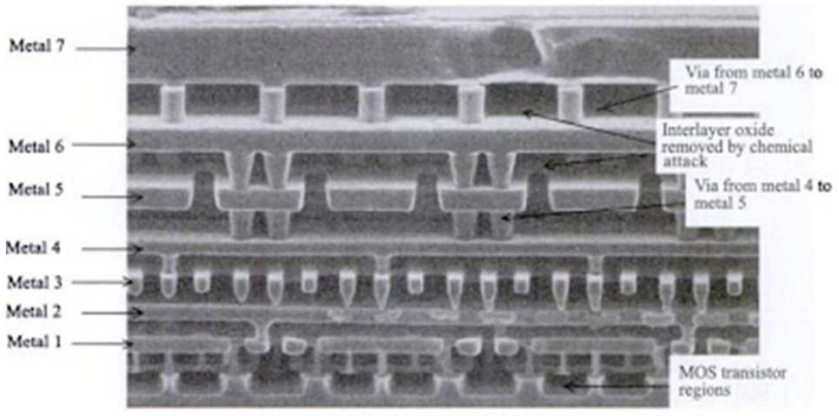
- Modern processes offer multiple metal layers to connect gates

wire thickness usually increases for higher layers



291

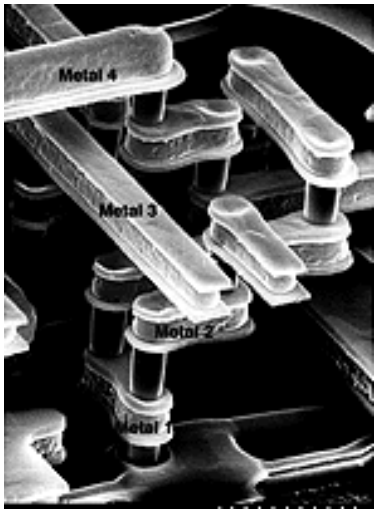
Modern chips have 7+ metal layers



Cross-section of a 0.12 µm technology (*Courtesy:* Fujitsu)

292

Modern interconnect



- Each metal layer has sandwich structure
- Via filled by different material
- Feature sizes increase for higher layers
- Today: can easily be 8-11 metal layers

A Scanning Electron Microscopy (SEM) with SiO_2 removed by HF wet etch

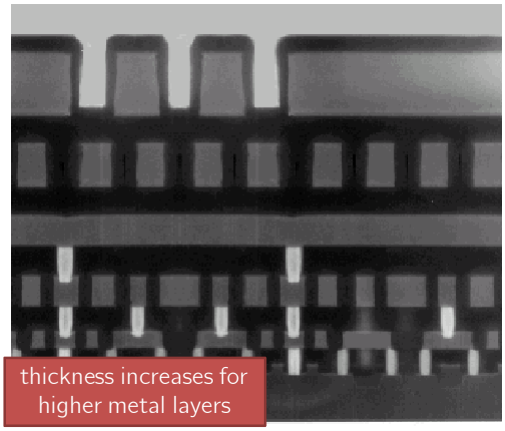
293

Example: Intel 250nm CMOS

- 5 metal layers, Ti/Al, Cu/Ti/TiN, SiO_2 dielectric

LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

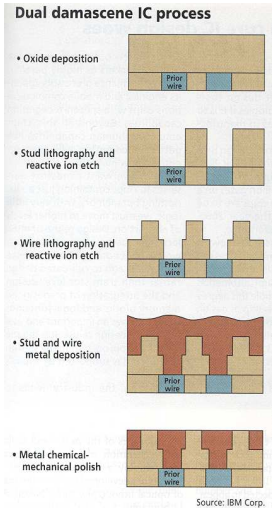
Layer pitch, thickness and aspect ratio

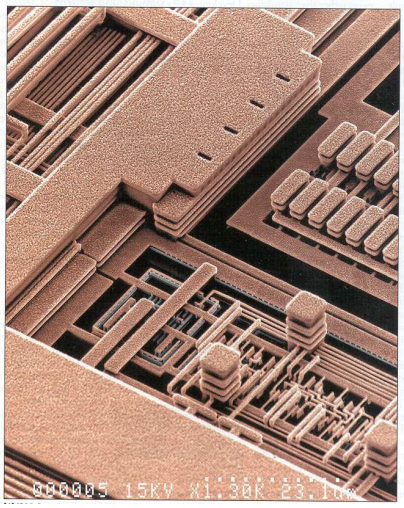


thickness increases for higher metal layers

294

Advanced metallization





295

Image taken from: Foundations for Microstrip Circuit Design by T. Edwards

Interconnect parasitics

- Wiring in today's circuits will
  - increase the propagation delay
  - have an impact on power consumption
  - cause extra noise/interference (reliability)
  - affect the density of your chip
- Classes of parasitics
  - Capacitive
  - Resistive
  - Inductive

NEXT LECTURE!

less important...

cross talk

IR drop

inductive peaking

296

Often overlooked but very important

Packaging

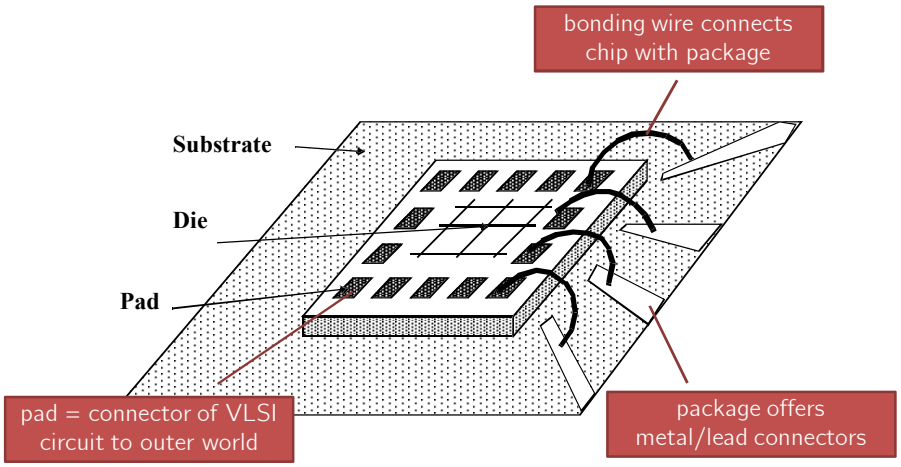
297

Packaging requirements

- Electrical: low parasitics (C and L)
- Mechanical: reliable and robust (shock etc.)
- Thermal: efficient heat removal
- Economical: cheap
- Recent: Restriction of Hazardous Substances Directive (RoHS)
  - no (or little) use of lead, mercury, cadmium etc.

298

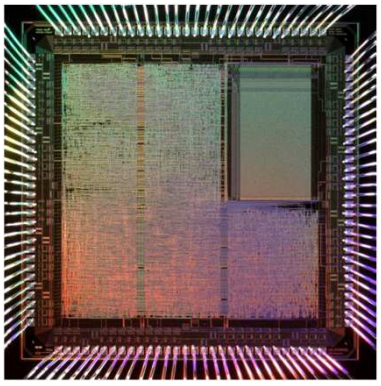
Wire bonding

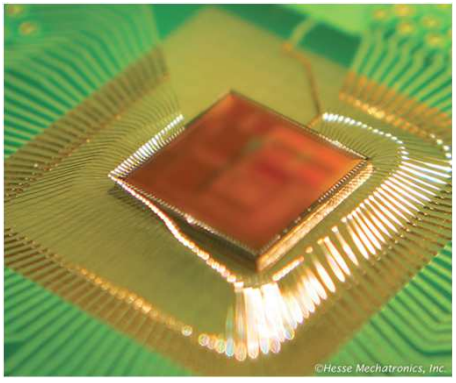


299

Image taken from: http://cnfolio.com/ENG710S2SemiconductorFabrication

Wire bonding (cont'd)

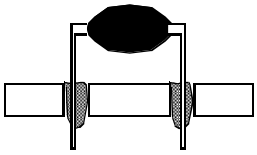




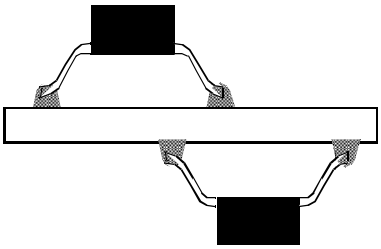
300

Image taken from: https://www.wirebonddemo.com/video/chip_on_board

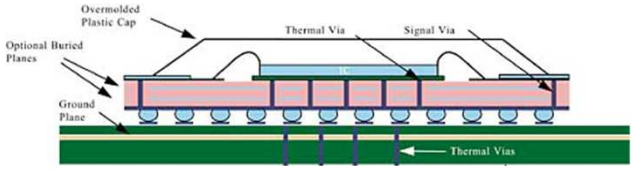
Package to board interconnect



through-hole mounting



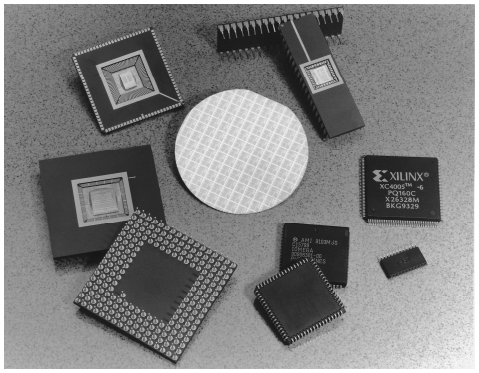
surface mounting



surface mounting: ball grid array (BGA)

Image taken from: https://www.electronics-cooling.com/2002/02/the-many-flavors-of-ball-grid-array-packages/# 301

Package types



- Chose one
  - with sufficient number of pins
  - with suitable thermal properties
  - that connects well to surroundings
  - that is available…

302

Image Taken From: EE141 Design Rules, Berkeley EECS

You really want to be sure that your chip works!

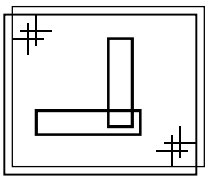
Design rules

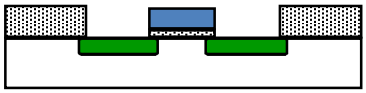
Design rules

- Interface between VLSI designer and process engineer/IC manufacturer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
- Rules ensure that design works even with minor fabrication errors (process errors, variations etc.)
- Set of rules includes
  - set of layers
  - intra-layer: relations between objects in same layer
  - inter-layer: relations between objects on different layers

Why do we need rules?

- Tolerate fabrication errors
  - Mask alignment
  - Dust
  - Process parameters (lateral diffusion)
  - Rough surfaces

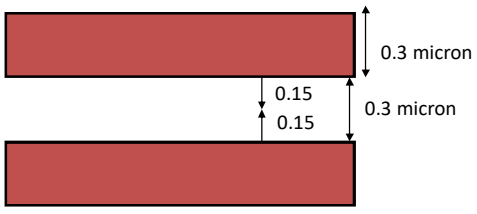




305

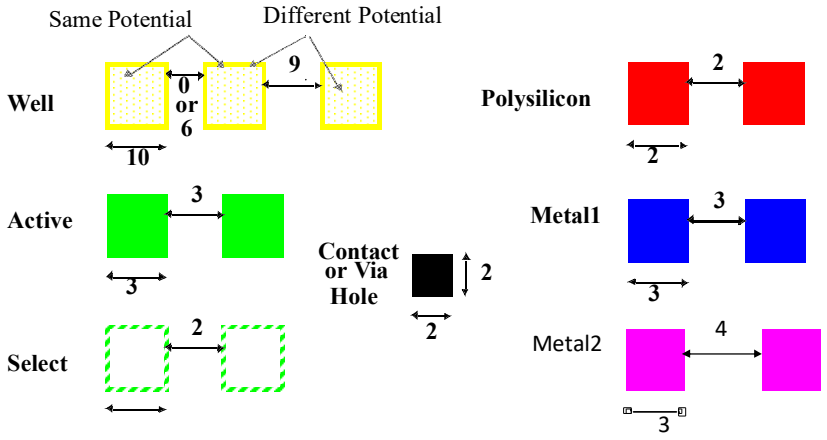
Intra layer design rules

- Minimum dimensions (widths, lengths)
  - determined by resolution of photolithography
- Minimum spaces between objects that are unrelated (avoid shorts)



306

Intra layer design rules (cont'd)

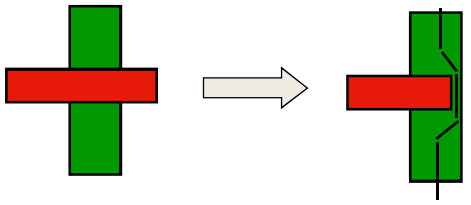


307

Image taken from: EE141 Design Rules, Berkeley EECS

Inter layer design rules

- Avoid transistor to form by overlap of active and poly layers, e.g.,

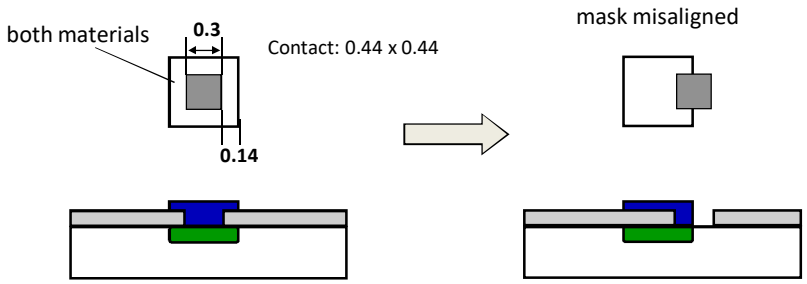


catastrophic error

308

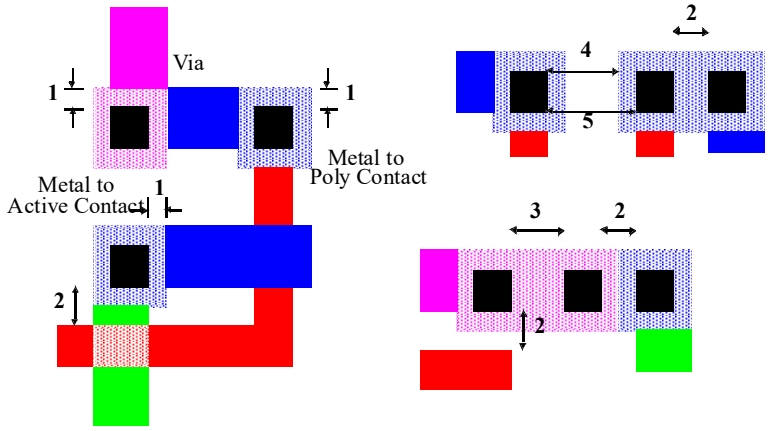
Inter-layer design rules (cont'd)

- Contact and via rules



309

Vias and contacts



310

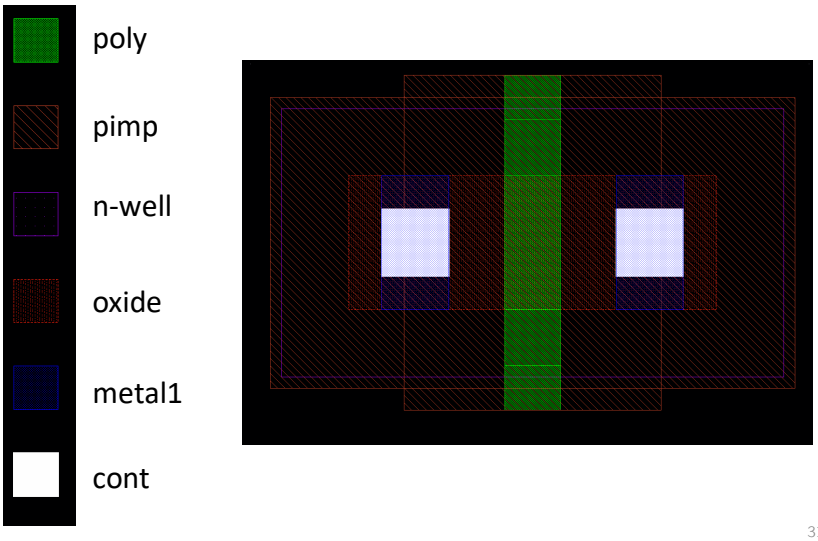
Image taken from: EE141 Design Rules, Berkeley EECS

Cadence stuff

Good to know

311

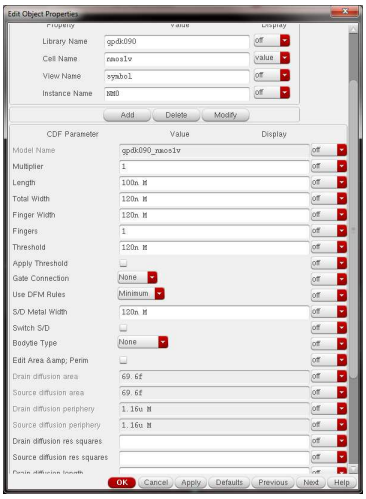
Layer color is not fundamental!



312

NMOS settings (Cadence)

- Multiplier: number of parallel devices
- Fingers: number of poly gate fingers used in layout
- Threshold: automatic fingers (must apply threshold)

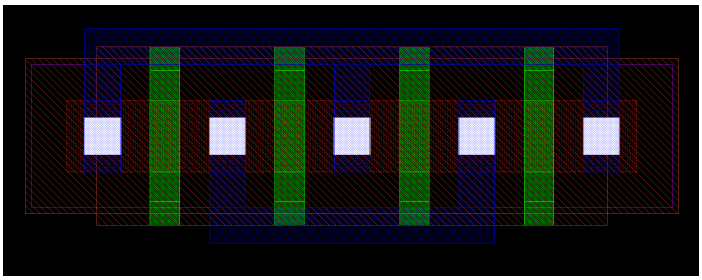


313

Fingers

check out Layout KungFU on blackboard

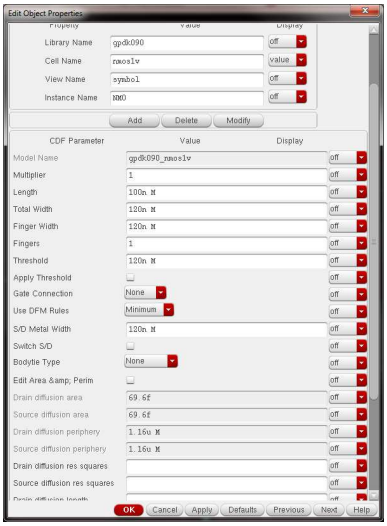
- Lower poly resistance
- Like S/D sharing between multiple FETs
- Lower diffusion capacitance
- Can reduce layout area



314

NMOS settings (cont'd)

- Gate connection: automatic connection of fingers
- S/D connection: automatic connection of sources and/or drains on multifinger devices
- Switch S/D: source is defined as left-most diffusion by default



315