# ECE4740: Digital VLSI Design

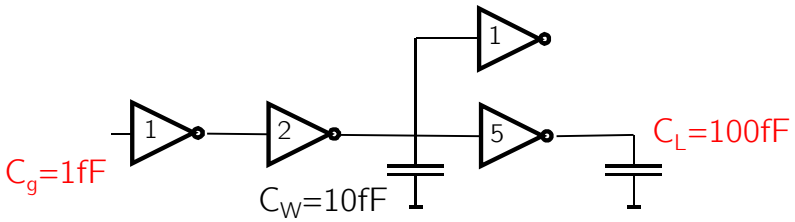
Lecture 7: Power consumption



Practice helps a lot

## Sizing examples

# Your turn: compute the p-delay



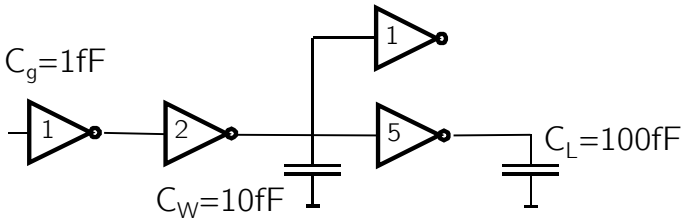

$$t_{p,i} = t_{p0}\left(1 + \frac{C_{ext,i+1}}{\gamma C_{g,i}}\right) \qquad \gamma = 1 \qquad t_{p0} = 3ps$$

226

# Solution

$$t_{p1} = t_{p0}\left(1 + \frac{2C_g}{C_g}\right) = t_{p0}3$$

$$t_{p3} = t_{p0}\left(1 + \frac{100\text{fF}}{5C_g}\right) = t_{p0}21$$




$$t_{p2} = t_{p0}\left(1 + \frac{C_g + 5C_g + 10\text{fF}}{2C_g}\right) = t_{p0}9$$

$$t_p = t_{p0}(3 + 9 + 21) = t_{p0}33 = 99\text{ps}$$

$$\gamma = 1$$
$$t_{p0} = 3ps$$

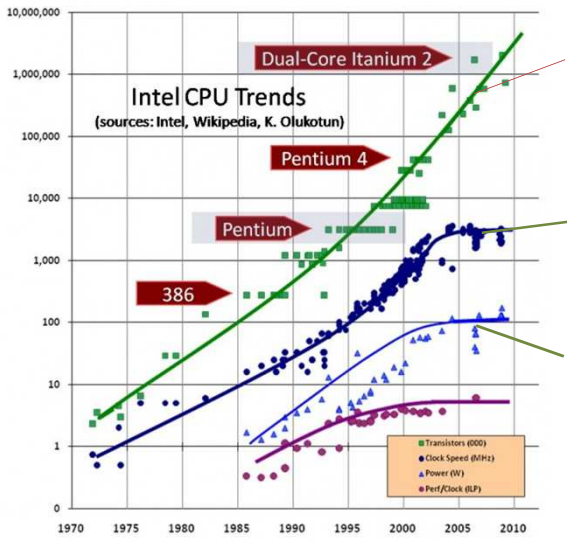
227

Very important

# Energy and power consumption

228

# Trends in power consumption




circuit complexity increases

clock frequency saturates

power consumption saturates

229

# Main sources of power consumption

- Dynamic power consumption
  - Charging and discharging capacitors
  - Short circuit currents (short between supply rails during switching)

dominating in most applications

- Static power consumption
  - Leakage (leaking diodes and transistors)

increasing with shrinking transistors!

already a concern for ultra low-power applications (e.g., watches, hearing aid devices, sensors)

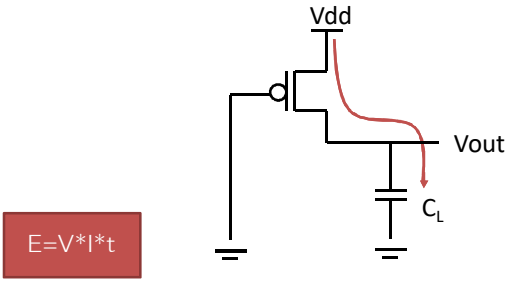
230

Still dominating in most designs

# Dynamic power consumption

231

# Energy consumption 1→0




E=V*I*t

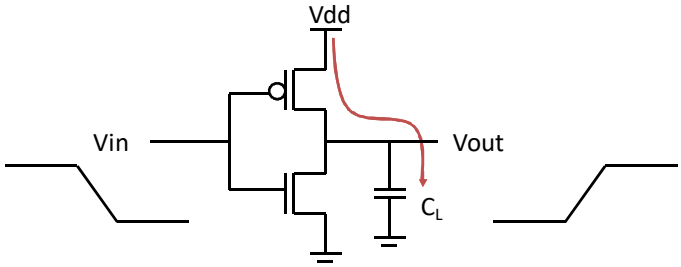
- Energy stored in capacitor:

$$E_C = \int_0^\infty i_{\mathrm{VDD}}(t) v_{\mathrm{out}} \mathrm{d}t = \int_0^\infty C_L \frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} v_{\mathrm{out}} \mathrm{d}t = \int_0^\infty C_L v_{\mathrm{out}} \mathrm{d}v_{\mathrm{out}} = \frac{1}{2} C_L V_{\mathrm{DD}}^2$$

- Energy taken by supply: $E_{\mathrm{VDD}} = C_L V_{\mathrm{DD}}^2$

232

# Charging and discharging




- Energy stored in $C_L$: $E_C = \frac{1}{2} C_L V_{DD}^2$
- Energy taken from supply: $E_{VDD} = C_L V_{DD}^2$
- Only half* of the energy stored in $C_L$!

*other half is "wasted" in PMOS transistor (resistance)

233

## Charging and discharging (cont'd)

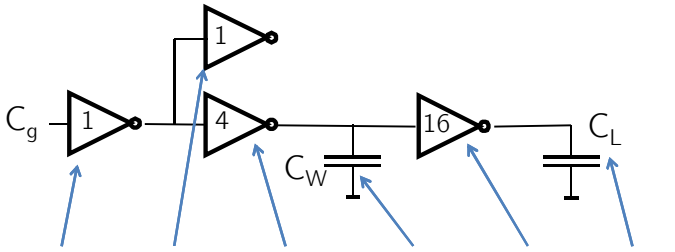
- Each switching cycle L→H→L takes a fixed amount of energy: $E_{cyc} = C_L V_{DD}^2$
- Energy dissipation is independent of
  - (size of NMOS/PMOS)
  - discharging circuitry (except the capacitance)
  - time of switching cycle

but depends on load

- Reducing energy: Reduce $C_L$ and $V_{DD}$

234

## Example: compute energy* (0-1-0)




$$E = E_1 + E_2 + E_3 + E_4 + E_5 + E_6$$

- Miller effect $2C_g$, $E_4$ and $E_6$ remain same

$$E = V_{DD}^2(2Cg + 2C_g + 8C_g + C_W + 32C_g + C_L)$$

*Remember: this is the energy of a 0-1-0 switching cycle

235

# Dynamic power consumption

- Power = energy / time
- Power consumption: $P_{dyn} = C_L V_{DD}^2 f_{0\to1\to0}$
- Gate switched on and off $f_{0\to1\to0}$ times per second (switching frequency)

- Example: 0.25µm design with 1M gates
  - $V_{DD}$=2.5V, 500MHz, $C_L$=15fF/gate (fan-out 4)
  - 46.875µW per gate → 46.875W (!!!)

236

# Dynamic power consumption

$$P_{total} = V_{DD}^2 f_{clk} \sum_{k}^{K} \frac{\alpha_k}{2} C_k$$

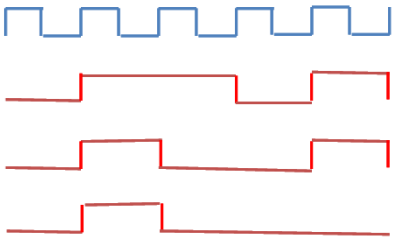
clock frequency

node/gate index

switching activity (per clock cycle)

load capacitance for node k

- Switching activity: $\alpha_k$ # of switches per cycle



clock signal $\alpha_k = 2$

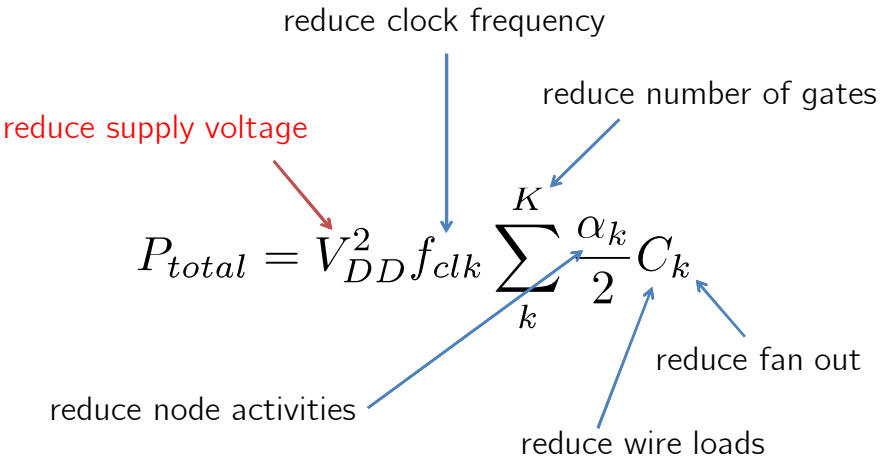
$\alpha_k = 4/5$

$\alpha_k = 4/5$

$\alpha_k = 2/5$

237

# How to reduce dynamic power?




238

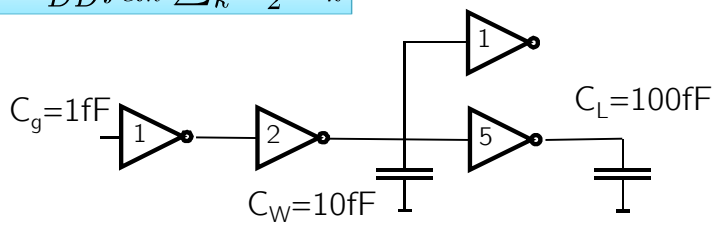
# Example revisited

- 0.25µm CMOS design with 1M gates
  - $V_{DD}$=2.5V,
  - 500MHz with 0-1-0 per cycle
  - $C_L$=15fF/gate (fan-out 4)
  - Average activity 10%
- 4.6875µW per gate → 4.6875W
- Reduce $V_{DD}$ to 1.8V → 2.43W

239

## Compute dynamic power consumption

$$P_{total} = V_{DD}^2 f_{clk} \sum_k^K \frac{\alpha_k}{2} C_k$$



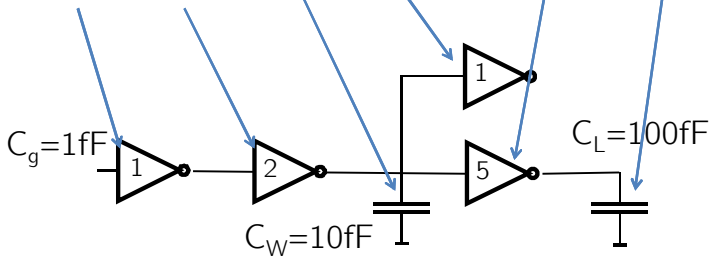

- Circuit switches once per clock cycle at every node (only for this simple example):

$$V_{DD} = 2\text{V} \quad f_{clk} = 1\text{GHz}$$

240

## Solution

$$E = V_{DD}^2(2C_g + 4C_g + 10\text{fF} + 2C_g + 10C_g + 100\text{fF})$$

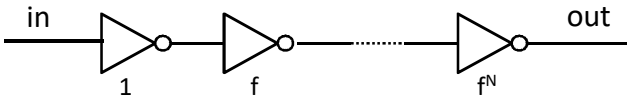



- Circuit switches once per clock cycle: $\alpha_k = 1$

$$P_{total} = 2^2 \cdot 1\text{GHz} \cdot \frac{1}{2} \cdot 128\text{fF} = 256\mu\text{W}$$

241

# Oh wait, sizing?!




- Sizing can reduce propagation delay
- But this is not free in terms of power!

$$C_{tot} = 2(C_g + fC_g + f^2C_g + \ldots + f^NC_g)$$

- Not easy to size inverters for min. power

242

Image adapted from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

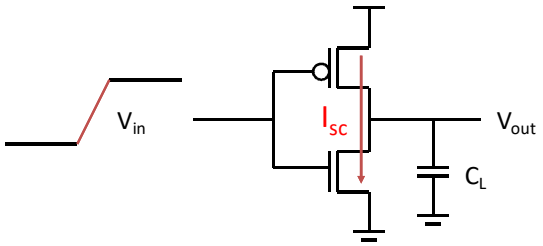
Another source of dynamic power consumption

# Crossover/direct-path currents

243

# Crossover or direct-path currents

- Finite slope of input signal causes direct path between $V_{DD}$ and GND for short time

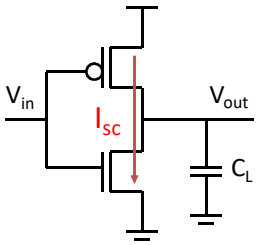


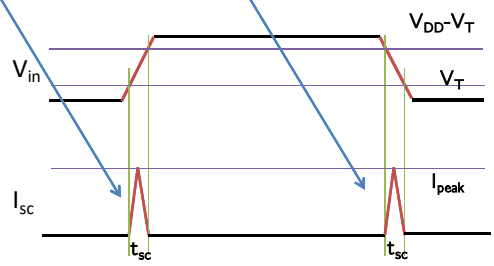

244

# Direct path/crossover energy

- Energy consumed per switching 0-1-0:

$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = V_{DD}I_{peak}t_{sc}$$




245

# Direct path/crossover power

- Average power consumption:

$$P_{dp} = V_{DD} I_{peak} t_{sc} f$$

- Peak current is determined by
  - saturation current:
    - depends on transistor size
    - technology
    - temperature
  - ratio between input and output slopes ($C_L$)

246

# Reduce direct-path currents

$$P_{dp} = V_{DD} I_{peak} t_{sc} f$$

$$t_{sc} \approx \frac{(V_{DD} - 2V_T)}{V_{DD}} \frac{t_r}{0.8}$$

rise or fall time

- Reduce W/L
- Reduce $V_{DD}$
- Make circuit switch fast: reduce $t_r$ and $t_f$

247

# Approximation for 0-1-0 cycle

$$E_{dp} \approx \frac{\beta}{12}(V_{DD} - 2V_T)^2 t_r$$

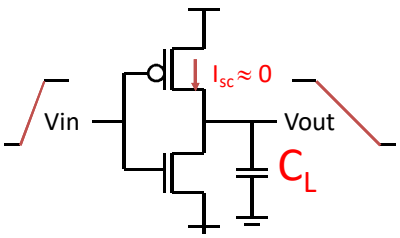
- Under a lot of assumptions
  - symmetry of $\beta_n$ and $\beta_n$, and threshold voltages
  - no output load… $C_L$=0
  - Input and output voltage rise linearly with ramp time $t_{ra}$
- Energy increases in $V_{DD}$ squared!

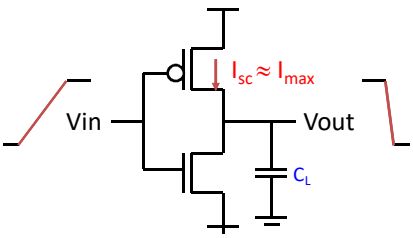
$\beta=\mu\varepsilon_{ox}/t_{ox}*W/L$

From the book H. J. M. Veendrick, Deep-Submicron CMOS ICs, from *Basics to ASICs*. Kluwer Academic Publishers, Deventer, 2000

248

# Impact of input/output slopes

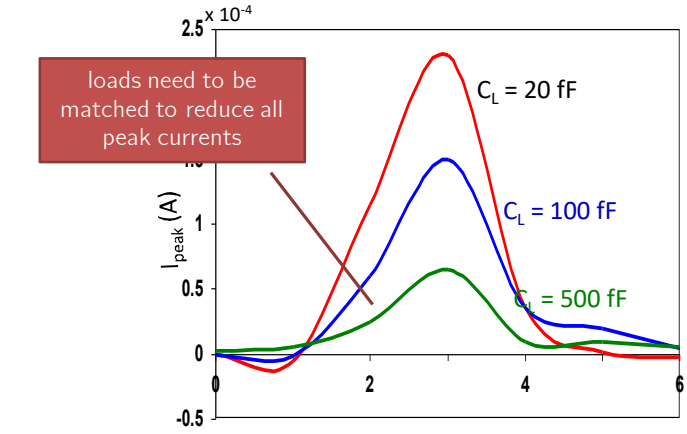



- Large load $C_L$
  - Output fall time larger than input rise time
  - Transistors off before output changed
- Small load $C_L$
  - Output fall time smaller than input rise time
  - Both transistors conducting for long time

249

# $I_{peak}$ as function of $C_L$




250

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