ECE4740: Digital VLSI Design

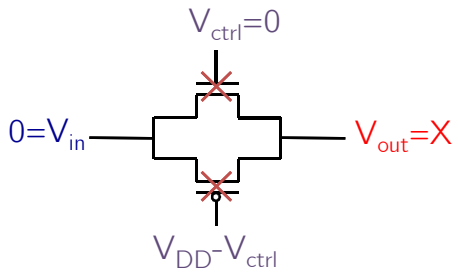
Lecture 4: The CMOS inverter

Just a few minutes

Recap pass transistors

The transmission gate

- A very useful circuit:



- Assume V_{in}=0
  - If V_{ctrl}=0, then NMOS & PMOS open
  - Input and output are not connected (ideally)

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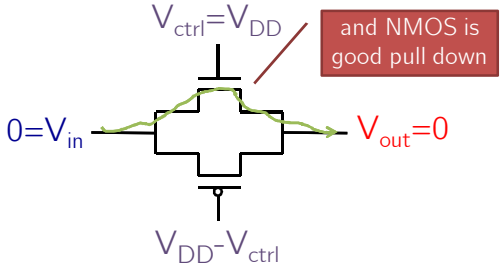
The transmission gate

- A very useful circuit:



- Assume V_{in}=0
  - If V_{ctrl}=V_{DD}, then NMOS & PMOS closed
  - Input and output are connected (ideally)

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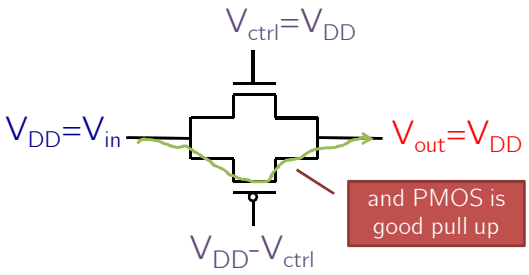
The transmission gate

- A very useful circuit:

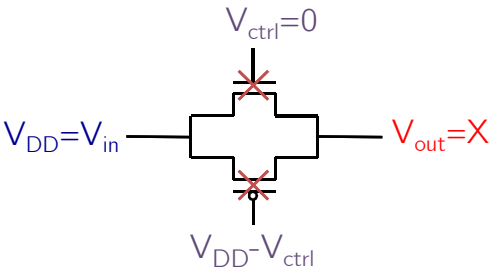


- Assume $V_{in}=V_{DD}$
  - If $V_{ctrl}=V_{DD}$, then NMOS & PMOS closed
  - Input and output are connected (ideally)

122

The transmission gate

- A very useful circuit:



- Assume $V_{in}=V_{DD}$
  - If $V_{ctrl}=0$, then NMOS & PMOS open
  - Input and output are not connected (ideally)

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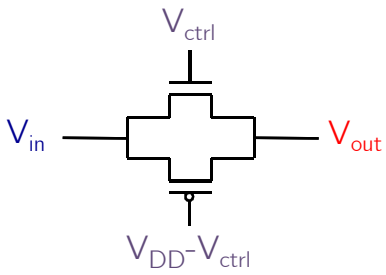
The transmission gate



Vin	Vctrl	Vout
Vss (0)	Vss (0)	X
Vdd (1)	Vss (0)	X
Vss (0)	Vdd (1)	Vss (0)
Vdd (1)	Vdd (1)	Vdd (1)

- Transmission gate → very good switch
  - Widely used for multiplexers, shifters, etc.
- Drawback: can be slow (serial resistance)

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The most basic device

The inverter

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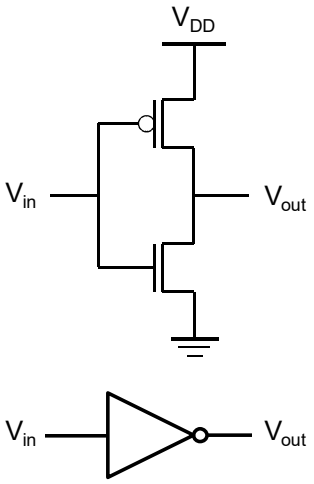
Objectives

- Analyze key properties of the CMOS inverter
  - noise margin
  - propagation delay
  - power consumption
- Two outcomes
  - able to analyze more complex but similar circuits
  - understand key concepts, gain intuition



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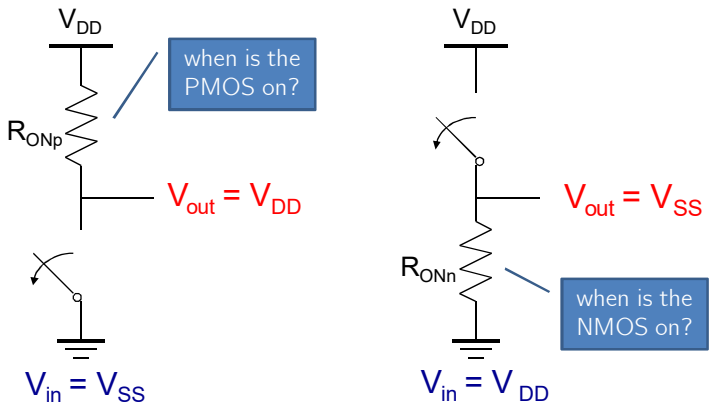
DC analysis of inverter: intuition



- What happens for general $V_{out}(V_{in})$?

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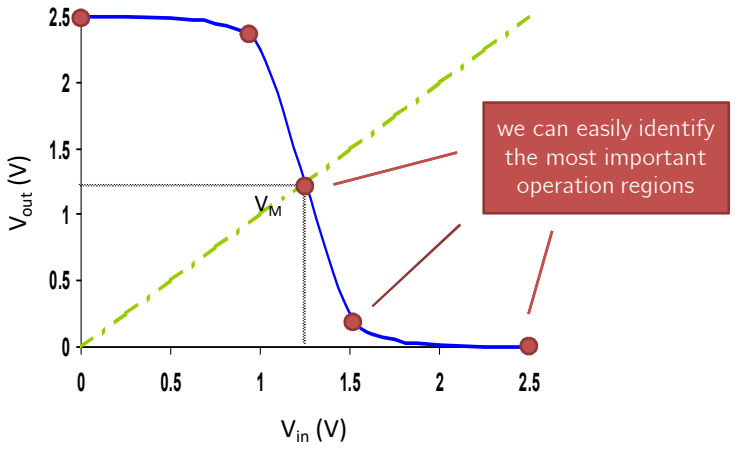
Voltage transfer characteristics



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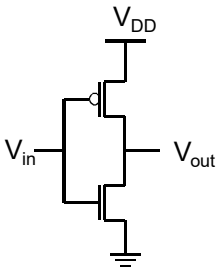
Regions of operation



	Cutoff	Linear/res.	Saturation
NMOS	$V_{GS}<V_{Tn}$	$V_{GS}-V_{Tn}>V_{DS}$ $V_{GS}>V_{Tn}$	$V_{GS}-V_{Tn}<V_{DS}$ $V_{GS}>V_{Tn}$
PMOS	$V_{GS}>V_{Tp}$	$V_{GS}-V_{Tp}<V_{DS}$ $V_{GS}<V_{Tp}$	$V_{GS}-V_{Tp}>V_{DS}$ $V_{GS}<V_{Tp}$

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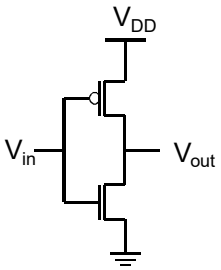
Regions of operation (cont'd)

NMOS view:

- $V_{in}=V_{GS}$
- $V_{out}=V_{DS}$

PMOS view:

- $V_{in}=V_{GS}+V_{DD}$
- $V_{out}=V_{DS}+V_{DD}$



	Cutoff	Linear/res.	Saturation
NMOS	$V_{in}<V_{Tn}$	$V_{in}-V_{Tn}>V_{out}$ $V_{in}>V_{Tn}$	$V_{in}-V_{Tn}<V_{out}$ $V_{in}>V_{Tn}$
PMOS	$V_{in}-V_{DD}>V_{Tp}$	$V_{in}-V_{Tp}<V_{out}$ $V_{in}-V_{DD}<V_{Tp}$	$V_{in}-V_{Tp}>V_{out}$ $V_{in}-V_{DD}<V_{Tp}$

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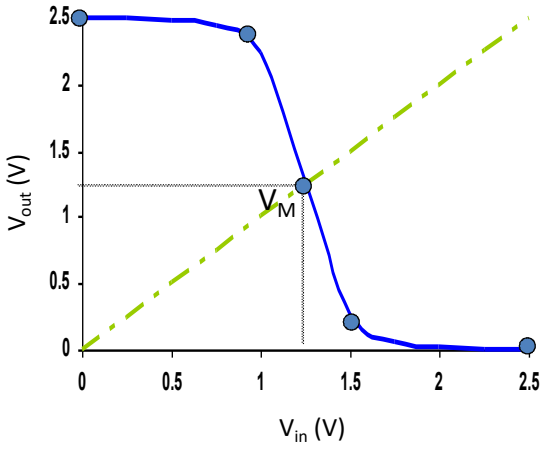
Voltage transfer characteristics

NMOS off
PMOS res



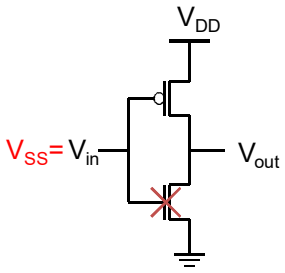


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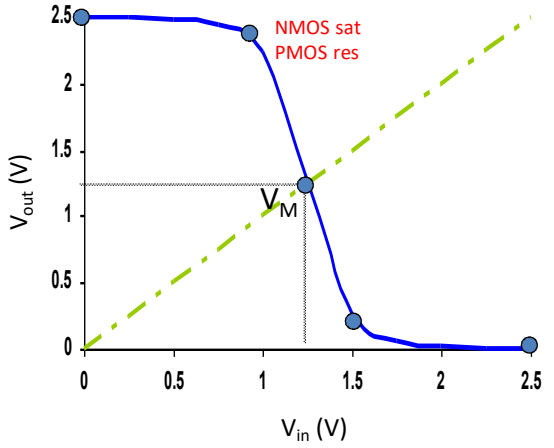
Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter5.pdf

Voltage transfer characteristics



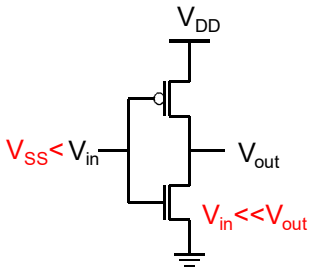


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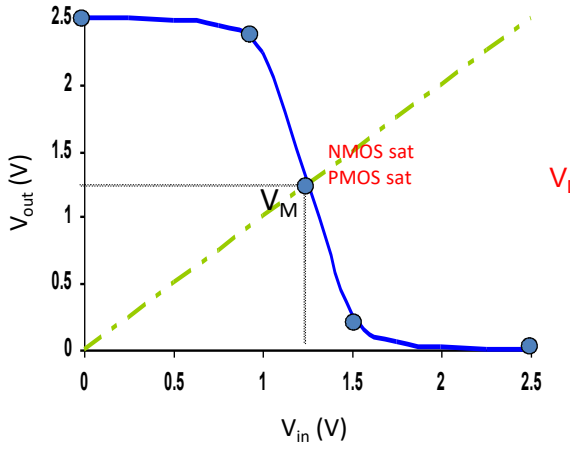
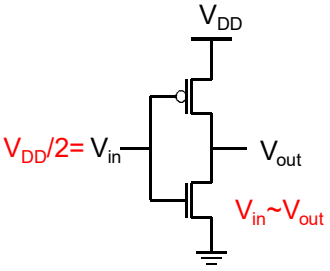
Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter5.pdf

Voltage transfer characteristics





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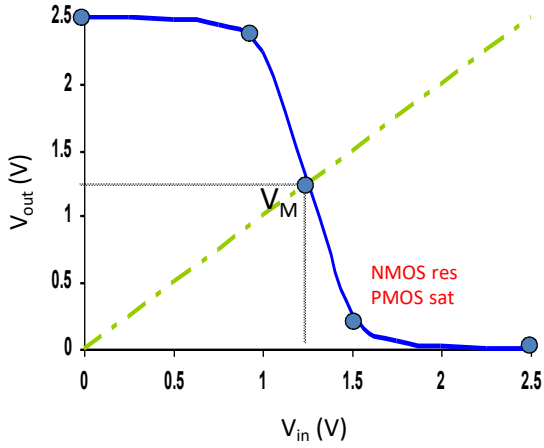
Voltage transfer characteristics



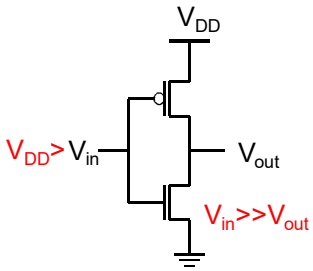


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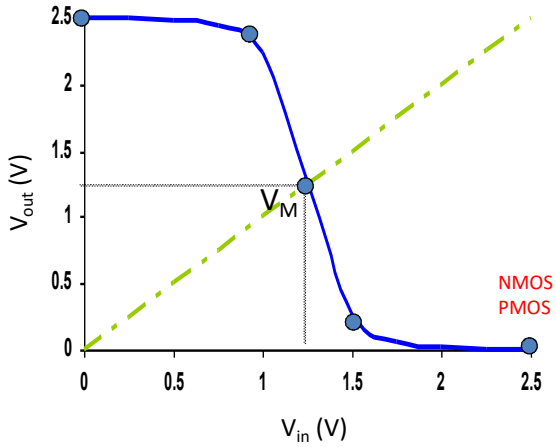
Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter5.pdf

Voltage transfer characteristics



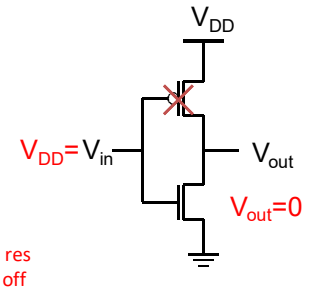


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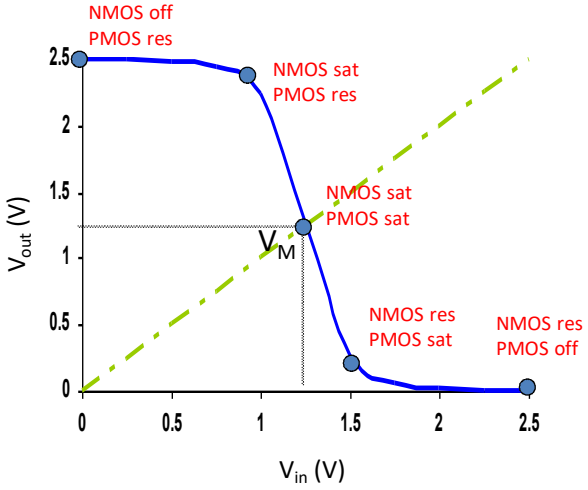
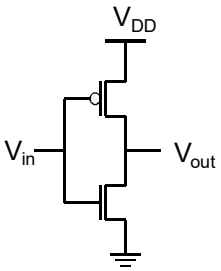
Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter5.pdf

Summary of VTC regions





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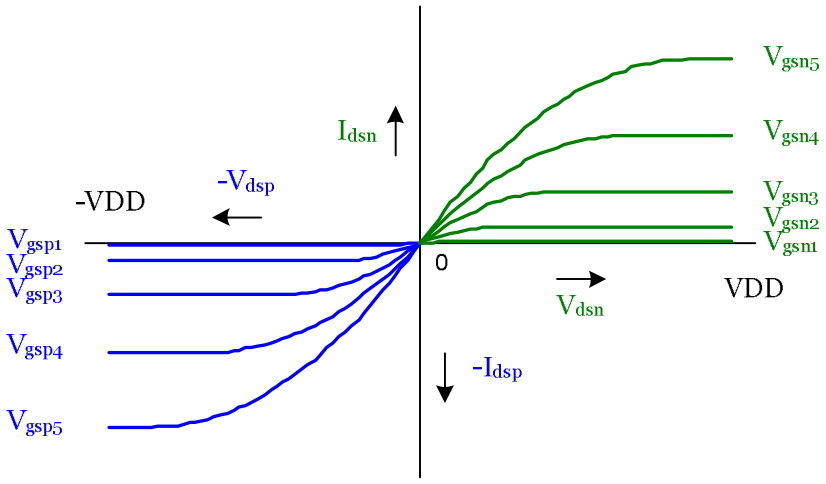
How to obtain VTC: Graphical way



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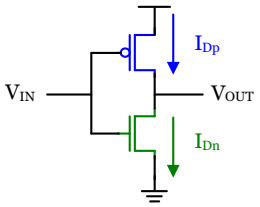
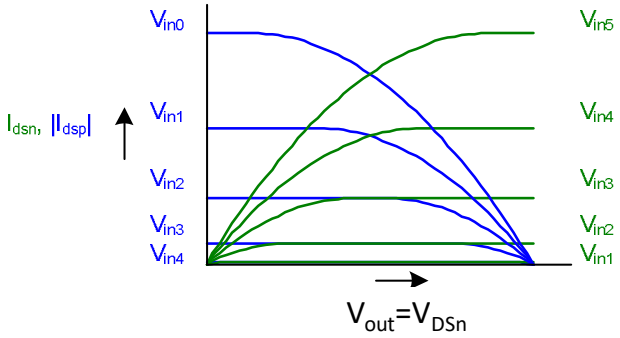
Load line analysis

- V_{out} is valid when $I_{Dn}=I_{Dp}$





$V_{GSn}=V_{in}$
$V_{GSp}=V_{in}-V_{DD}$

$V_{DSn}=V_{out}$
$V_{DSp}=V_{out}-V_{DD}$

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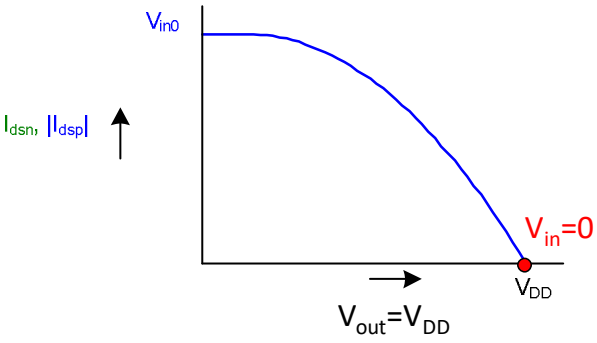
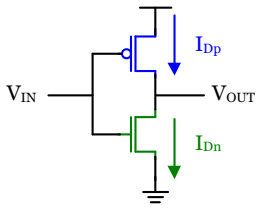
Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter5.pdf

Load line analysis (cont'd)

- $V_{in}=0.0V_{DD}$

PMOS res
NMOS off





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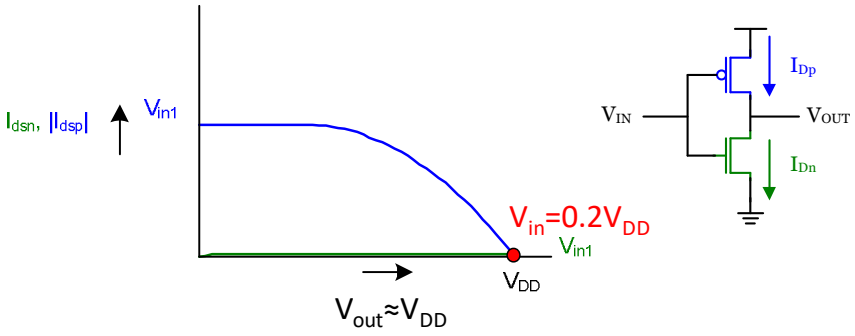
Load line analysis (cont'd)

- $V_{in}=0.2V_{DD}$

PMOS lin
NMOS sat



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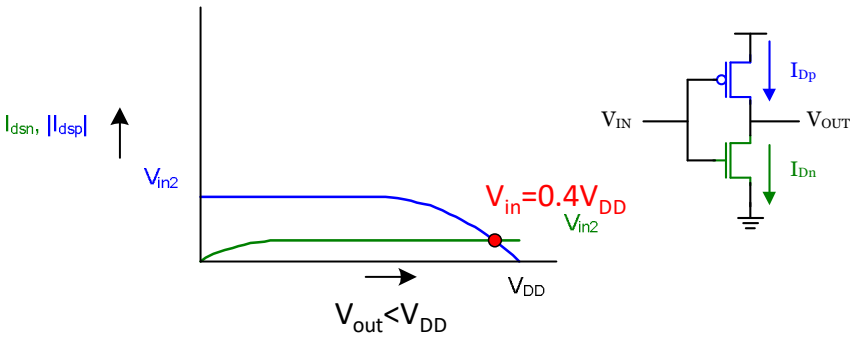
Load line analysis (cont'd)

- $V_{in}=0.4V_{DD}$

PMOS lin
NMOS sat



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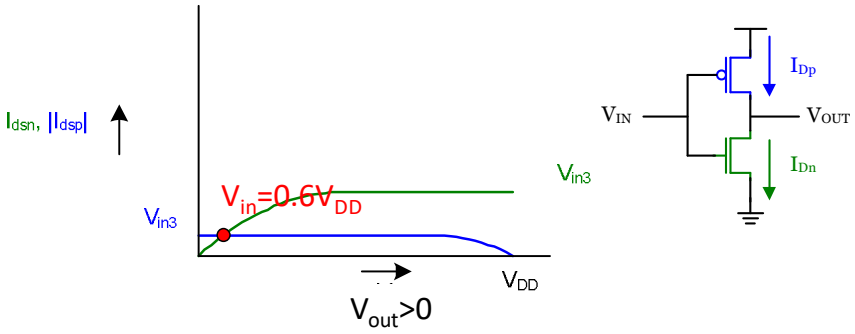
Load line analysis (cont'd)

- $V_{in}=0.6V_{DD}$

PMOS sat
NMOS lin



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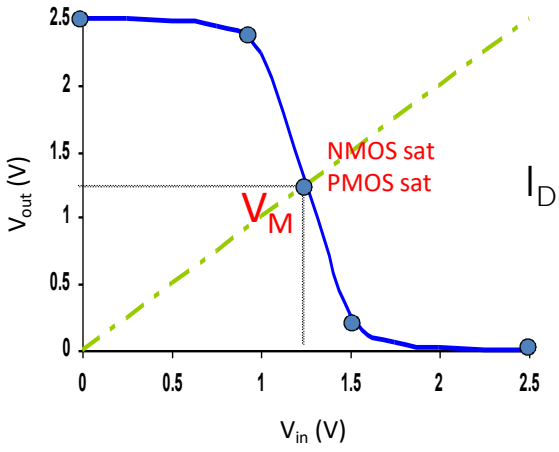
Switching threshold V_M

- Defined as the point where $V_{in}=V_{out}$



$I_{Dn}=I_{Dp}$

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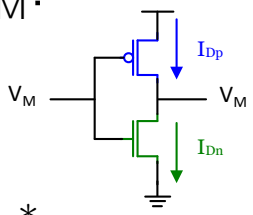
We can change V_M!



- PMOS & NMOS are saturated
- Assume velocity saturation, ignore channel length modulation*

$$I_{DSATn} = \nu_{SATn} C_{ox} W_n \left(V_M - V_{Tn} - \frac{1}{2} V_{DSATn} \right)$$

$$I_{DSATp} = \nu_{SATp} C_{ox} W_p \left(V_M - V_{DD} - V_{Tp} - \frac{1}{2} V_{DSATp} \right)$$

- Set $I_{DSATp} = -I_{DSATn}$ and solve for V_M

*follows from saturation formula (2.26) in Weste & Harris

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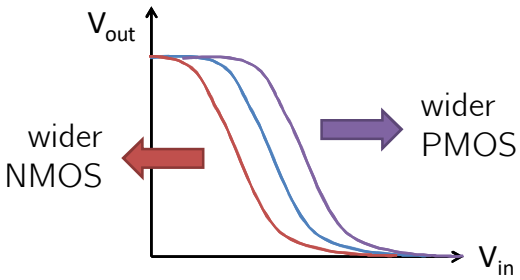
Switching threshold (cont'd)

- We want r=1 to have V_M=0.5V_{DD}
- Called skewed gate

$$V_M \approx \frac{r V_{DD}}{1 + r} \qquad r = \frac{\nu_{SATp} W_p}{\nu_{SATn} W_n}$$



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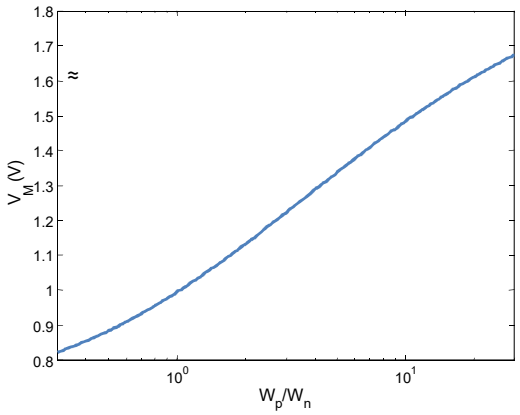
Sensitivity of V_M



- Process variation has little impact on V_M

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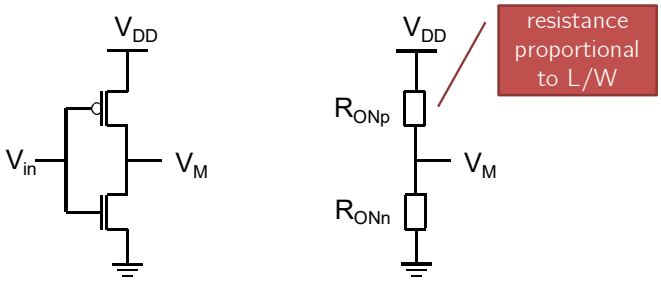
Taken From: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Intuition

- Think about a resistive divider



- Making W_p larger (or W_n smaller) reduces resistance R_{ONp} → V_M increases

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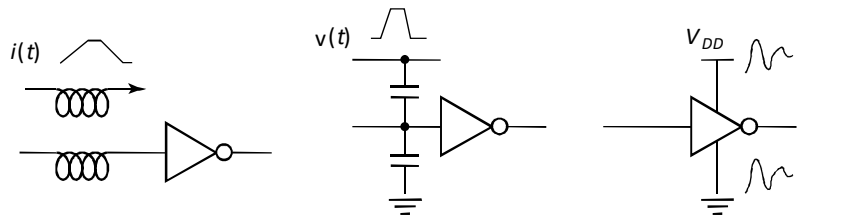
Good inverters are robust to noise!

Noise margins

Motivation: digital noise

- Inverter (and other circuits) should be robust to noise



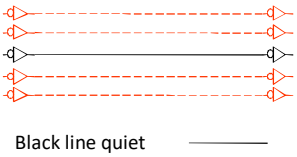
inductive coupling (crosstalk)

capacitive coupling (crosstalk)

power & ground noise (affects signal levels)

Example: Capacitive coupling

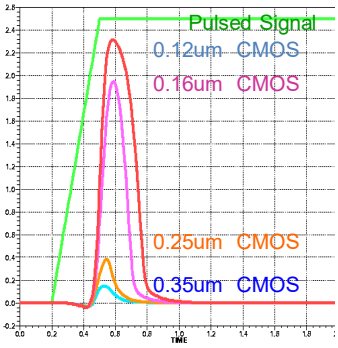
- With decreasing feature sizes, wire glitches stronger than 80% may occur due to crosstalk



Black line quiet

Red lines pulsed

Glitches strength vs. technology



From Dunlop, Lucent, 2000

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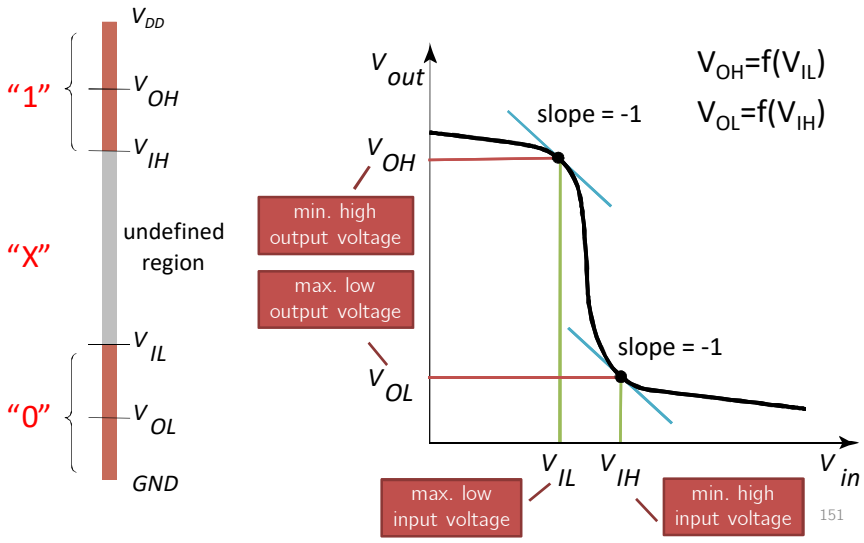
Mapping between analog voltage levels and digital signals



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Noise margins

- $NM_H = V_{OH}-V_{IH}$
- $NM_L = V_{IL}-V_{OL}$

should be as large as possible!

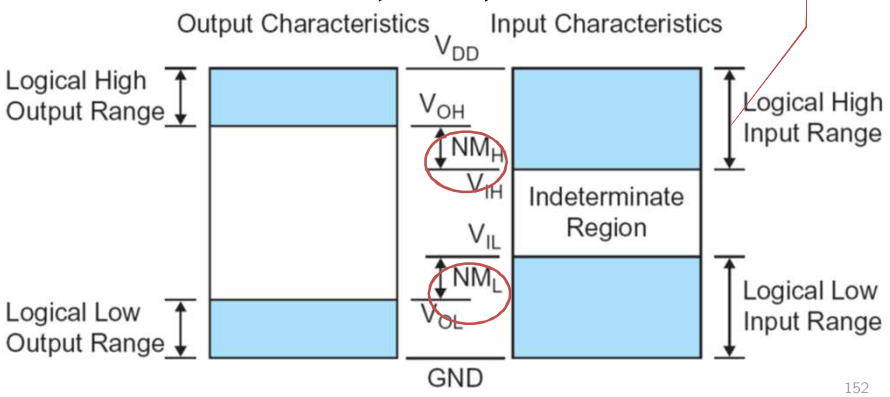

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Image taken from: Digital Design and Computer Architecture, Harris and Harris

Noise margins (cont'd)

- Good inverters map a larger logical input range to a smaller logical output range

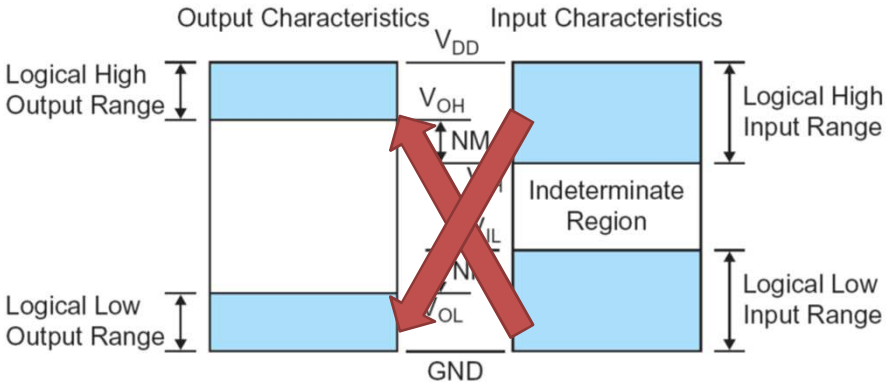

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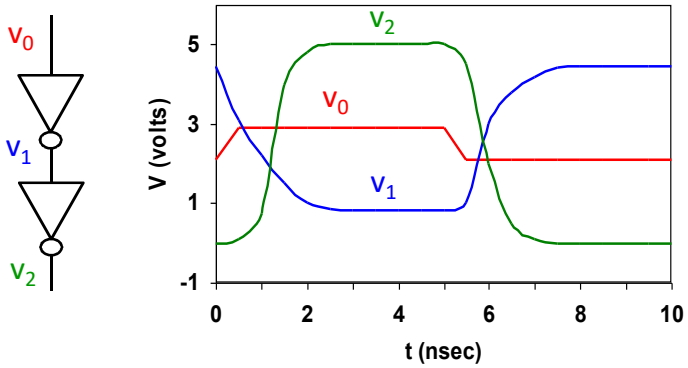
Image taken from: Digital Design and Computer Architecture, Harris and Harris

Regenerative property

- Disturbed signal goes back to nominal voltage levels by passing through inverters



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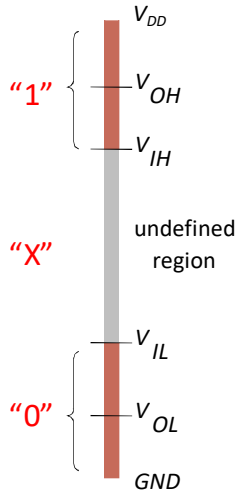
Implications

- Assume input signal is
  - "1", i.e., $V_{in} > V_{IH}$
  - "0", i.e., $V_{in} < V_{IL}$
- Inverter with regenerative property will restore signal to
  - $V_{out} = V_{OH}$
  - $V_{out} = V_{OL}$



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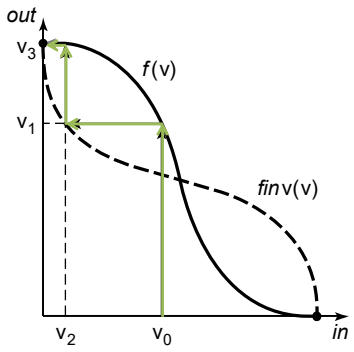
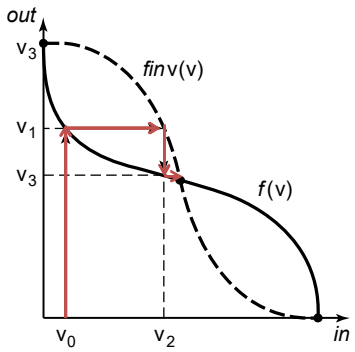
Intuition: Regenerative property



regenerative inverter



non-regenerative inverter

- Good inverter:
  - undefined region: gain>1
  - defined region: gain<1

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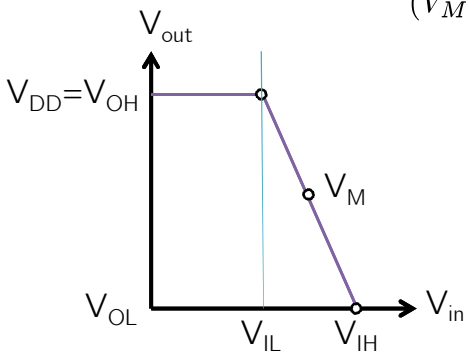
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Determining V_{IL}

- Assume piece-wise linear inverter & use gain at V_M which is

$$g = \frac{1+r}{(V_M - V_{Tn} - V_{SATn/2})(\lambda_n - \lambda_p)}$$



$$V_M = \frac{V_{IH} + V_{IL}}{2}$$

$$\frac{V_{DD}}{V_{IH} - V_{IL}} = -g$$

$$V_{IL} = V_M + \frac{V_{DD}}{2g}$$

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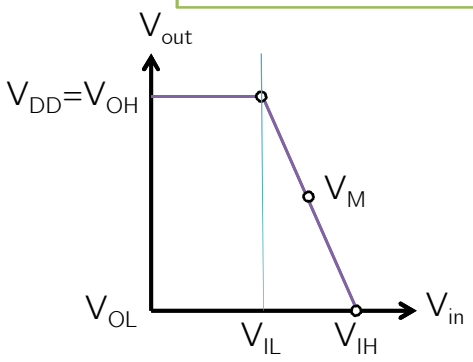
Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter5.pdf

You determine V_{IH}

$$V_{IH} = V_M - \frac{V_M}{g}$$



$$V_M = \frac{V_{IH} + V_{IL}}{2}$$

$$\frac{V_{DD}}{V_{IH} - V_{IL}} = -g$$

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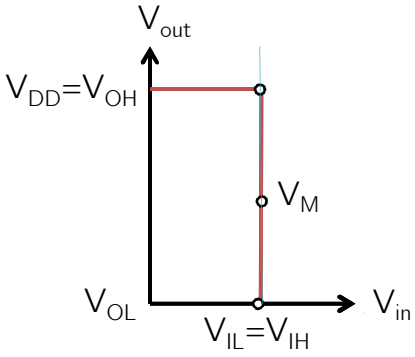
The "ideal" inverter

- High gain g in transition region is highly desirable



- $NM_H = V_{OH}-V_{IH}=VDD/2$
- $NM_L = V_{IL}-V_{OL}=VDD/2$

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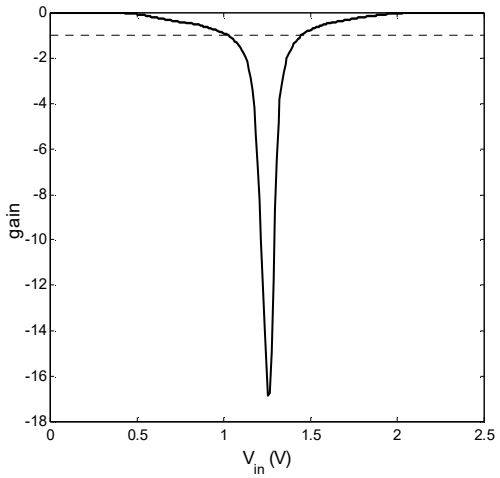
Gain of a real inverter



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