ECE4740: Digital VLSI Design

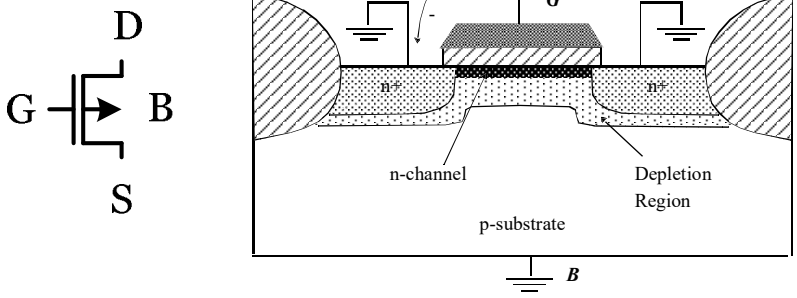
Lecture 3: Nanometer MOSFETs

It's not that complicated...

Body effect revisited

Body effect revisited

- Again: What is the impact of V_B to V_T?



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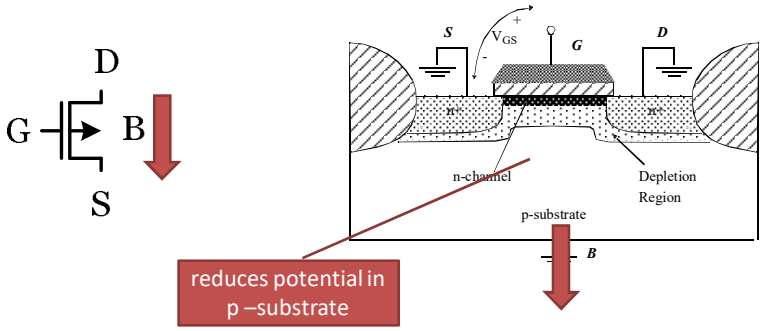
Body effect revisited (cont'd)

- Let us lower V_B (such that $V_B<V_S$)
- Equivalent with reducing $V_{BS}=V_B-V_S$ or increasing $V_{SB}=V_S-V_B$



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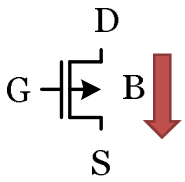
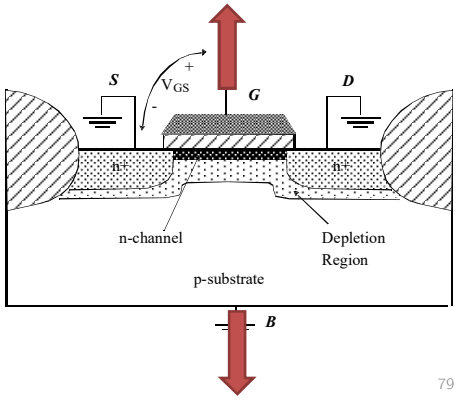
Body effect revisited (cont'd)

- Means we need larger V_G to form n-channel!
- Threshold voltage V_T increases





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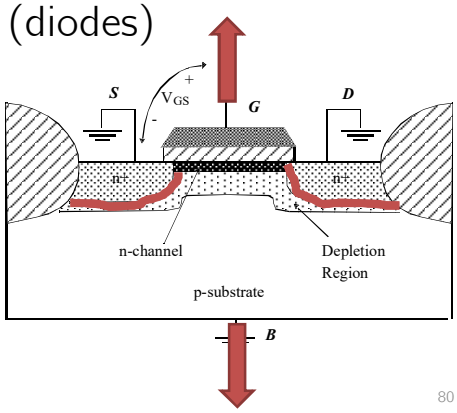
Other explanation

- If we lower V_B, then depletion region at source and drain grows → think reverse biased pn-junctions (diodes)
- Charge gets pulled out of channel to depletion region
- Requires larger V_{GS} to undo that effect



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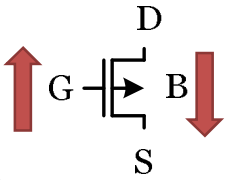
Summary of body effect

- Reducing V_B such that $V_B<V_S$ is equivalent to reducing V_{BS} or increasing V_{SB}
- V_{SB}↑ means threshold voltage V_T↑
- V_{SB}↓ means threshold voltage V_T↓
- Opposite behavior for V_{BS}



$$V_T = V_{T_0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

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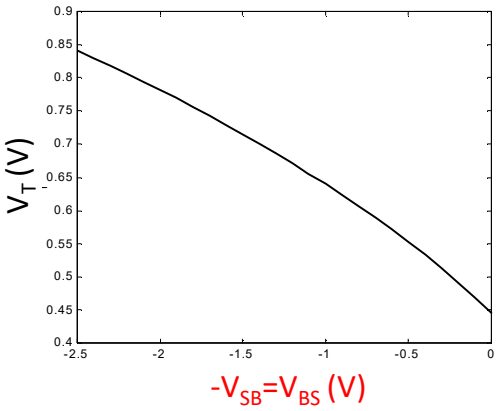
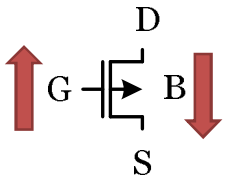
The graph





increasing V_{SB} reduces V_{BS}, which increases V_T

Why should we care?

- The body effect can be used to
  - Make switching faster (reducing V_T)
  - Reduce static power consumption due to leakage (increasing V_T):
    - normal operation:
      → connect B with S
    - standby operation:
      → lower V_{BS}

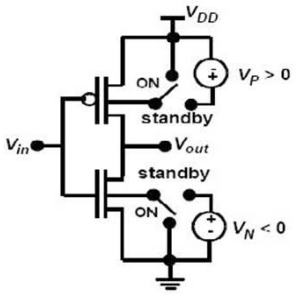


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Image taken from: http://www.eeherald.com/section/design-guide/Low-Power-VLSI-Design.html

Today's devices are tiny!

Short-channel effects

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Modern transistors are tiny

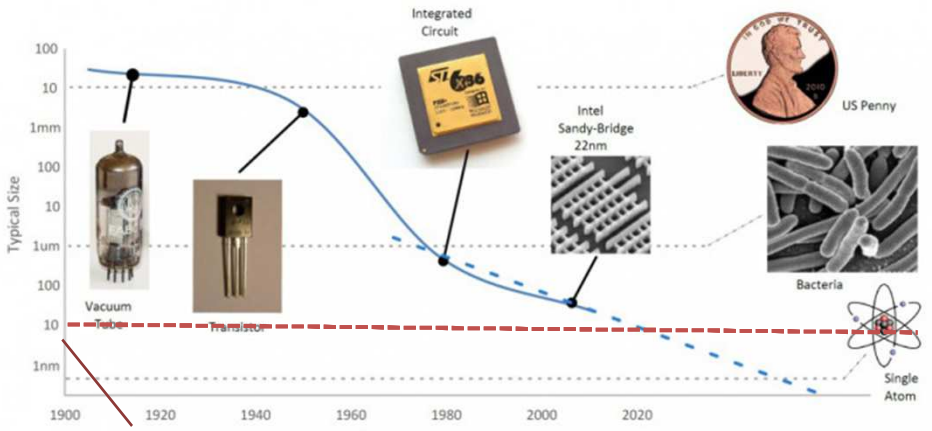

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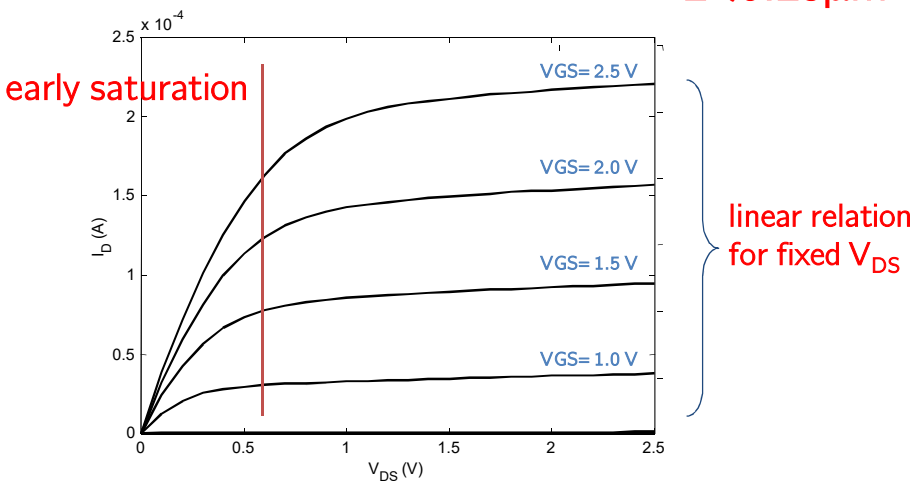
Image taken from: https://theglobalscientist.com/2014/04/07/the-next-big-step-in-computers-what-can-physics-offer-us/

How about short-channel devices?

L<0.25µm



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Velocity saturation

- Velocity of carriers saturates due to scattering (collisions)
- For L=0.25µm NMOS, only $V_{DS} \approx 2V$ is sufficient to reach velocity saturation

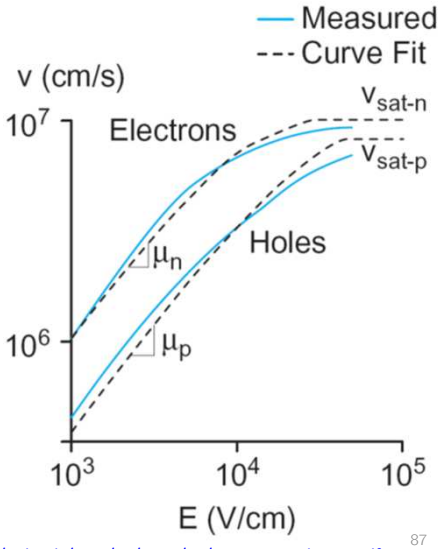

Image taken from: http://ic.sjtu.edu.cn/ic/dic/wp-content/uploads/sites/10/2013/04/CMOS-VLSI-design.pdf

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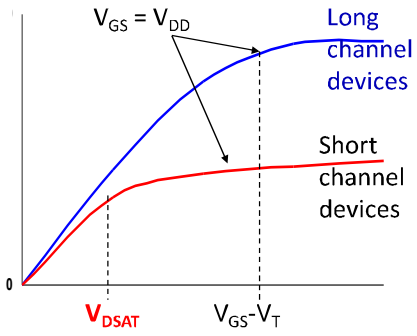
Effects of velocity saturation



- Short-channel device enters saturation before $V_{DS}=V_{GS}-V_T$
- Saturation current $I_{DS(sat)}$ shows linear dependence with V_{GS}
- V_{sat} more pronounced in NFET than PFET

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(First-order model)

- Carrier velocity can be modeled as:

$$\nu = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \le \xi_c$$
$$= \nu_{sat} \quad \text{for} \quad \xi \ge \xi_c$$
$$\xi_c = \frac{2\nu_{sat}}{\mu_n}$$

- We can redo the calculations for the resistive and saturation region (not important)

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Improved FET models

this term lowers the carrier mobility

- Resistive (linear) region: $V_{GS}-V_T>V_{DSat}$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \kappa(V_{DS})$$
$$\kappa(V_{DS}) = \frac{1}{1 + V_{DS}/(\xi_c L)}$$

- (Velocity) saturation region: $V_{GS}-V_T<V_{DSat}$

$$I_{DSsat} = \mu_n C_{ox} \frac{W}{L} \left(V_{GT} V_{DSsat} - \frac{V_{DSsat}^2}{2} \right) \kappa(V_{DSsat})$$
$$V_{DSsat} = \kappa(V_{GT}) V_{GT} \approx \frac{L\nu_{sat}}{\mu_n}$$

$V_{DSat}=\kappa(V_{GT})*V_{GT}$, $V_{GT}=V_{GS}-V_T$

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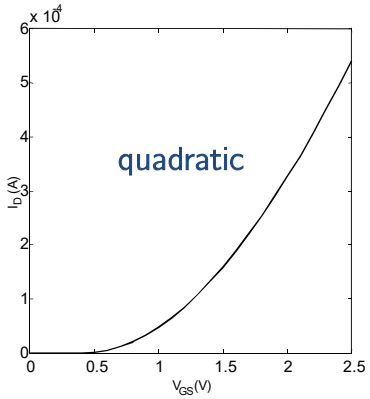
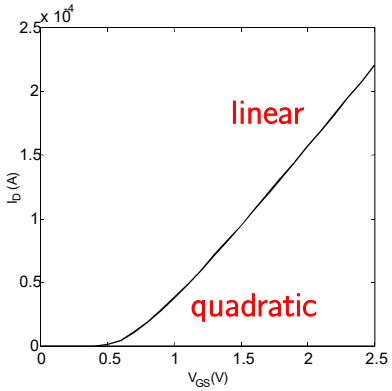
I_D vs. V_{GS} characteristics



long channel



short channel

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Short-channel PFET

- Once, again: polarities of all voltages and currents reversed

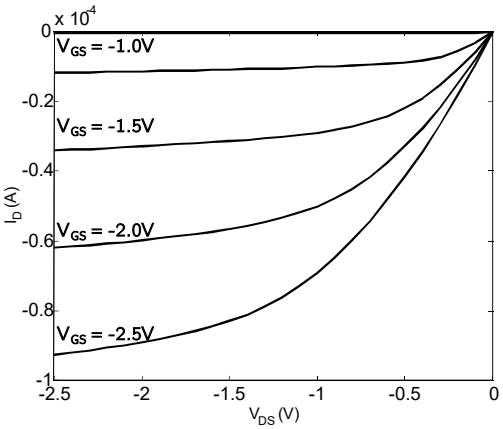

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Image taken from: http://spongebobia.com/spongebob-captures/gallery.php?prod=009b

What happens if $V_{GS}<V_T$?

Subthreshold conduction

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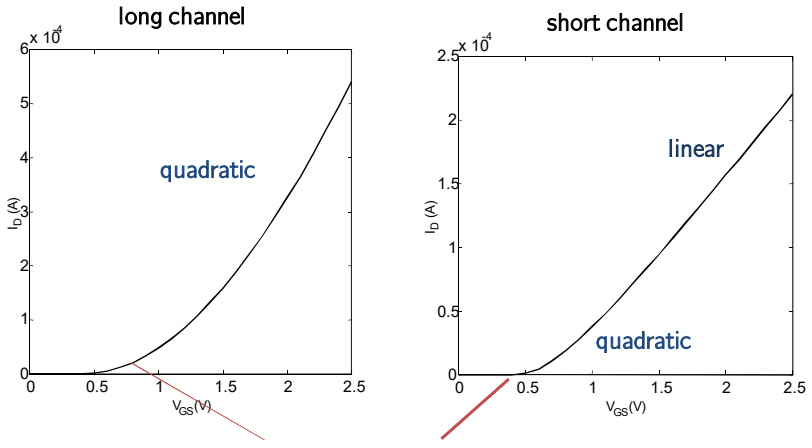
Another look at I_D vs. V_{GS} curves



current does **not** drop abruptly to 0 for $V_{GS}<V_T$

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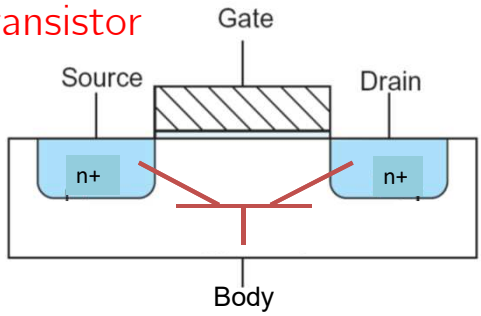
Subthreshold conduction (leakage)

- FETs are conducting partially for $V_{GS}<V_T$
- Parasitic bipolar transistor



- Two diode equations:

$$I_{DS} = I_S e^{\frac{V_{GS}}{nkT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)(1 + \lambda V_{DS})$$

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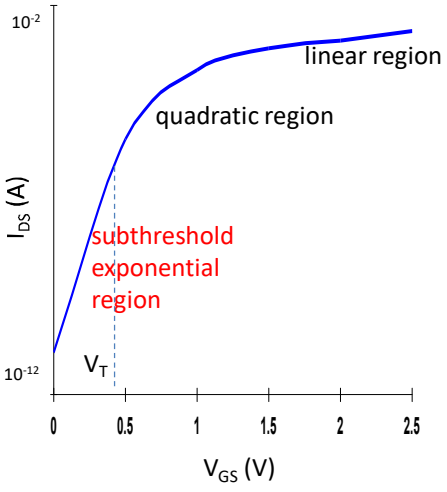
Subthreshold conduction (cont'd)

- Undesirable effect:
  - Current flowing when transistor should be off
- Affects dynamic circuits (DRAMs)
- Affects static power consumption

WHY?

$$I_{DS} \sim I_S e^{\frac{V_{GS}}{nkT/q}}$$



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They will affect the dynamic behavior!

FET capacitances and resistances

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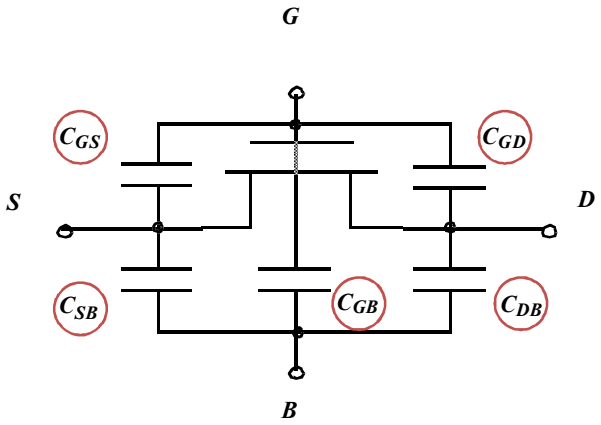
MOSFET capacitance model



- We are typically interested in modeling this as a single capacitance C_G

Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f10/Lectures/Lecture11-MOS_Cap_Delay-6up.pdf

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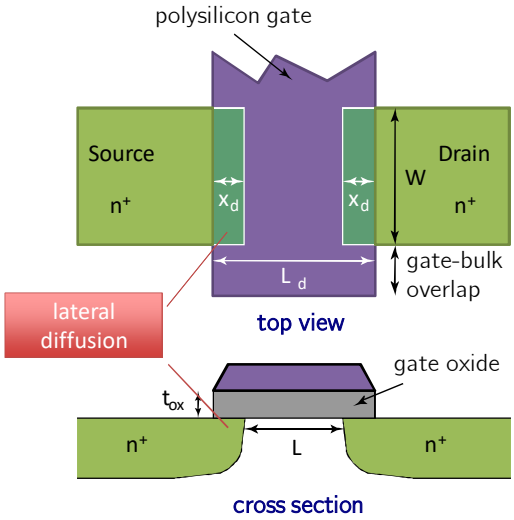
Gate capacitance*



$$C_{gate} = C_{ox} W L$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\left.\begin{matrix} C_{GSO} \\ G_{GDO} \end{matrix}\right\} = C_{ox} x_d W$$

overlap capacitances; no big deal in deep submicron technology!

*The gate capacitance is necessary to form the channel; all other capacitances are parasitic and not needed.

Image taken from: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f10/Lectures/Lecture11-MOS_Cap_Delay-6up.pdf

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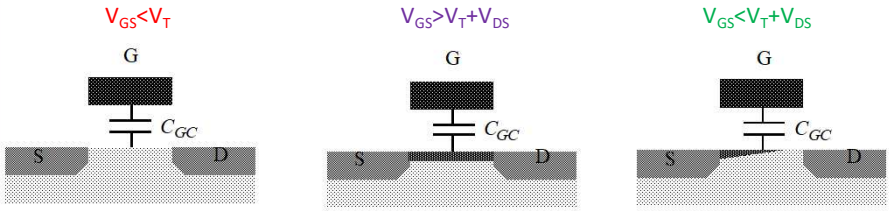
C's depend on operation regime!



Region	C_{GB}	C_{GS}	C_{GD}	C_G
Subthreshold	$C_{ox}WL$	0	0	$C_{ox}WL + 2C_oW$
Linear	0	$C_{ox}WL/2$	$C_{ox}WL/2$	$C_{ox}WL + 2C_oW$
Saturation	0	$2/3C_{ox}WL$	0	$2/3C_{ox}WL + 2C_oW$

C_o=overlap cap. often ignored

- Important regions are saturation and subtreshold

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Junction (diffusion) capacitances

- Caused by reverse-biased source-body and drain-body pn-junctions
- Nonlinear (voltage dependent)

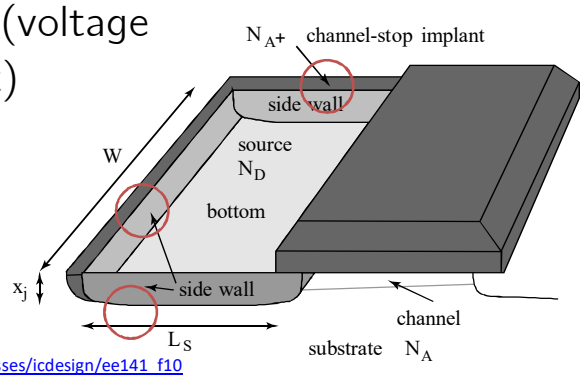

Image taken from:
http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f10/Lectures/Lecture11-MOS_Cap_Delay-6up.pdf

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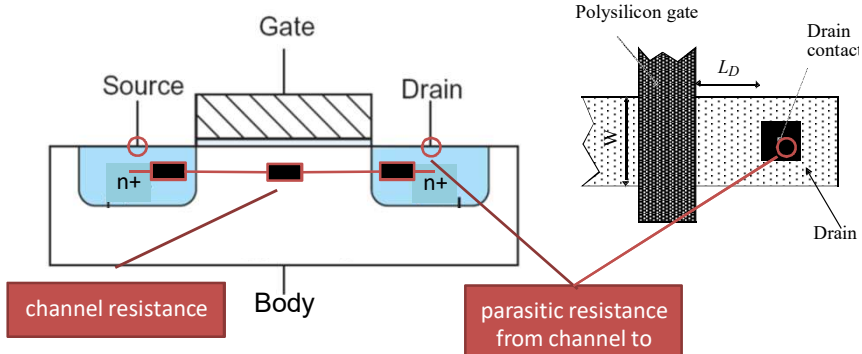
Parasitic resistances

- Drain-source on resistance (R_{DSon})



$$R_{DSon} = \frac{L_{S,D}}{W} R_{\square} + R_C$$

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Challenges of deep-submicron devices

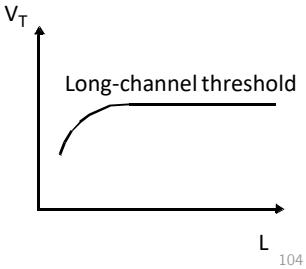
Nanometer transistors

Threshold variations

- For deep submicron devices, threshold voltage becomes function of (small) L, W, **and V_{DS}**

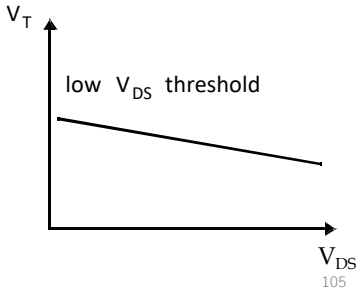
$$V_T = V_{T_0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

- Depletion regions of source and drain junction cannot be ignored anymore
  - parts of gate already depleted
  - reduces V_T



Threshold variations (cont'd)

- Increasing V_D increases width of drain pn-junction depletion region
  - decreases V_T: approximate model $V_T = V_{T0} - \lambda_d V_{DS}$
  - known as drain-induced barrier lowering (DIBL)
  - Not that critical for digital circuits
- If V_{DS} exceeds certain voltage: D-S shortened
  - called punch-through
  - permanent device damage!



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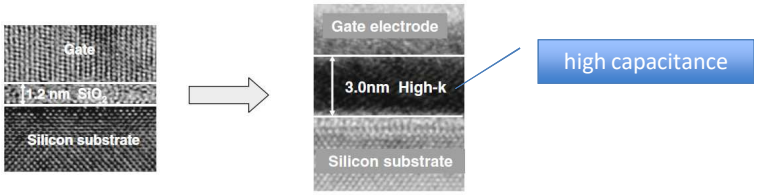
Gate leakage

- High electric field can cause tunneling through gate oxide (insulator)
- Becomes an issue for L=100nm and below (static power consumption)



	High-*k* vs SiO_2	Benefits
Gate capacitance	60% greater	Faster transistors
Gate dielectric leakage	>100% reduction	Lower power

http://ixbtlabs.com/articles2/intel-65nm/

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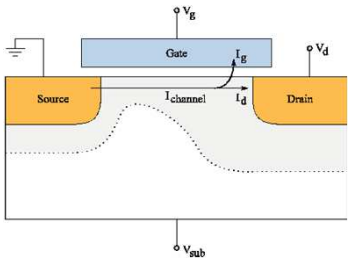
Hot carrier effects

- Threshold voltage drifts over time
- Electrons (and holes) can tunnel into the gate oxide at 1V/µm
  - V_T increases for NMOS
  - V_T decreases for PMOS



- Causes long-term reliability issues

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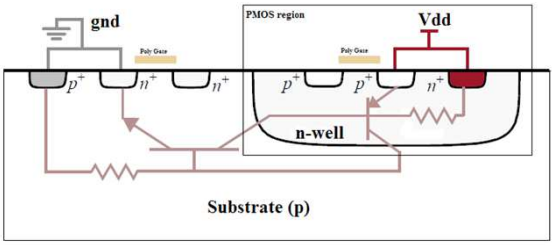
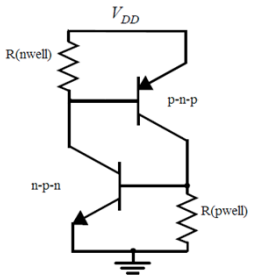
CMOS latch-up





- Parasitic bipolar transistors
  - If one of the bipolar transistors is forward biased, current flows into other BJT
  - Positive feedback → circuit fails
- R_{nwell} and R_{pwell} must be minimized!
  - provide additional well and substrate contacts close to source connections

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Image taken from: https://en.wikipedia.org/wiki/Latch-up

They will be very useful later

Pass transistors

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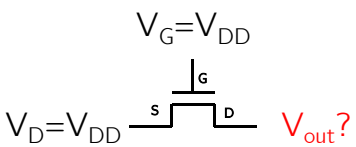
Pass transistor*

- We assumed that V_S is on GND
- What if $V_S>0$? E.g., transistor passing V_{DD}



- If $V_G-V_T<V_S$ then NFET is off
- NMOS cannot pull higher than $V_{DD}-V_{Tn}$
- PMOS pull no lower than $|V_{Tp}|$

*You should think that there is a big resistor pulling D down to ground.

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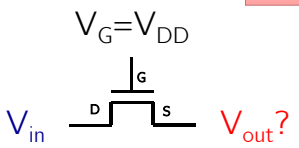
Pass transistor (cont'd)

- NMOS cannot pull higher than V_{DD}-V_{Tn}
- Simple formula for NMOS:

$$V_{out} = \min\{V_G - V_T, V_{in}\}$$



- NFET is a bad pull up (max V_{DD}-V_T)
- PFET is a bad pull down (min V_T)

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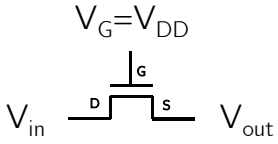
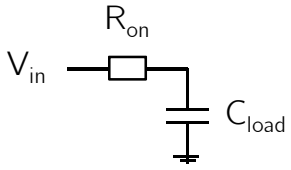
Pass-transistor delay



time constant:

$$\tau = R_{on} C_{load}$$



but they can be very cheap switches!

- Pass transistors can be slow, especially if load capacitance is large

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Things to remember

Recap MOSFET

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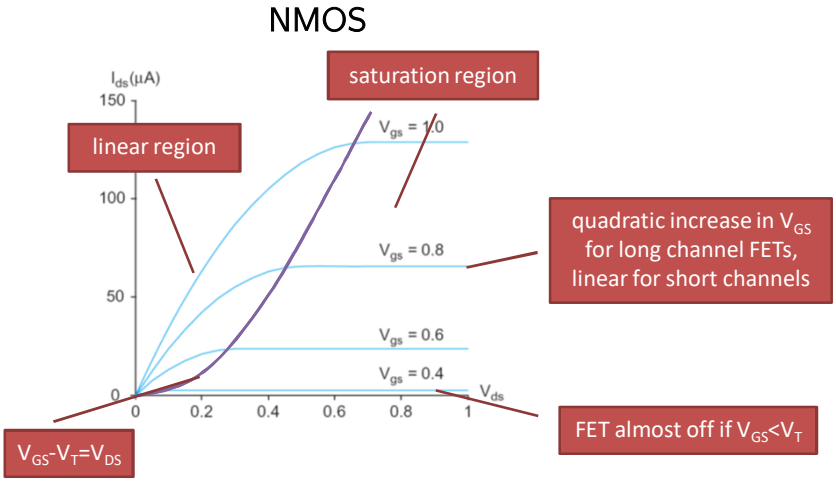
Recap: MOSFET

NMOS



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Things to remember: NFET/NMOS

- FETs are "switches"; almost off when $V_{GS}<V_T$
- Operating regimes
  - linear (resistive) regime: $V_{GS}-V_T>V_{DS}$
  - saturation regime: $V_{GS}-V_T<V_{DS}$
- Channel-length modulation
- Short-channel effects: velocity saturation
  - transistor earlier in saturation regime
  - V_{GS} has linear relationship on I_D
- Subthreshold conduction ☹

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Square law equations of long NMOS

- Linear (resistive or triode) regime

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

$V_{GS} > V_T$
$V_{DS} < V_{GS}-V_T$

- Saturation regime

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$V_{GS} > V_T$
$V_{DS} > V_{GS}-V_T$

- Subthreshold regime

$$I_{DS} = I_S e^{\frac{V_{GS}}{nV_{th}}}(1-e^{-\frac{V_{DS}}{V_{th}}})$$

$V_{GS} < V_T$

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PFET/PMOS

- Polarities of all voltages and currents reversed

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