ECE4740: Digital VLSI Design

Lecture 2: Diodes and MOSFET

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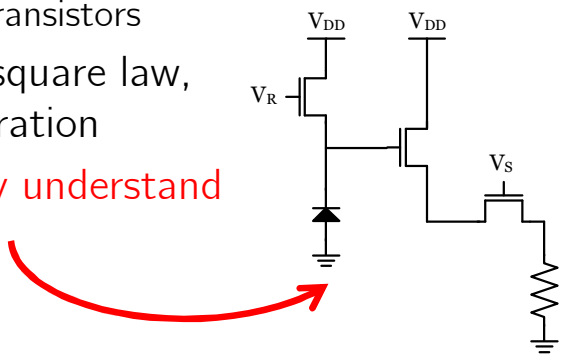
Goals for next few lectures

- Device basics:
  - Diode
  - MOS(FET) transistors
- Origin of V_T, square law, regions of operation
- Able to quickly understand such circuits:



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Recap: End of Moore's Law?

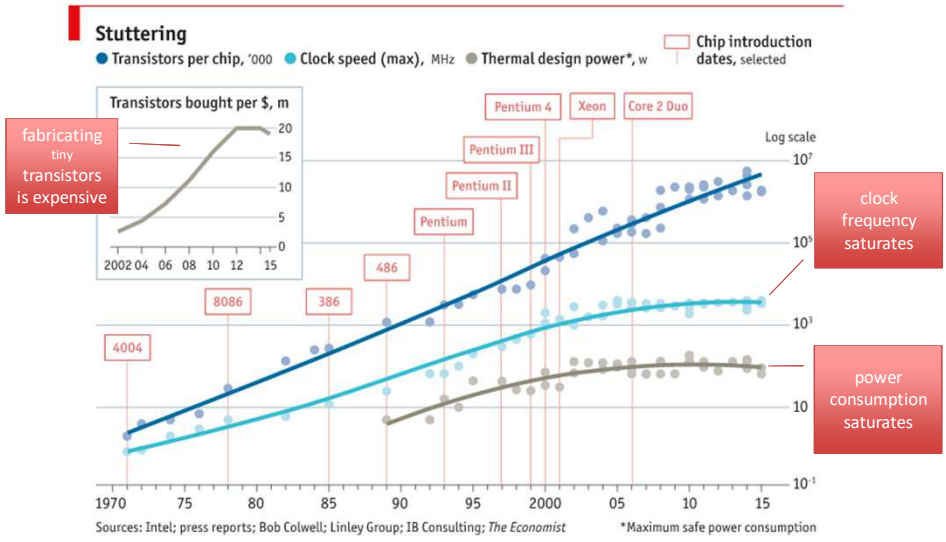

Image taken from: http://www.economist.com/technology-quarterly/2016-03-12/after-moores-law

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Device basics

The diode

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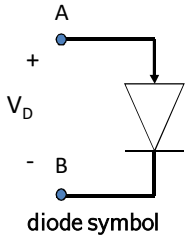
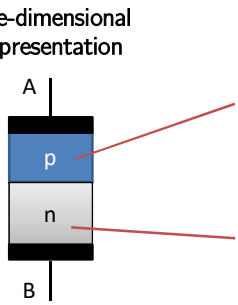
Basics: pn-junction diode

- Simplest of the semiconductor devices
- Mostly occur as parasitic elements
- Used to protect chips against electrostatic discharge (ESD)





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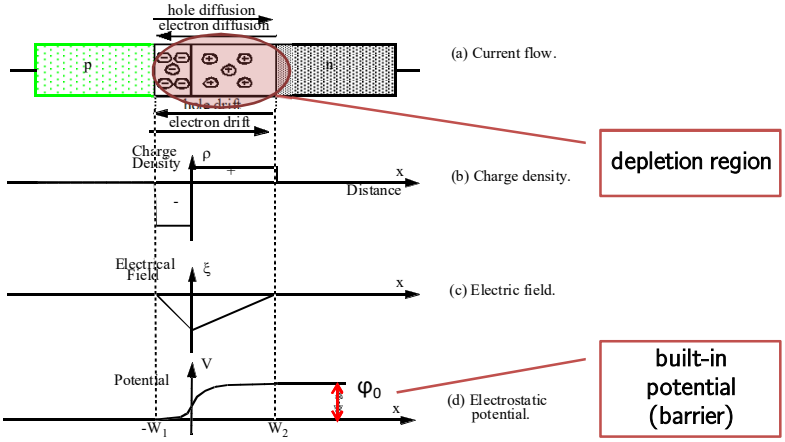
Depletion region



- Forward-bias lowers barrier; carriers can flow across junction
- Reverse-bias raises barrier; diode becomes non-conducting

Image taken from: https://archive.cnx.org/contents/432561b3-5dbf-4142-b9d2-60c08c3a5cee@1/sspd-chapter-3-solid-state-diode-physics

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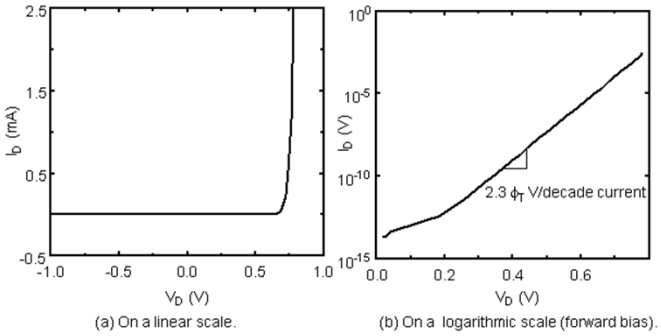
What is it doing?

- Diode allows current in forward direction
- Blocks current in reverse direction



(a) On a linear scale. (b) On a logarithmic scale (forward bias).

Image taken from: https://www.roadtrafficsigns.com/one-way-signs

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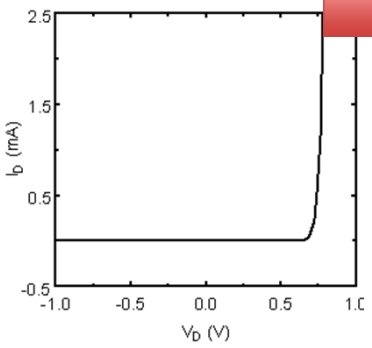
Shockley (ideal) diode equation



saturation current ~ 1e-14A

ideality factor (emission coefficient) n=1....2

$$I_D = I_S(e^{\frac{V_D}{n\phi_T}} - 1)$$

$$\phi_T = \frac{kT}{q} = 26\,\mathrm{mV}$$

thermal voltage (usually at 300K)

- Saturation current is proportional to the area of the diode: Roughly 17e-17A/μm^2

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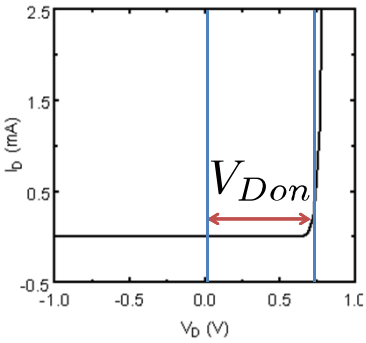
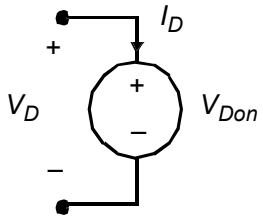
Model for manual analysis





$$V_{Don} \approx 0.7\,\mathrm{V}$$

- Model for fully conducting diode
- Non-conducting diode is simply an open circuit
- In digital ICs, diodes are usually reverse biased!

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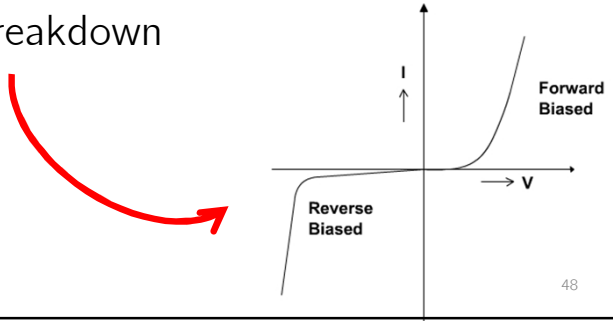
Secondary effects

- Serial resistivity (1Ω-100Ω)
- Junction capacitance: one way to build (small) capacitors for analog circuits
- Temperature dependence (ϕ_T and I_S)
- Avalanche breakdown



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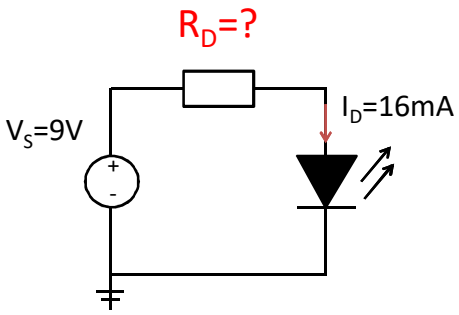
Example: Don't destroy the LED!



LED parameters:

- $I_S=10^{-18}A$
- n=1.8
- ϕ_T=26mV @ 300K

- Size the resistor R_D!
  - Use simple model with V_{Don}=0.7V
  - Use Shockley model

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Image taken from: https://docs.onion.io/omega2-starter-kit/circuit-diagram-crash-course.html

Basic but important devices

MOS(FET) transistors

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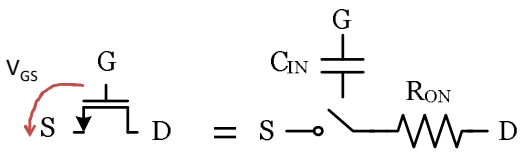
MOSFET transistor

- Metal-oxide-semiconductor (MOS)
- Field-effect transistor (FET)

$V_{GS} < V_T$: open
$V_{GS} > V_T$: closed



IT'S A SWITCH!

G = gate, S = source, D = drain, B = bulk

Image taken from: https://www.rollingstone.com/movies/lists/50-best-star-wars-characters-20151203/admiral-ackbar-20151203

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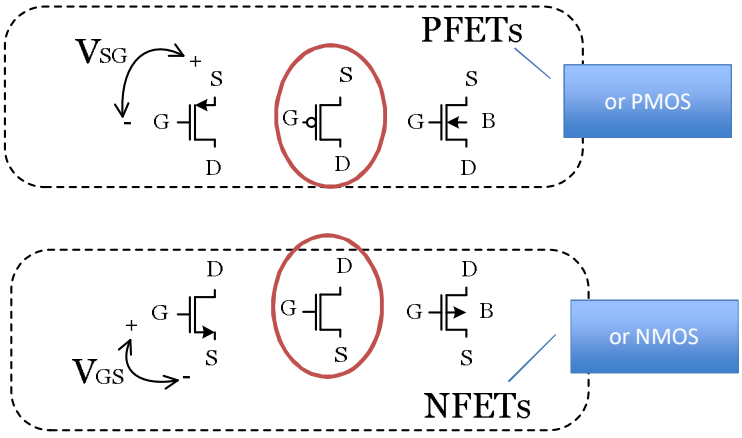
MOSFETs are 4-terminal devices



- In most cases V_{BS}=0; can be used to alter V_T

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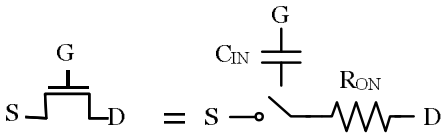
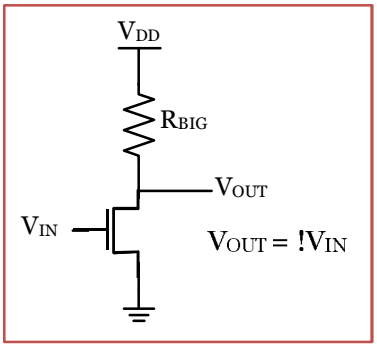
MOSFET as switches

$V_{GS} < V_T$: open
$V_{GS} > V_T$: closed





- What happens if V_{IN}=0?
- What happens if V_{IN}=V_{DD}?

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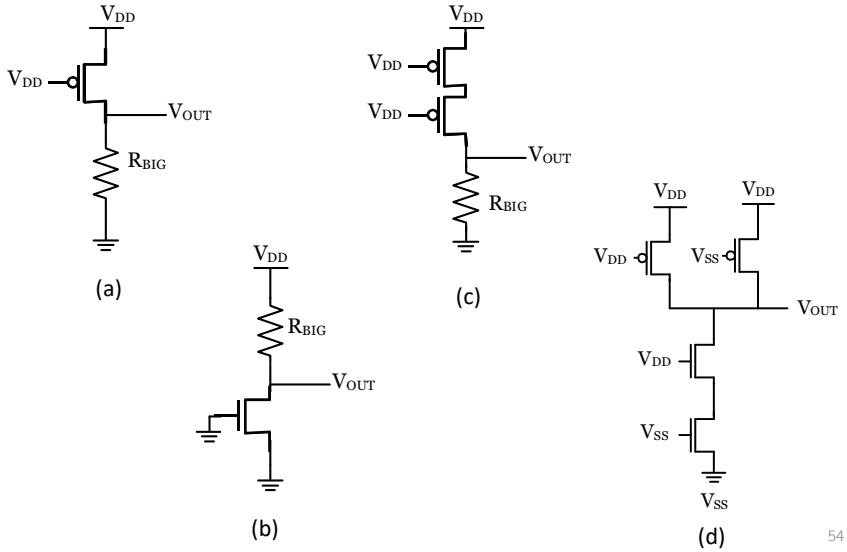
MOSFET as switches (cont'd)



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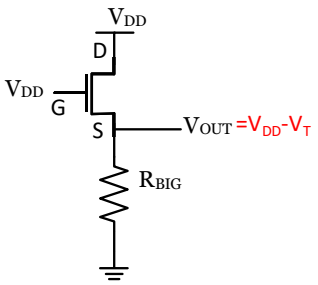
What is going on here?

- Assume that NMOS is on
- Assume that $V_{OUT}=V_{DD}$
- Then, node S would be V_{DD}
- Hence, $V_{GS}=0$ → NMOS off!



- If, however, $V_{OUT}=V_{DD}-V_T$, then transistor is on
- $V_{DD}-V_T$ is highest voltage for which that transistor can be on

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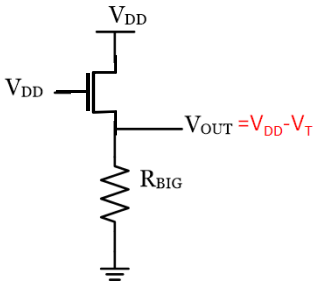
Important to remember

- NFET is a bad pull up (max $V_{DD}-V_T$)
- PFET is a bad pull down (min GND+$|V_T|$)



If V_{out} would be V_{DD}, then $V_{GS}<V_T$ and hence, NFET would be off!

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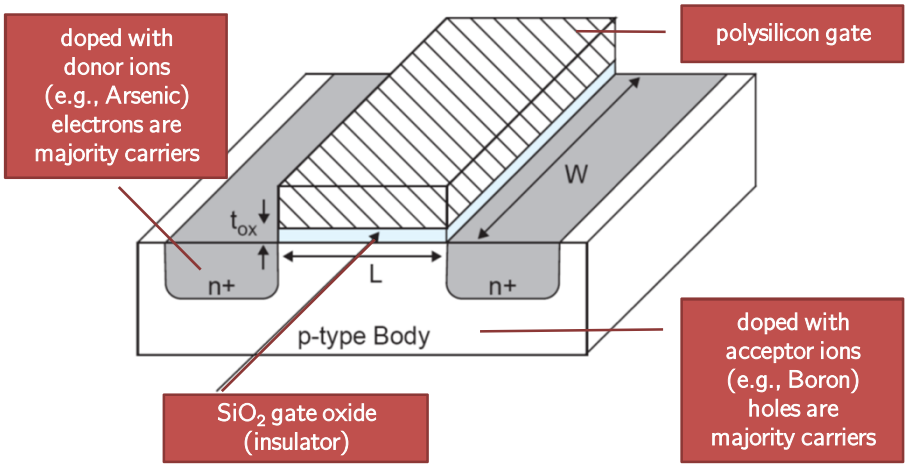
3-D view: NMOS



- Key design parameters: W = width; L = length

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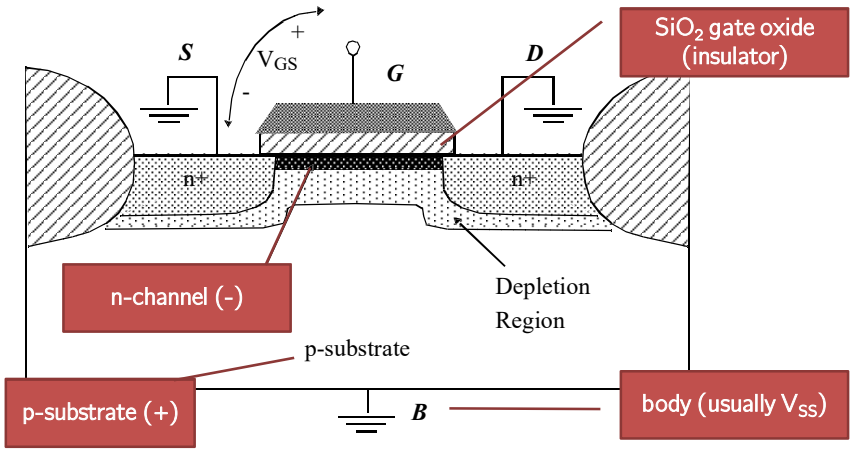
Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Harris, Weste

Depletion region: NMOS



- Situation: $V_S=V_D=V_B=0$ and $V_{GS}>0$

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Threshold voltage V_T

- Increasing gate voltage V_{GS}
  - n-channel forms below gate dielectric
  - onset of strong inversion
  - additional electrons from n+ source region
- Happens if $V_{GS}>V_T$

$$V_T = V_{T_0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

empirical parameter for $V_{SB}=0$

Fermi potential (influenced by doping)

$$\phi_F = \phi_T \log\left(\frac{N_A}{n_i}\right)$$

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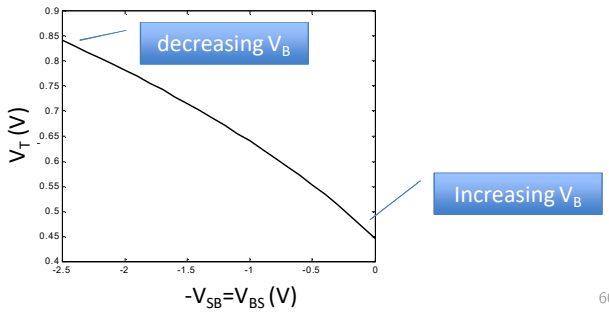
Bulk voltage affects V_T: Body effect

- Increasing V_B?
- Decreasing V_B?

called body-effect coefficient: $\gamma \approx 0.4V$

$$V_T = V_{T_0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$



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MOSFET model

Operation regions

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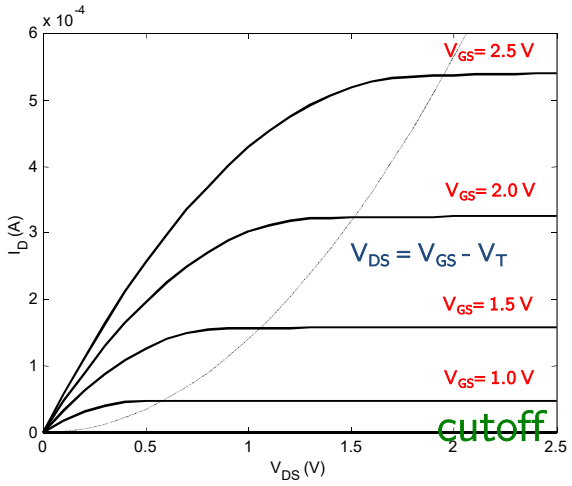
Current-voltage characteristics



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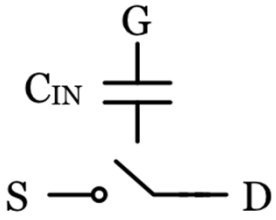
Cutoff region: $V_{GS}<V_T$

- If $V_{GS}<V_T$, then FET is (almost) off
- Ideally, open circuit between drain and source and no current flows
- $I_{DS} \approx 0A$ independent of V_{DS}



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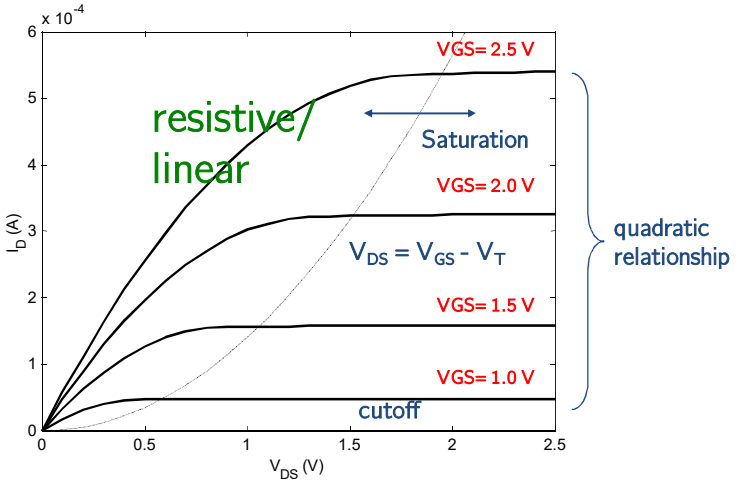
Current-voltage characteristics



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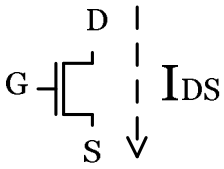
Resistive (or linear) operation region



Assume:
- V_{GS}-V_T>V_{DS}
- L large (>0.25μm)

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

- For small V_{DS} → I_{DS} is **linear** in V_{DS}

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(Origin of I_{DS})

- Charge on a capacitor:
$$Q = CV$$
- Charge on channel:
$$Q_{ch} = -C_{ch}(V_{GB} - V_T)$$
- Size of capacitor:
$$C_{ch} = \frac{\epsilon_{ox} W L}{t_{ox}}$$
- Charge in slice of channel:
$$Q(x) = -C_{ox}(V_{GS} - V_T - V(x))$$
- Current
$$I = \frac{Q}{\text{sec}}$$

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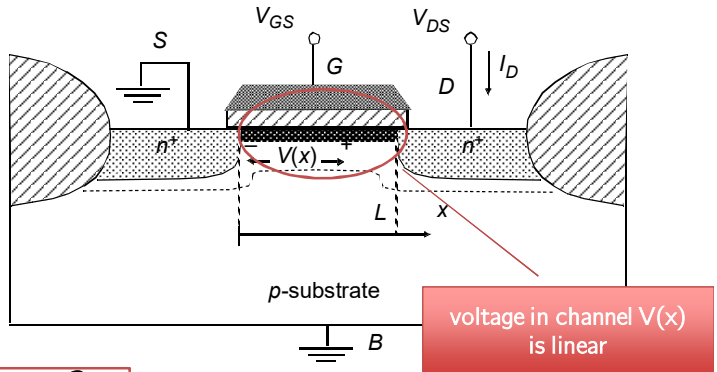
(Origin of I_{DS})



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

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(Origin of I_{DS})

- Current through channel: $I_D = -\nu(x)Q(x)W$
- Carrier velocity: $\nu(x) = -\mu_n E = \mu_n \frac{\mathrm{d}V}{\mathrm{d}x}$
- Drain Current: $I_{DS} = \mu_n C_{ox} W (V_{GS} - V_T - V) \frac{\mathrm{d}V}{\mathrm{d}x}$

$$\int_0^L I_{DS}\mathrm{d}x = \int_0^{V_{DS}} \mu_n C_{ox} W (V_{GS} - V_T - V)\mathrm{d}V$$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

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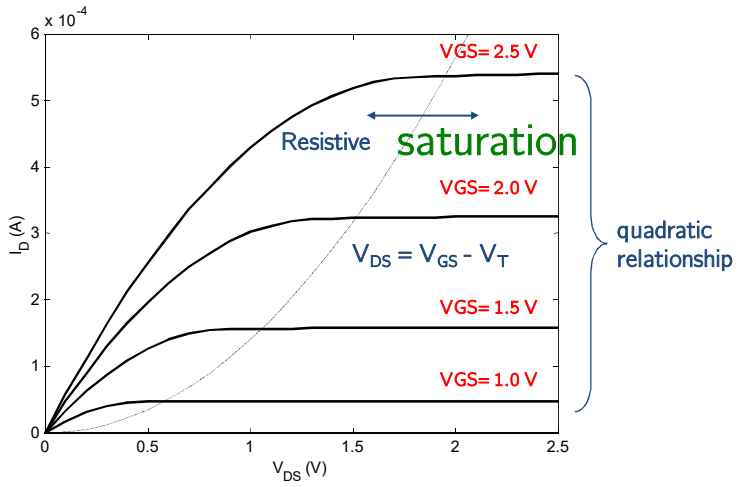
Current-voltage characteristics



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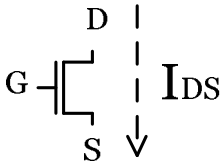
Saturation region



Assume:

- V_{GS}-V_T<V_{DS}
- L large (>0.25µm)

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\boxed{\frac{W}{L}}(V_{GS} - V_T)^2$$

- Ideally, current no longer a function of V_{DS}

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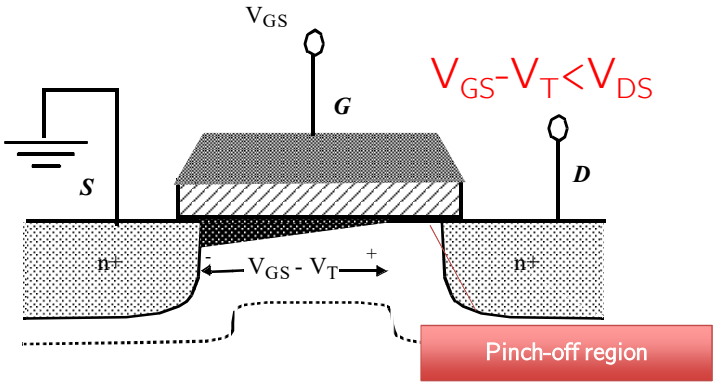
What happens in the channel?



$V_{DS}(sat) = V_{GS}-V_T$

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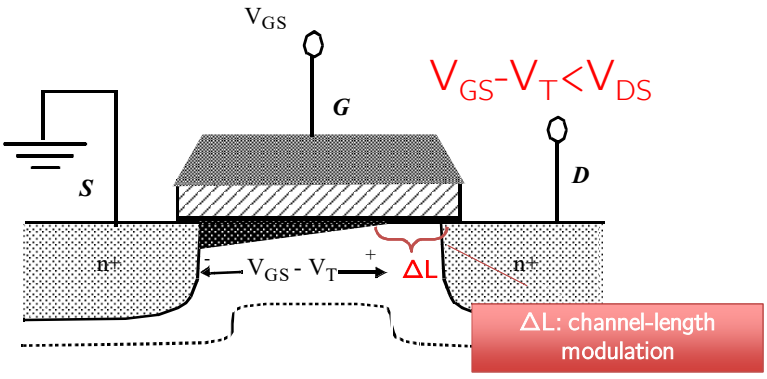
Channel-length modulation



- Effective channel length is modulated by V_{DS}
- Increasing V_{DS} reduces effective length

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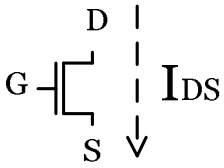
Saturation region revisited



Assume:
- V_{GS}-V_T<V_{DS}
- L large (>0.25µm)

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

- λ is an empirical parameter:
  - name: channel-length modulation
  - inversely proportional to channel length L

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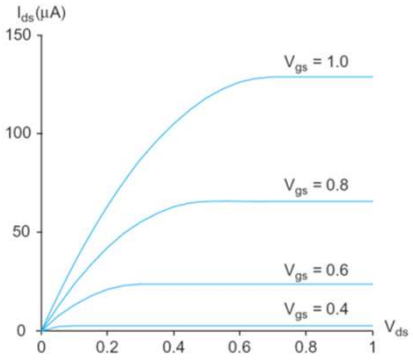
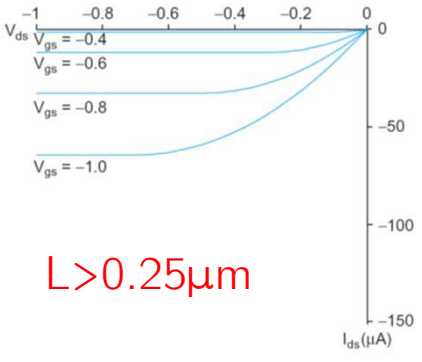
Image taken from: http://knowyourmeme.com/memes/half-life-3-confirmed

Current-voltage characteristics of long-channel devices

NMOS



PMOS



L>0.25µm

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Harris, Weste

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