ECE4740:
Digital VLSI Design

Lecture 1: Introduction

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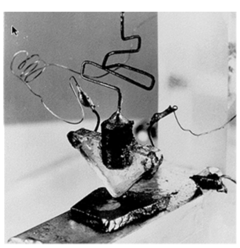
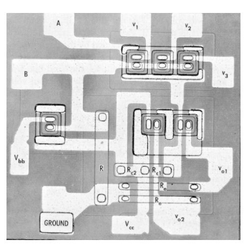
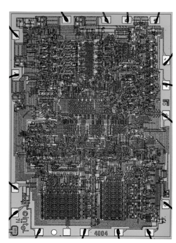
What is digital VLSI



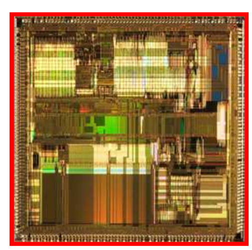
1T (1948)



6T (1960s)



1kT (1971)



1MT (1989)

- VLSI = very large scale integration
- Idea: Implement thousands (…I mean billions) of transistors on a single chip

Images taken from: http://www.computerhistory.org/collections/catalog/102618871, http://gecko54000.free.fr/?documentations=1989-04__Intel__80486

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First electronic computer: ENIAC

- ENIAC = Electronic Numerical Integrator And Computer
- 17,468 vacuum tubes
- Unreliable (longest period without failure: 116h)
- Excessive power (150kW)
- Not scalable

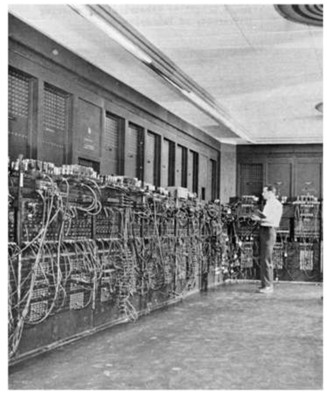

Image taken from: http://www.internetlooks.com/oncomputers.html

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First computer bug

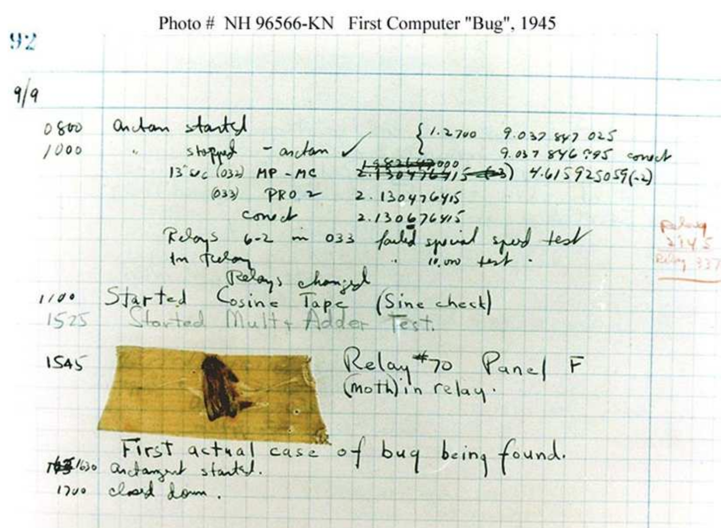

Image taken from: http://www.ksyash.com/2011/01/178/

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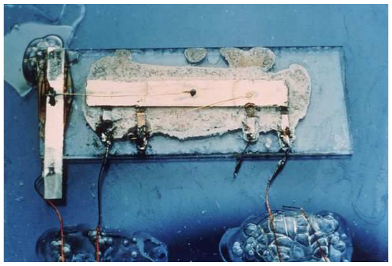
First "integrated" circuit



- Invented by Jack Kilby in 1959 (TI)
- Simple analog oscillator on a single chip
- Received Nobel Prize
- Scalable!

Image taken from: https://www.pcworld.com/article/2048664/the-legend-of-jack-kilby-55-years-of-the-integrated-circuit.html

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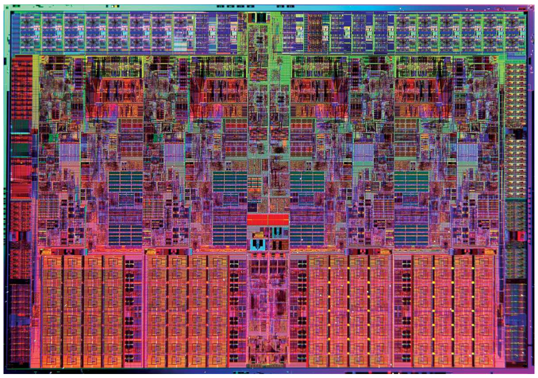
Modern digital VLSI

1BT (2002)



- Semiconductors account for about 0.5% of the world gross domestic product (GDP)
- Has much larger impact on world economy!

Images taken from: https://www.intel.com/pressroom/archive/releases/2008/20081117comp_sm.htm

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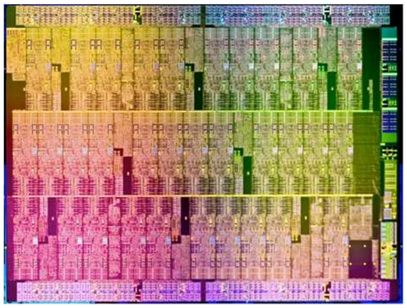
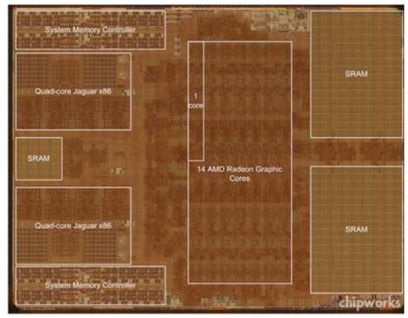
Large chips



Intel Xeon Phi processor
5B T, 62-cores, 22nm



Xbox One SOC
5B T, Microsoft/AMD, 28nm

Images taken from: https://www.extremetech.com/extreme/171678-intel-unveils-72-core-x86-knights-landing-cpu-for-exascale-supercomputing, https://www.extremetech.com/gaming/171735-xbox-one-apu-reverse-engineered-reveals-sram-as-the-reason-for-small-gpu

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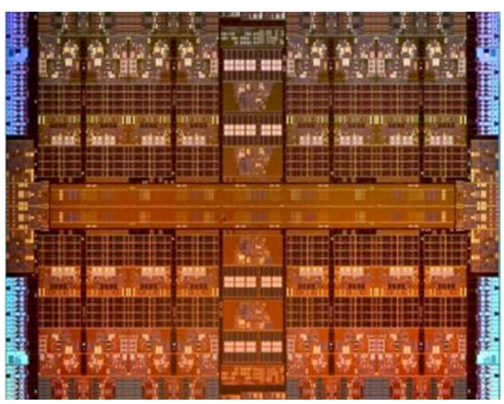
Larger chips



Oracle SPARC M7 processor
32 cores, about 10B T, 16nm FinFET

Image taken from: https://www.enterprisetech.com/2014/08/13/oracle-cranks-cores-32-sparc-m7-chip/

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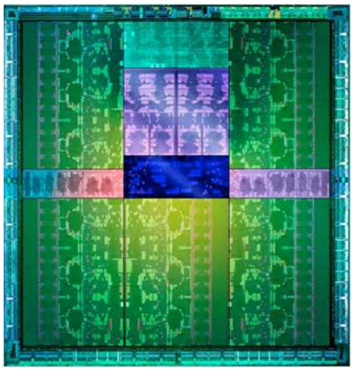
Even larger chips



NVIDIA Kepler GK110 GPU
7.08B T, 28nm

Xilinx Virtex Ultrascale
FPGA
+20B T, 20nm

Images taken from: https://www.nvidia.com/content/PDF/kepler/NVIDIA-Kepler-GK110-Architecture-Whitepaper.pdf, https://ngcodec.com/news/2013/12/16/xilinx-pulls-back-the-20nm-ultrascale-curtain

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Largest chips today: Memories

Samsung 128Gb DDR4 DIMM
about 140B T, 30nm

Image taken from:
https://www.tweaktown.com/news/24799/samsung_announces_16gb_ddr4_dimm_to_be_released_in_2014/index.html

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Do you own VLSI?

- Which devices rely on VLSI?
- What tasks are VLSI circuits doing?
- Why do you think is VLSI used?

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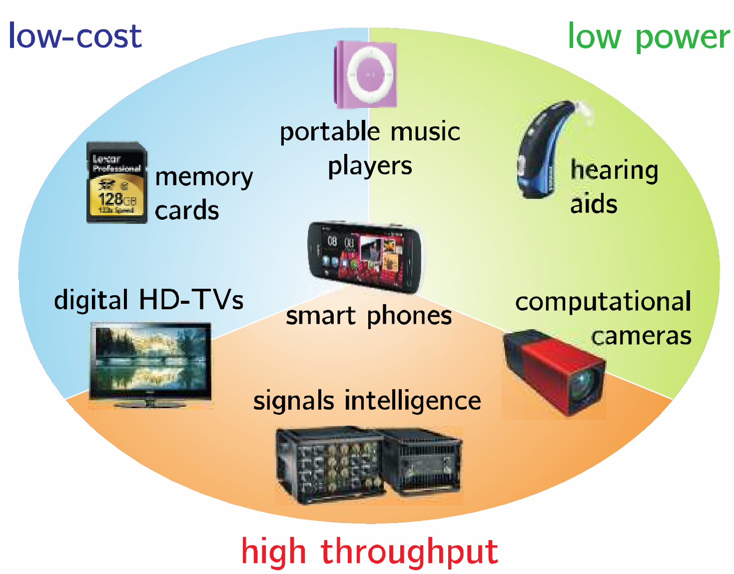
VLSI is (almost) everywhere!



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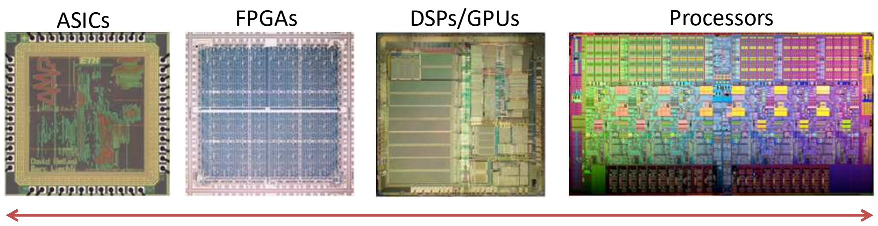
VLSI comes in different flavors

- Application specific integrated circuits
- Programmable logic (e.g., FPGAs)
- Dedicated processors (e.g., DSPs, GPUs)
- General-purpose processors



Images taken from: https://spectrum.ieee.org/tech-history/silicon-revolution/chip-hall-of-fame-xilinx-xc2064-fpga, http://www.cpu-world.com/forum/viewtopic.php?p=178537, https://phys.org/news/2010-03-intel-xeon-center-processor.html

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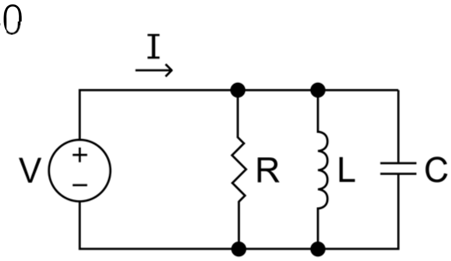
Prerequisites

- ECE2300 or solid digital logic understanding
- ECE3150 or solid understanding of CMOS

- Key concepts from ECE3150 will be recovered in ECE4740

- Remember basic RLC circuits!!!



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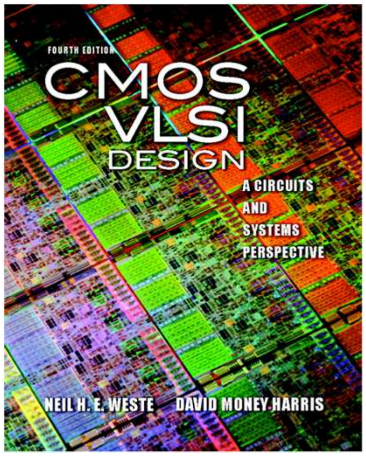
Primary textbook



Neil E. Weste

David M. Harris

CMOS VLSI Design: A Circuits and Systems Perspective

4th Ed., Pearson

Image taken from: http://pages.hmc.edu/harris/cmosvlsi/4e/index.html

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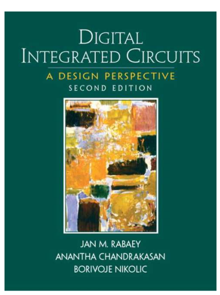
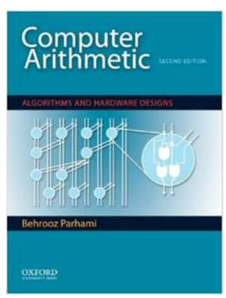
Optional textbooks





- For those who want to learn more (details)
- For those who plan to do a PhD in VLSI

Images taken from: https://sites.google.com/site/oftaitumo/digital-integrated-circuits-2nd-edition-5242536, https://www.ece.ucsb.edu/~parhami/text_comp_arit.htm

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DO NOT CHEAT!

Cornell Code of Academic Integrity:
http://cuinfo.cornell.edu/Academic/AIC.html

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What is ECE4740 all about?

Course outline and goals

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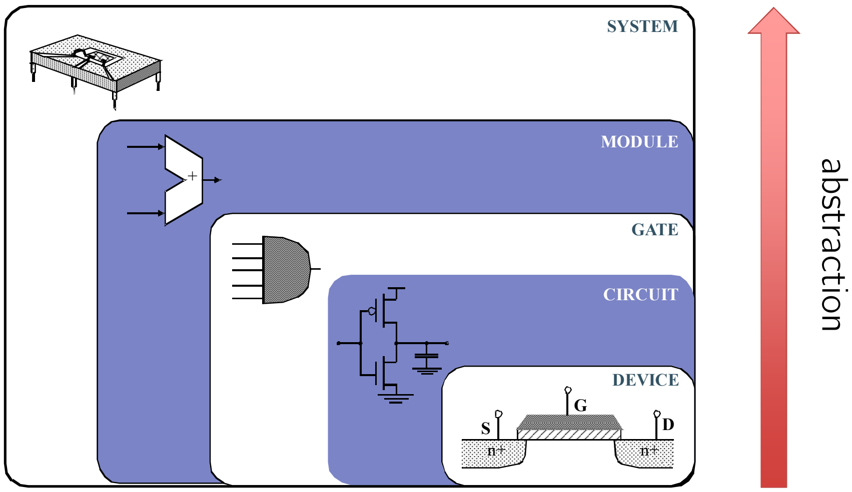
Course overview



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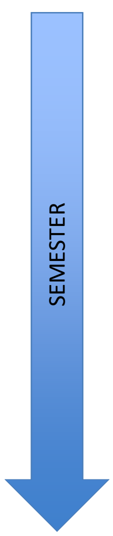
Topics covered



- Standard-cell design
- Full-custom layout
- Logic families
- Combinational and sequential logic
- Timing & clock distribution
- Computer arithmetic
- Architecture transforms
- Memories (DRAM/SRAM)
- Low-power design strategies

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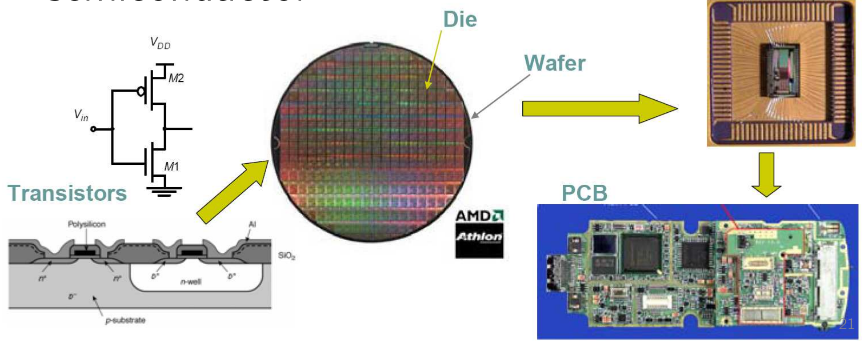
What is digital VLSI?

- Digital integrated circuits: many transistors (thousands to billions) on a single chip
- CMOS = complementary metal oxide semiconductor



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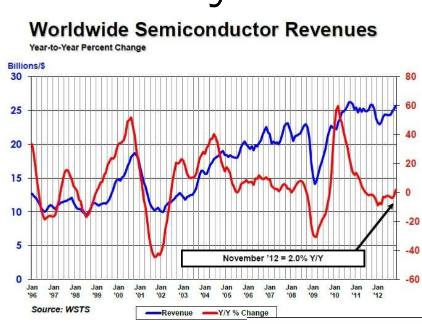
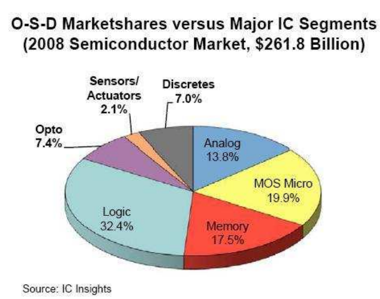
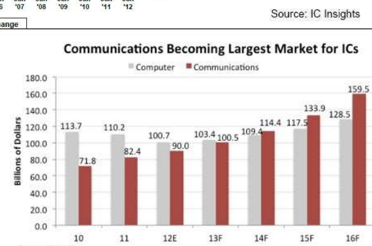
Why should I study VLSI?







Images taken from: https://www.forbes.com/sites/jimhandy/2014/01/15/sia-record-world-semiconductor-revenues-in-november/#5a8f0e573ed0, http://electroiq.com/insights-from-leading-edge/2012/11/

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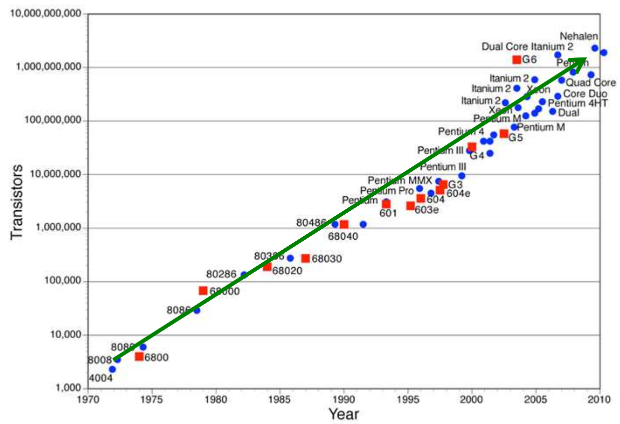
Moore's Law (1965)

- # of transistors doubles every 18 months

Gordon Moore



Images taken from: http://entrepreneurhalloffame.com/gordon-moore/, https://cielotech.wordpress.com/2016/06/10/moores-law/

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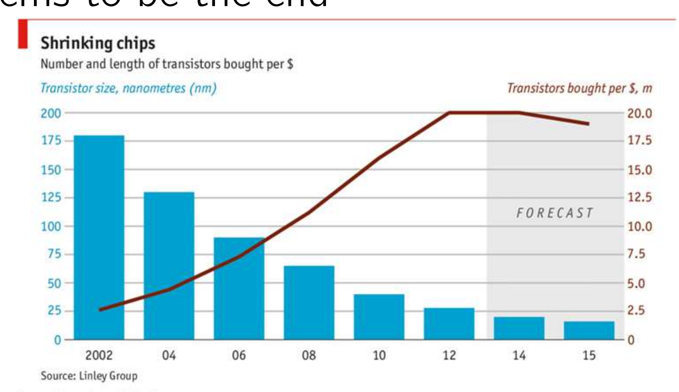
Will Moore's Law end?

- 10nm with standard silicon technology seems to be the end*



*for now

Image taken from: https://www.pragcap.com/is-this-the-end-of-moores-law/

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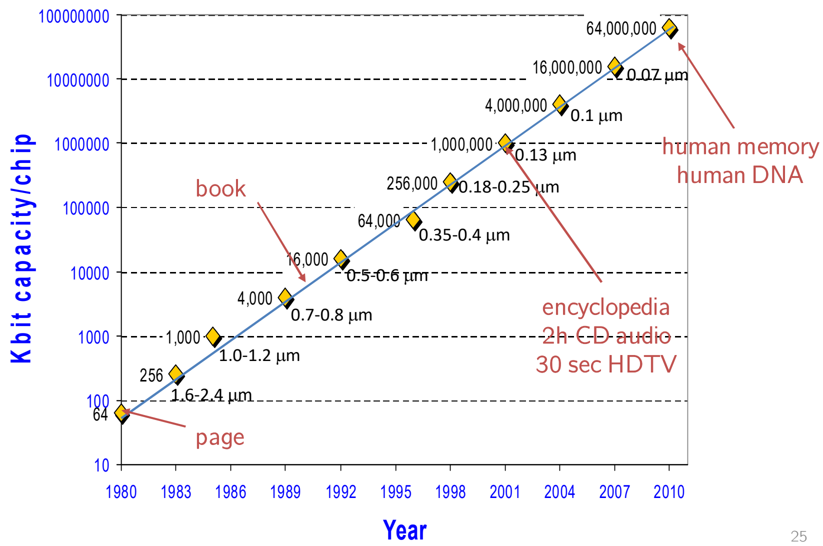
Evolution of DRAM capacity



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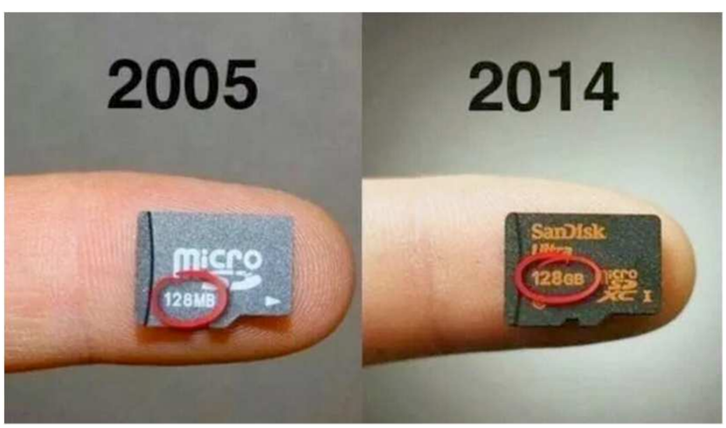
Impressive "example:" Flash memory



What's interesting about this?

In 2017, we had 400GB!

Image taken from: https://www.gsgtelco.com/2014/05/02/the-leap-in-memory-technology-from-2005-to-2014/

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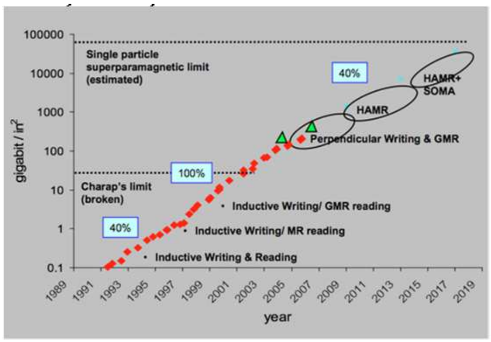
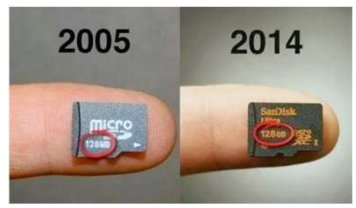
Kryder's Law

- 10 years have about 6.66x 18 months
- Moore's law only predicts 2^(6.66) ≈ 101
- But storage density increased 1000x in 1

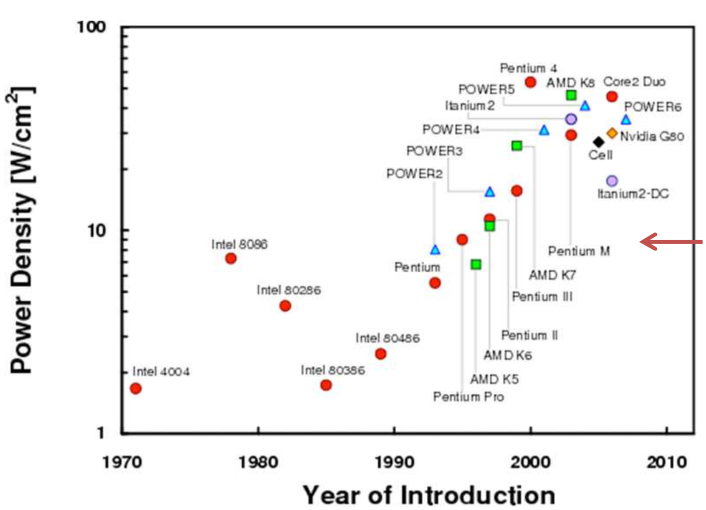




Images taken from: https://www.gsgtelco.com/2014/05/02/the-leap-in-memory-technology-from-2005-to-2014/, http://blog.dshr.org/2016/05/talk-at-seagate.html

Power dissipation

nuclear reactor



hot plate

Image taken from: http://celsiainc.com/blog-btx-desktop-pcs-a-thermally-superior-system-design-that-failed-horribly/

Can we master these challenges?

- Moore's Law is slowing down, demands for more data and processing still increasing
- Need to design increasingly complex ICs but we also have to ensure they work 100%
- Require denser and faster memories
- Circuits must be low-power

- This class will teach you the foundations to find solutions to these challenges!

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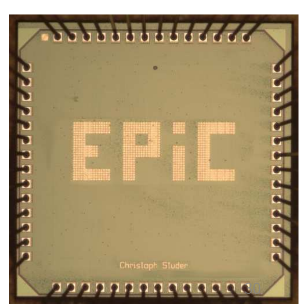
Course goals

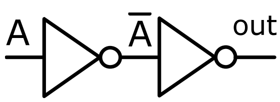
- Know how to design basic building blocks
- Learn to develop digital ICs across several layers of hierarchy via abstraction
- Hands-on experience with state-of-the-art software: Cadence Virtuoso
- Develop strong intuition

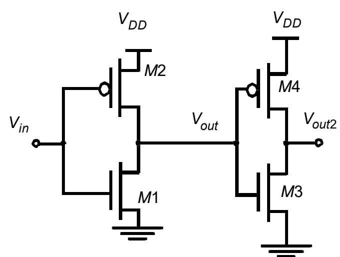
- Most important: enjoy VLSI design!

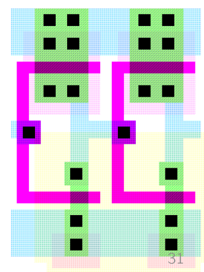


Main focus: Full-custom design

- High-performance or "high-volume" ICs
  - Example: flagship Intel microprocessors
  - Fundamentals for computer architects
  - Used in data converters (DACs/ADCs)
  - RF engineers







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Advantages and disadvantages

- Full-custom design gives full control over all possible design parameters:
  - (potentially) lower power
  - (potentially) lower area
  - (potentially) higher throughput
  - (potentially) higher yield
  - (potentially) more fun
- Drawback:
  - A lot of (tedious) work
  - Difficult to quickly develop large designs
  - Design tools are getting better and better

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Why aren't we just using CAD tools?

- Ex.: Synposys DC enables the design of high-performance complex VLSI designs
  - You write Verilog/VHDL and compile
  - Results are hard to beat by hand (especially for inexperienced users)

Even with such tools, you must understand the fundamentals

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Why? – an academic perspective

- Top journals/conferences in solid-state circuits and VLSI require fabricated chips
- ISSCC, the flagship conference, favors designs with transistor-level schematics

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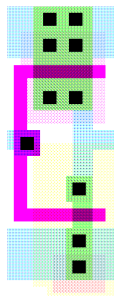
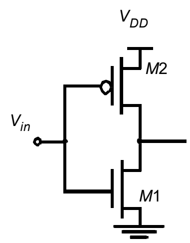
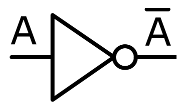
There are different abstraction layers



layout view



schematic view



logic symbol

A	NOT A
0	1
1	0

truth table

- We are going to use all these abstractions

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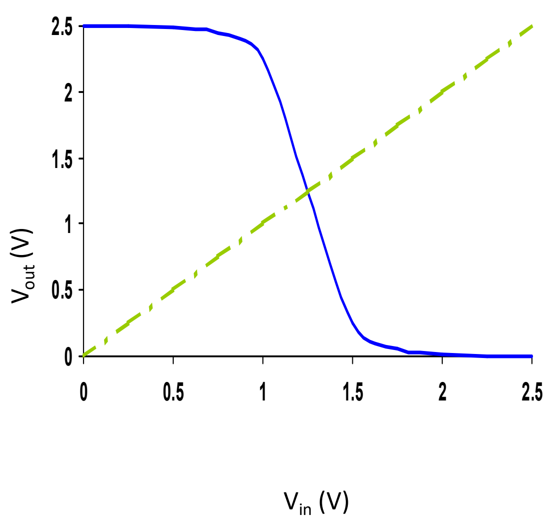
Wait, there is more!

- Voltage transfer characteristic (VTC)



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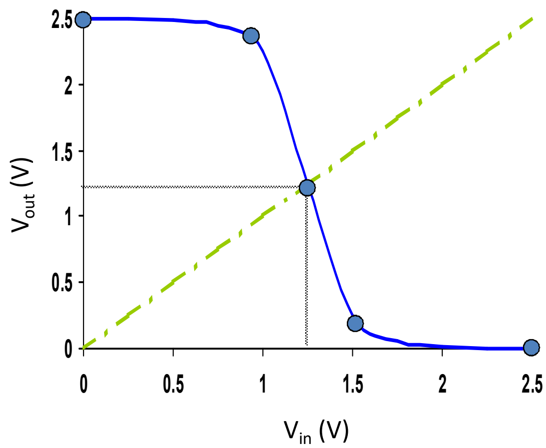
MOS operating regimes



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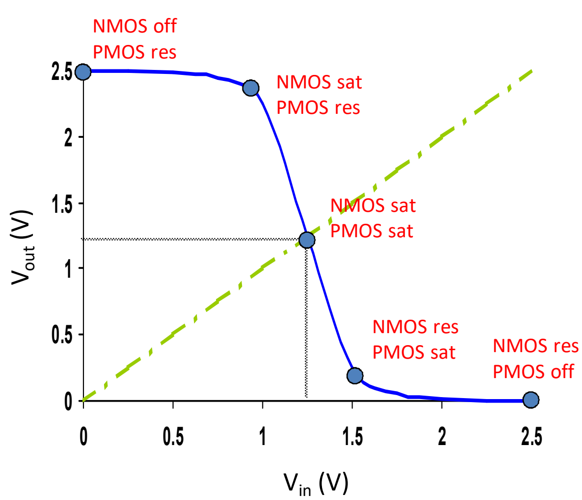
MOS operating regimes (cont'd)



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