Lab 4: Design of a 16-bit Adder

Report Due Date: April 20, 2018 at 11:59pm

- The goal of this lab is to design a 16-bit adder
- You will optimize the adder design for speed and area
- An important part of this lab is to verify the functionality and characterize performance of the adder

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1 Design of a 16-bit adder

Your goal is to design a **16-bit adder** according to the specifications shown in the grading section and under the following constraints:

1. Your adder must include a carry-in for the least-significant bit (LSB) and a carry-out for the most-significant bit (MSB).
2. All output bits, including the final carry-out, must drive a load of 10 fF.
3. Input signals have a 10 ps rise and fall time. Create a Verilog-A block to generate the input signals for the worst-case and best-case transitions (instead of analogLib components). Also use Verilog-A to generate other test input signals to verify the functionality of your adder design.
4. VDD = 1.2V and the standard operation temperature **cannot** be changed.

Hints:

- You may use the `clock_gen` file of Lab 2 as a template to design the inputs for this Lab.
- There are multiple adder topologies; some simplify design and layout and also make it smaller, faster, or more energy efficient. You may have to try out different designs to maximize your score.
- You are allowed to size the transistor widths however you want.
- Spend effort on finding the worst-case delay of your adder.
- Test and verify corner cases of your adder to ensure proper functionality. It may be helpful to write a script that generates the test signals in the Verilog-A block.
- You may want to organize and distribute the workload in your group.

2 Grading

Grading consists of a real-time evaluation by the Prof. or a TA, as well as the PowerPoint report. You can get up to 5 points for the real-time evaluation, 5 points for layout beauty, 5 points for circuit area, 5 points for delay, 5 points for verification and testing, and 5 points for following our instructions.

Delay, area, and beauty: The grade for delay and area will be determined using the following table:

Score	Delay	Area
5	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 500\text{ps}$	$\leq 800\,\mu\text{m}^2$
4	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 550\text{ps}$	$\leq 1000\,\mu\text{m}^2$
3	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 600\text{ps}$	$\leq 2000\,\mu\text{m}^2$
2	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 650\text{ps}$	$\leq 4000\,\mu\text{m}^2$
1	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 700\text{ps}$	$\leq 8000\,\mu\text{m}^2$
0	otherwise	otherwise

For the area, a square bounding box around your adder design is what matters. For the layout, we check whether you use the basic guidelines (such as sufficiently large supply wires) to create compact digital standard cells.

Verification and testing: Fully test and verify the functionality of your design through MATLAB as you have learned in Lab 2. You should add a few slides explaining the following items:

- How you compute/extract/identify the worst-case propagation delay
- How did you verify the functionality of your adder? Does your adder really add any pair of numbers correctly? Does the carry in and carry out work properly?

Real-time evaluation: An evaluation time will be scheduled with the Prof. or a TA. First, we will verify the delay, area, energy, DRC, and LVS. Then, we will ask questions about your design choices or conceptual questions (e.g., how do the load capacitors, supply voltage, or transistor sizes affect your benchmark metric). We will also ask you how you verified and measured your adder solution.

You will receive an individual grade of 0-5 based on the evaluation:

5: Demonstrated good capacity and understanding

3: Demonstrated some capacity and understanding

1: Did not demonstrate capacity or understanding

Follow the directions: If you follow all of our instructions, then you will get 5 points! If you fail on one of these, you get zero points.

- Complete the PowerPoint report template posted on blackboard. Make sure your schematics and plots are clear and legible. You can label Cadence screenshots or draw the schematics in a program of your choice. Be sure that you clearly label your screenshots, plots, and schematics. The objective is to create a concise report that could be evaluated quickly. Finally, convert the report into a pdf file.

  Do not forget to include one slide explaining your design choice(s).

- Turn in a *single* zip file containing your schematics, symbols, and the report. Name the zip file Lab4-Group(groupnumber).zip without the parentheses. Also have your report converted to pdf and be sure to include all specified files in your zip file. Also make sure none of your files are corrupted. What we cannot open, we will not grade.
- The report is due on April 20, 2018. There will be only one submission attempt allowed.

Important: We are going to randomly try out 5 out of all the submitted designs and compare it to the reported numbers. In case you fudge on benchmark numbers, and the schematics and symbols are not submitted, the entire group gets penalized by 20%. In addition, we are going to use the performance numbers of the submitted design.