Homework 3

Deliver to Homework Dropbox in PHL 2nd floor, April 13, 2018 no later than 6:00pm

Name: _____ NetID: _____

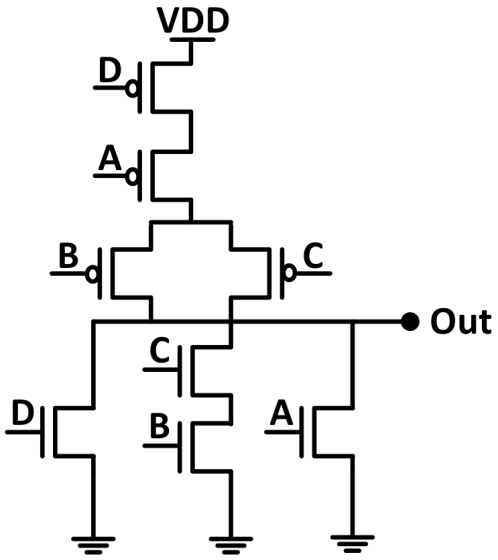
Important: You may collaborate with other students on this homework assignment, but each student must turn in their own assignment and in their own writing. In addition, you must specify the names of all your collaborators and all the resources used to solve the homework assignment. ***Failing to specify your collaborator(s) or resources will result in a 20% penalty***. Late homework will receive a 20% penalty for every day late (including submissions made after 6:30pm); homework more than 3 days late will not be accepted.

Get bonus points! Follow these instructions to receive **5 bonus points**: Put your name and NetID on the first page. All your answers must be within the blank spaces of this homework. You have to print the homework two-sided and staple it *once* prior to submission in the top-left corner. Staple your homework after you have finished it, to avoid having folded corners. In the exceptional case you have source code, Cadence schematics, or plots you want to include in your submission, you are allowed to add *one* printed page per plot *after* the associated question; do not forget to clearly label each additional sheet. Do not use extra staples or glue additional pages to your work! ***Clearly mark all your final answers.***

Question	**Maximum Points**	**Points**
1	20	
2	25	
3	35	
Follow the rules	+5 bonus	
Total	**80 (+5 bonus)**	

Problem 1: Power consumption in Logic (20pts)

1. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices such that the output resistance is same as that of an inverter with PMOS $W/L = 2$ and NMOS $W/L = 1$. (5pts)



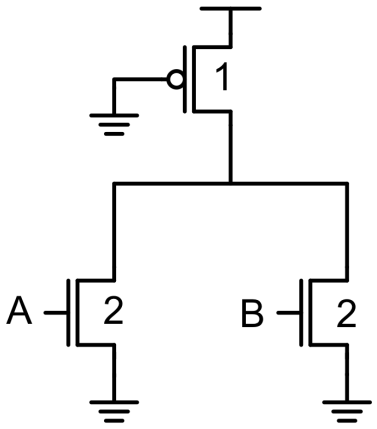
2. What input pattern(s) give the worst & best delays for t_{pHL} and t_{pLH}? Consider all internal node capacitances but neglect the Miller effect. Specify the capacitance value of each internal node. Clearly write the initial input state and the final input state. (5pts)

3. Calculate the logical effort for all the inputs. What is the intrinsic delay of the gate? (5pts)

4. What is the power dissipation of the logic gate assuming the following input probabilities: $p_{A=1} = 0.5$, $p_{B=1} = 0.2$, $p_{C=1} = 0.9$, $p_{D=1} = 0.75$. Assume VDD = 1.2 V, $C_{out} = 10$fF and $f_{clk} = 0.5$ MHz. Neglect internal node capacitances. Don't forget to write intermediate steps and the required formulas. (5 pts)

Problem 2: Pseudo-NMOS Logic (25pts)

$V_{DD} = 1\text{V}$	$L = 120\text{nm}$	$\lambda = 0$
$V_{\text{tn}} = 250\text{mV}$	$V_{\text{dsatn}} = 100\text{mV}$	$k'_{\text{n}} = 250\mu\text{A/V}^2$
$V_{\text{tp}} = -250\text{mV}$	$V_{\text{dsatp}} = -220\text{mV}$	$k'_{\text{p}} = 190\mu\text{A/V}^2$



1. Calculate the logical effort at both inputs and the intrinsic delay. Assume a unit inverter has NMOS $W/L = 1$ and PMOS $W/L = 2$. (5pts)

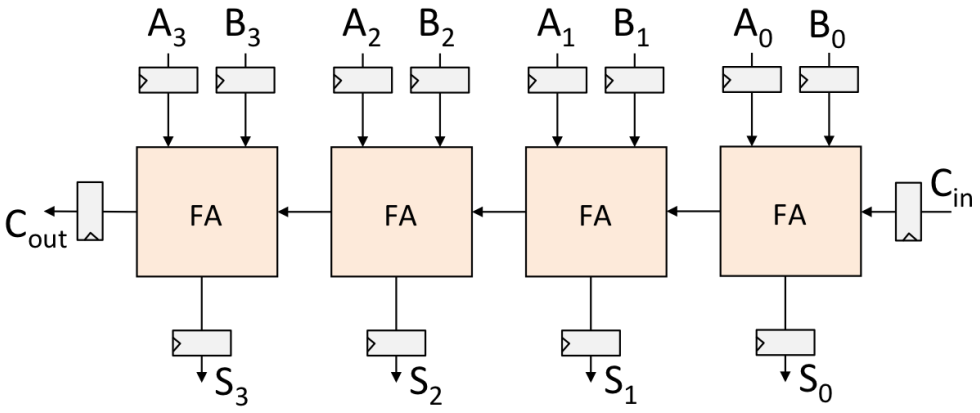
2. Find the output voltage when $A = 1$ and $B = 0$ (5pts) *Hint: Use software to solve for V_{DS}*

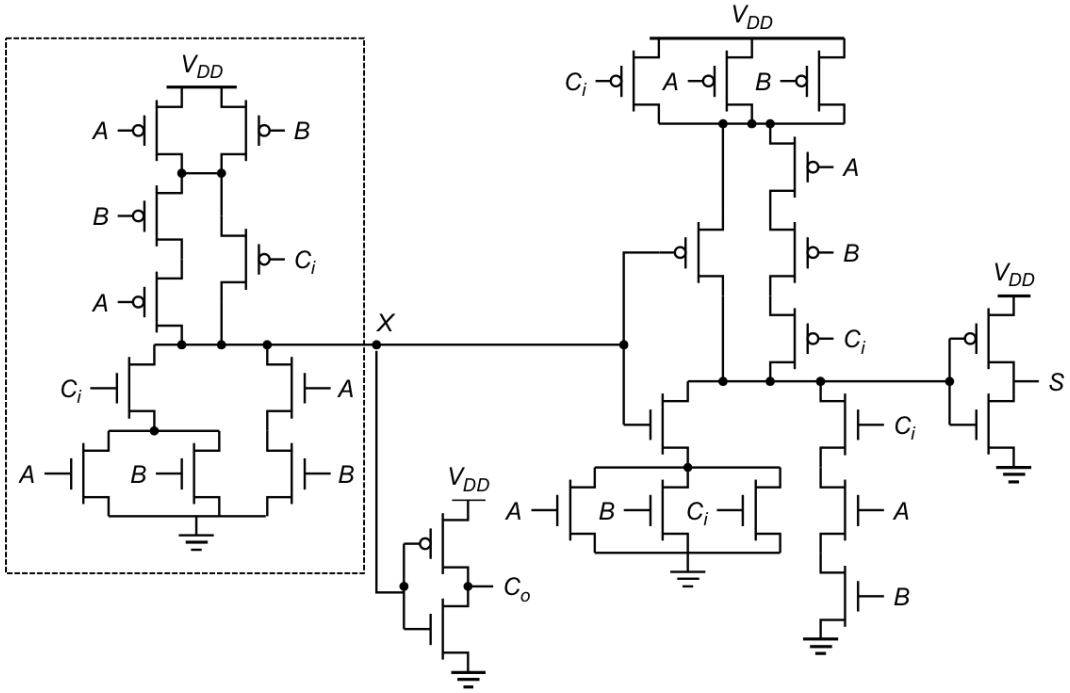
3. Find the output voltage when $A = 1$ and $B = 1$ (5pts)

4. Confirm parts 2 and 3 with Cadence simulations. Report the bias current for each case and show the Cadence schematic with DC operating points annotated. For DC operating points show id, vgs, vds, vth, and region. To change the default display options, go to View→Results Annotation Setup, and check parameter. Click on the relevant device (you must do this for NFETs and PFETs) and under "Parameter Labels" select "cell," "operating point," and "dc". (10pts)

Problem 3: Area-Delay Trade-off of a 4-bit Ripple Carry Adder (35pts)

Consider the 4-bit ripple carry adder (RCA) consisting of four static CMOS full adders (FAs) shown below. In this problem, we are interested in the area A and delay D of 3 different RCA designs. For simplicity, the circuit area is measured in terms of $A = \sum_i S_i$, where S_i is the sizing factor of transistor i and the sum is over all transistors in the FA design; the area of each flip-flop is $A_{ff} = 60$ (also measured in sizing factors). For combinational gates, the delay D is measured only in terms of the intrinsic delay of the gate (ignore the logical effort, electrical effort, fan out, etc.). All flip-flops are assumed to have setup time $D_{ff,su} = 12$ and propagation delay $D_{ff,pd} = 6$. Assume that there is no clock skew and the hold conditions are all met.





1. Size the FA such that the gate in the dashed box has a PMOS:NMOS ratio of 4 : 2 and the rest PMOS : NMOS = 2 : 1. Find a sizing solution that results in the minimum circuit area. Use minimal transistor lengths (i.e., 1) and only use integer-valued sizes for the widths. Compute the area of one FA, A_{FA}, as well as the delays from the inputs to the carry and sum outputs of the FA $D_{FA,C}$ and $D_{FA,S}$, respectively. (10pts)

2. Compute the area A_1 of the entire RCA (including all flip-flops). Find the critical path of the RCA and compute the total delay D_1. Draw a so-called AT-diagram, where the x-axis shows the delay and the y-axis the area; add the point (D_1, A_1) to this diagram. (10pts)

3. Use the inversion property discussed in class to reduce the critical path of the 4-bit RCA. Draw the resulting block diagram (similarly to the RCA above). Compute the critical path D_2 and the area A_2 of the resulting (hopefully improved) RCA. Add the resulting (D_2, A_2) point to your AT diagram. (5pts)

4. Insert one pipeline stage into the optimized RCA such that the critical path is minimized. Compute the critical path D_3 and the area A_3 of the resulting, pipelined RCA, and add this design to your AT diagram. (5pts)

5. The AT-efficiency of VLSI designs is commonly measured in terms of the AT product $A \cdot D$ (small is better). Which of your designs is the most efficient? Perform retiming of the introduced pipeline stage. Can you improve the AT efficiency of your design? (5pts)