Homework 2

Deliver to Homework Dropbox in PHL 2nd floor, March 9, 2018 no later than 6:00pm

Name: _____ NetID: _____

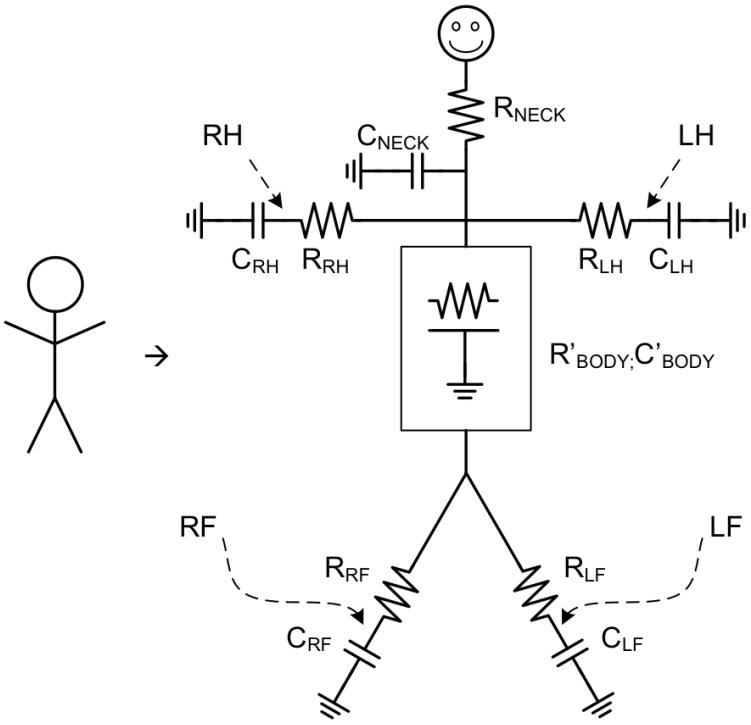
Important: You may collaborate with other students on this homework assignment, but each student must turn in their own assignment and in their own writing. In addition, you must specify the names of all your collaborators and all the resources used to solve the homework assignment. Failing to specify your collaborator(s) or resources will result in a 20% penalty. Late homework will receive a 20% penalty for every day late (including submissions made after 6:00pm); homework more than 3 days late will not be accepted.

Get bonus points! Follow these instructions to receive **5 bonus points**: Put your name and NetID on the first page. All your answers must be within the blank spaces of this homework. You have to print the homework two-sided and staple it *once* prior to submission in the top-left corner. In the exceptional case you have source code, Cadence schematics, or plots you want to include in your submission, you are allowed to add *one* printed page per plot *after* the associated question; do not forget to clearly label each additional sheet. Please do not put extra staples or glue additional pages to your work. ***Clearly mark all your final answers.***

Question	**Maximum Points**	**Points**
1	20	
2	20	
3	20	
4	20	
5	20	
Follow the rules	+5 bonus	
Total	**100 (+5 bonus)**	

Problem 1: Elmore (20pts)

You can model your friend Elmore as an RC network. You want to know the time it takes for neural signals from his brain to propagate down his spinal cord to his extremities.



1. Find the Elmore delay to his hands and feet assuming you inject a pulse just above his neck. Assume $R_{\text{BODY}} = R'_{\text{BODY}} \cdot L_{\text{TORSO}}$ and $C_{\text{BODY}} = C'_{\text{BODY}} \cdot L_{\text{TORSO}}$. (Four equations; 10pts)

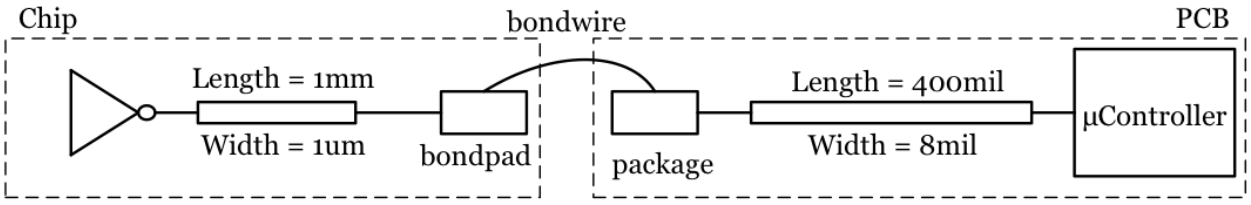
2. A terrible tragedy has befallen Elmore (while going to Collegetown without proper footwear) resulting in the loss of sensation to his feet. Rewrite the time constant to his hands and from his left foot (LF) to his right foot (RF). Assume that there is a break in the distributed-RC line of Elmore's body: let L_{UP} be the distance from his neck to the break and L_{DOWN} be the distance from the break to his waist, i.e., we have $L_{\text{TORSO}} = L_{\text{UP}} + L_{\text{DOWN}}$. (Three equations; 10pts)

Problem 2: Pad driver (20pts)

You need to transmit some analog-to-digital converter (ADC) data off-chip into a microcontroller but you are space-constrained. Design the smallest inverter while ensuring that the propagation delay from the inverter to the microcontroller is minimal.

- Assume that the width of the PMOS is twice as that of the NMOS
- Ignore channel-length modulation
- Assume C_{diff} and C_{gd} scale linearly with the width
- Note that mil $\neq$ mm

$R_{\text{on}} = \frac{3}{4} V_{\text{DD}} / I_{\text{dsat}}$	$V_{DD} = 1.8\text{V}$	
$V_{\text{dsatn}} = 0.63\text{V}$	$V_{\text{dsatp}} = 1\text{V}$	$V_{\text{Tn}} = \lvert V_{\text{Tp}} \rvert = 0.35\text{V}$
$k'_{\text{n}} = 0.12\text{mA/V}^2$	$k'_{\text{p}} = 0.03\text{mA/V}^2$	$L_{\text{n}} = L_{\text{p}} = 250\text{nm}$
$C_{\text{diff}} = 0.5\text{fF}/\mu\text{m}$	$C_{\text{gd}} = 0.2\text{fF}/\mu\text{m}$	
$R'_{\text{Chip}} = 20\text{m}\Omega/\square$	$C'_{\text{Chip}} = 0.1\text{fF}/\mu\text{m}^2$	
$C_{\text{bondpad}} = 200\text{fF}$	$R_{\text{bondwire}} = 1\Omega$	$C_{\text{package}} = 1\text{fF}$
$R'_{\text{PCB}} = 10\text{m}\Omega/\square$	$C'_{\text{PCB}} = .1\text{fF/mil}^2$	
$C_{\text{microcontroller}} = 100\text{fF}$		



1. Draw the circuit model for the delay line and write out the Elmore delay symbolically for both t_{pHL} and t_{pLH}. (10pts)

2. Find the smallest width PMOS and NMOS to the nearest 0.1μm for t_{pHL} and $t_{\text{pLH}} <$ 1ns. Write a MATLAB or Python script to solve this problem; include a print out of your source code with your answers. (10pts)

Problem 3: Half-adder (XOR) (20pts)

A	B	out
0	0	0
0	1	1
1	0	1
1	1	0

1. Draw the schematic of the logic function above using only static complementary CMOS logic (do not use pass transistors or other logic styles). Try to find a solution with a minimal number of transistors. (10pts) *Hint: You may need multiple (and possibly different) gates to realize the entire half-adder.*

2. Extract the logic graph(s) and find consistent Euler path(s). (5pts)

3. Draw the stick diagram(s) and connect them if necessary. This is a lot of fun! (5pts)

Problem 4: Random logic (20pts)

1. Implement the equation $Y = [(\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D} + \overline{E}) + \overline{F}] \cdot \overline{G}$ using a single, monolithic CMOS gate. (5pts)

2. Size the devices such that the output resistance is the same as an inverter with NMOS $W/L = 2$ and PMOS $W/L = 4$. Try to find a sizing solution that minimizes the overall area of the logic gate (without penalizing the delay); only use integer sizes. (5pts)

3. Find the input pattern for the worst-case delay for pull-up and pull-down. Defend your answer with math and words (1-to-2 sentences). Also find the Elmore delay for the worst-case, given your sized transistors. (5pts)

4. Find the input pattern for the best-case delay for pull-up and pull-down. Defend your answer with math and words (1-to-2 sentences). Also find the Elmore delay for the best-case, given your sized transistors. (5pts)

Hint: For part 3 and 4, assume for simplicity that all node capacitances are equal to C. This is not correct in practice, but useful to get a first-order estimate of the delay.

Problem 5: Seeing is Believing: More Fun with Inverter Sizing (20pts)

1. Create a 2:1 sized PMOS:NMOS inverter schematic (with minimal gate lengths) in Cadence Virtuoso, as well as a corresponding testbench, with the same specifications as Lab 1 Part 1.

2. As in Lab 1 Part 3 Problem 2, give the inverter instantiated in the testbench the property ”m,” and assign it to the variable ”mult.”

3. Perform a parametric sweep over the variable “mult” with values 1, 2, 4, and 8.

4. Plot the Voltage Transfer Characteristic (VTC), i.e., V_{in} versus V_{out} for each sizing value (multiplier). The VTCs should be in a single graph overlapping with a clear legend so the lines can be distinguished. (10pts)

5. Plot the transient response for each value, centered around a low-to-high input response and scaled to see the timing characteristics. Again, this should be on one graph overlapping with clearly labeled axes and legend. (10pts)