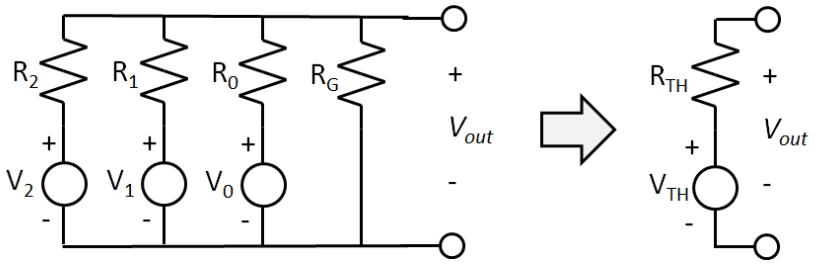
Prelab Problem 2.1: A binary-weighted resistive Digital-to-Analog Converter (DAC)

(a) Consider the circuit shown for a 3-bit DAC, and assume the following component values: $R_G = 8R$, $R_0 = 8R$, $R_1 = 4R$, $R_2 = 2R$. Applying superposition, find the Thevenin equivalent of this circuit. What is R_{TH}, in terms of R? What is V_{TH}, in terms of V_0, V_1, and V_2? (Hint: This problem is easier to solve by defining $G = 1/R$, and converting R_G, R_0, R_1, and R_2 to G_G, G_0, G_1, and G_2).

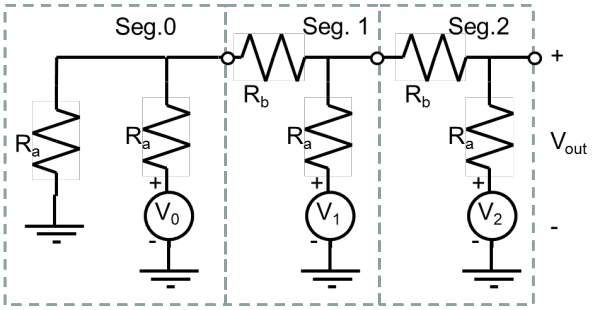


(b) For the following truth table, (where 0 means 0 V, 1 means 1 V), find V_{out} in each case.

V_2	V_1	V_0	V_{out}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(c) Based on this approach, draw a circuit for a 5-bit DAC (5 input voltages) with the same Thevenin resistance, and a Thevenin voltage of $V_{TH} = (16V_4 + 8V_3 + 4V_2 + 2V_1 + V_0)/32$.

Prelab Problem 2.2: A resistive ladder, 3-bit Digital-to-Analog Converter (DAC)



(a) Write the Thevenin equivalent of segment 0 as seen by segment 1 (that is find V_{th0} and R_{th0} in terms of V_0 and R_a).

(b) Now, find the Thevenin equivalent of the combination of segments 0 and 1, as seen by segment 2 when $V_1 = 0$. Write your solution in terms of V_{th0}, R_{th0}, R_a, and R_b, and then re-write in terms of R_a, R_b and V_0.

(c) Now, set $V_0 = 0$, and find the Thevanin equivalent of the combination of segments 0 and 1, as seen by segment 2 in terms R_a, R_b and V_1. (Hint: think "superposition")

(d) Choose the values of R_a and R_b such that $R_{th1} = 50\ \Omega$ and, by superposition, $V_{th1} = V_1/2 + V_0/4$.

(e) Now, for these values of R_a and R_b, and using the results from part (d), what is the Thevenin equivalent of the full circuit, in terms of V_0, V_1 and V_2?

(f) If this circuit were loaded with a resistance, $R_L = 100\ \Omega$, fill in the truth table below for the loaded output voltage V_{out} given the values of V_0, V_1 and V_2.

V_2	V_1	V_0	V_{out}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(g) Draw a circuit that extends this 3-bit analog-to-digital converter (DAC) into a 5-bit DAC with the same output resistance.