Sinusoidal Steady-State and Black Boxes

Goals:

1. Use understanding of sinusoidal steady-state behavior of individual components, and their combinations, to reverse engineer three different two-port black boxes. Specifically, you are given the topology of the circuit inside a black box, and you have to determine the components used and their values (in Ohms, Farads, Henrys).

Preparation:

1. Carefully review this document.
2. Review lecture slides on sinusoidal steady-state responses, especially amplitude and phase responses across frequency.
3. Complete Prelab 5.

Experiments:

You will analyze three distinct black boxes in this lab. The black boxes are labeled "easy" (E), "medium" (M), or "hard" (H), depending on how difficult it is to reverse engineer them. You must reverse engineer one "easy," one "medium," and one "hard" black box.

Each black box has three components. These components are connected to form either a T-network or a π–network, as shown in Fig. 1, and the black box is labeled with the type of network inside. Each component of the network (shown as a rectangle in Fig. 1) can be either a resistor, a capacitor, or an inductor. Resistors can be of one of the following values: 2.2 Ω, 240 Ω, 510 Ω, 1 kΩ, or 2.2 kΩ. Capacitors can be of one of the following values: 22 nF or 10 nF. Inductors have value of 1.2 mH.

You will use lab instruments, including multimeter, signal source and oscilloscope, to try to determine which three components are in each black box and their values. An exhaustive list of all possible RLC networks that might be in a black box is given at the end of this document. YOU WILL NEED TO THINK ABOUT THE MEASUREMENTS YOU ARE DOING. Don't just blindly run every possible experiment. Start with an "easy" black box and then move to "medium" and "hard."

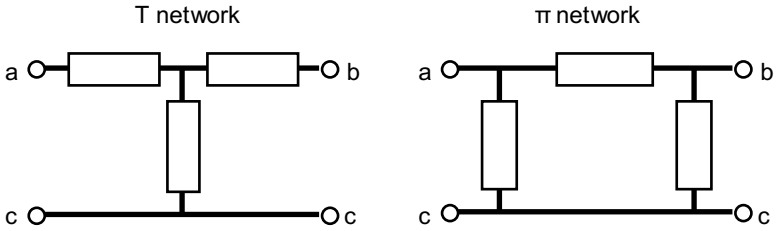

Fig. 1. T-network (left) and π-network (right) used in the black boxes.

1. **Task 1**
   Sign out a black box from the TAs. Write down the box's identification number, its difficulty level, and whether it is a "T" or "π" network in the lab report.

2. Task 2

Measure the magnitude of the impedances at dc (i.e., at 0 Hz) seen between each pair of terminals (Z_{ac0}, Z_{bc0} and Z_{ab0}), using the DMM as if you were measuring resistance, and enter these values in the lab report. Note that the two terminals marked "c" in Fig. 1 are always shorted together and are a single node.

(a) What possible component types and values do these measurements imply for each component of the network? Enter this information in the lab report. (*Hint: recall the impedance of a capacitor and an inductor at 0 Hz*).

(b) Check the exhaustive list of possible RLC topologies given at the end of this document and list those with the same general topology (T or π) that would fit the behavior you measured. Also enter this information in the lab report. (*Hint: When you measure impedance across terminals of a T-network, you are always measuring the series impedance of two components. When you measure impedance across terminals of a* π*-network, you are measuring the impedance of one component in parallel with the series combination of the other two*).

(c) **If these measurements are sufficient to completely determine your network, including the component types and values, then go to Task 6.** *(Hint: if the black box is not labeled "easy" don't jump to Task 6)*.

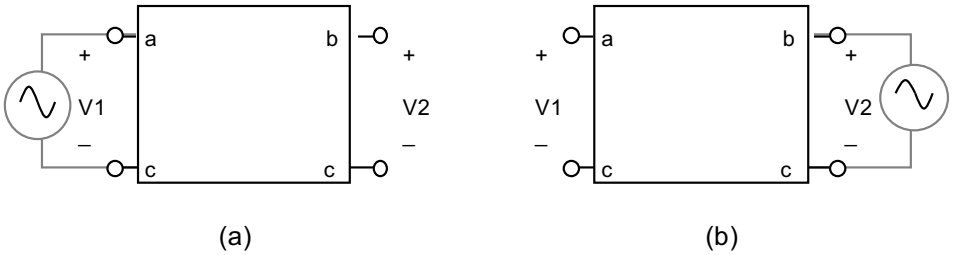

Fig. 2. Sinewave injection into: (a) port 1, and (b) port 2.

3. Task 3

Inject a 1-V 1-kHz sinewave into port 1 (i.e., across terminals a and c) using the signal source, as shown in Fig. 2(a) (set signal source amplitude to 1 V and frequency to 1 kHz). Attach oscilloscope probes across both ports, and set amplitude of both channels to be 500 mV/division, and time scale to be 250 μs/div. (Note: you can set up your signal drive and oscilloscope probes attached to a set of banana plugs, and then just move the plugs around, instead of disconnecting everything every time.)

(a) For the voltage at port 2 (i.e., across terminals b and c), record its amplitude and its phase shift relative to the voltage at port 1. Enter these values in the lab report, and also include a plot of port 1 and port 2 voltage waveforms, showing their relative amplitudes and phases. (*Hint: When you measure the sinusoidal response of a T-network, the component connected in series with the "output" does not contribute to the voltage division. When you measure the sinusoidal response of a* π*-network, the component connected in parallel with the "input side" does not contribute to the voltage division, though it may load the input if its impedance is close to or less than 50* Ω).

(b) Change the injected frequency to 100 kHz and repeat Task 3(a) (set time scale on the oscilloscope to be 2.5 μs /div). Enter amplitude and phase shift information in the lab

report, as well as a plot of port 1 and port 2 voltage waveforms, showing their relative amplitudes and phases.

(c) Connect the signal source to port 2, as shown in Fig. 2(b), and repeat Tasks 3(a) and 3(b). Enter amplitude and phase shift information in the lab report, as well as a plot of port 1 and port 2 voltage waveforms, showing their relative amplitudes and phases (do this for 1 kHz and 100 kHz).

(d) In your lab report, comment on the amplitude and phase of the voltage at the output port relative to the voltage at the input port. Also comment on any other important observations, in particular is the input voltage really 1 V, and if not, why not? Remember that the source is effectively a Thevenin equivalent with $R_{TH} = 50\ \Omega$.

(e) Can you reverse engineer the network now? Check the exhaustive list of possible RLC topologies at the end of this document and list those that fit the behavior you observed. **If the above measurements are sufficient to completely determine your network, including the component types and values, then go to Task 6**.

4. **Task 4**

Using the signal source, sweep frequency either from 10 kHz to 100 kHz in 10 kHz steps, or from 2 kHz to 20 kHz in 2 kHz steps (decide what range makes sense based on your earlier observations about the network).

(a) Measure the peak-to-peak amplitudes of the input and the output voltages (using the measurement capabilities of the oscilloscope) at each frequency and plot their ratio. At what frequency is the amplitude ratio largest? What would this imply for your network? In your lab report, include plots of amplitude ratio vs. frequency. Note for highly resonant circuits, you may want to take finer frequency steps near the resonant frequency.

(d) **If these measurements are sufficient to completely determine your network, including the component types and values, then go to Task 6**. *(Hint: in most cases you should be able to reverse engineer your network with the information you have collected)*.

5. **Task 5**

If the above tasks are not sufficient in helping you reverse engineer what is inside the back box, you can try one or more of the following:

(a) Deliberately load the circuit with a 510 Ω resistor and/or drive it through a 510 Ω resistor and repeat Tasks 3 and 4. Think through why this might help.

(b) Inject a 1-V, 1-kHz square-wave into port 1 and measure the voltage at port 2 using the oscilloscope. You can also inject the square-wave into port 2, and measure the voltage at port 1. Think through why this might help.

(c) If you are still unsure about the network inside the black box, you can build a copy of what you think is in the box, test it, and compare (but beware of bugs in your "copy").

(d) If you end up using these techniques to determine what is in the black box, include waveforms and any other relevant information in your lab report.

6. **Task 6**

In your lab report, draw the reverse engineered network, showing the component types, how they are connected and their values. Also describe how you used the information available from the earlier tasks to work out which components are connected where, and their values. Note that depending on the difficulty of the black box, you may not have to take all of the measurements described above to reverse engineer what is in the box. You need not include unnecessary measurements. (*Hint: You can get the right answer without solving for every*

component value very accurately, as there are a finite number of possible resistor and capacitor values. So "trial and error" is not a bad approach; there is no shame in this, use whatever works!)

7. **Task 7**
   Return the black box to the TAs and sign them back in (**don't just pass the boxes around**).

Wind down:

Clean up around your bench and return any components back to their storage bins. Be sure all data is collected and placed on your own storage media. Delete all files on your desktop or at least organize them in a folder. ECE makes no guarantee that these files left on your desktop will remain over time.

Analysis:

1. For each of the three black boxes that you reverse engineered, record the information required to be entered in the lab report as described under each of the tasks in the experiments section. At the very minimum, your lab report should include the following for each of the three black boxes:
   (a) Black box number, difficulty and network type (T or π).
   (b) Drawing of the reverse engineered network, showing the components types, how they are connected (internally and to port terminals a, b and c), and their values.
   (c) Description of the logic used to reverse engineer the black box, including all supporting measurements (waveforms etc.).

Appendix - Possible RLC Networks:

An exhaustive list of all possible RLC networks in this lab (not all of which have been implemented). Numbers 1- 27 are T-networks, 28-54 are π-networks.

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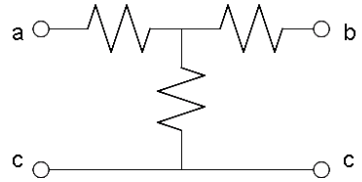

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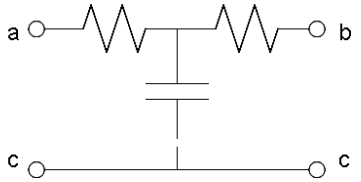

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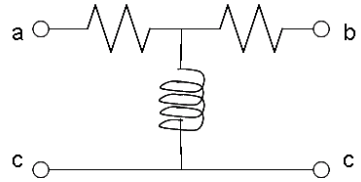

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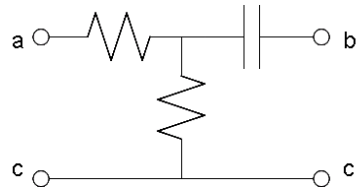

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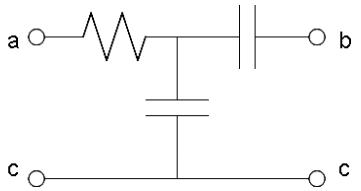

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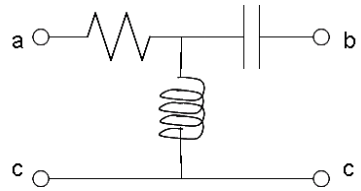

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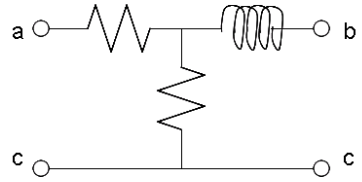

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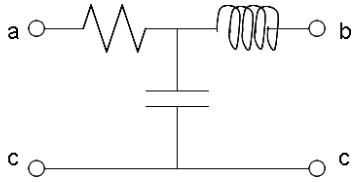

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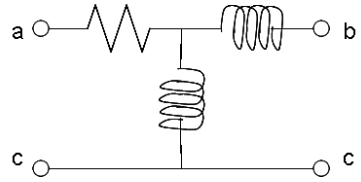

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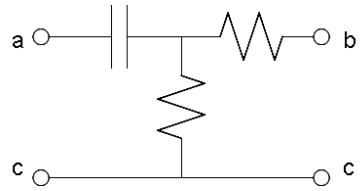

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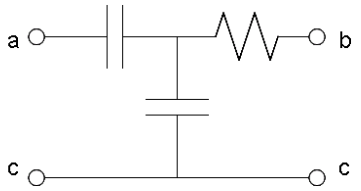

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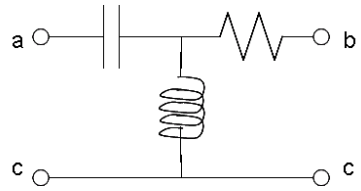

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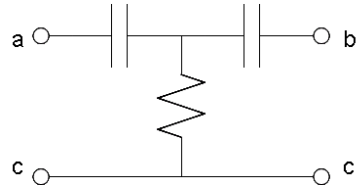

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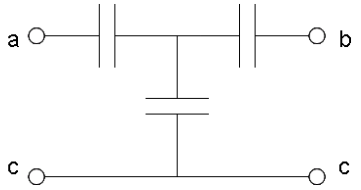

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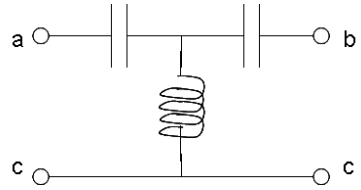

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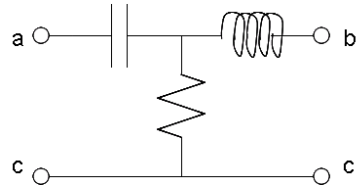

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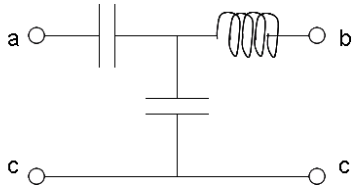

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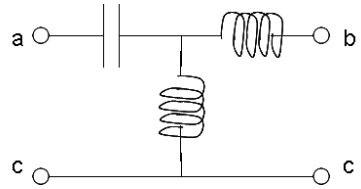

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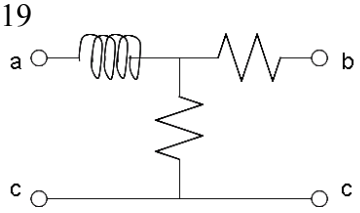

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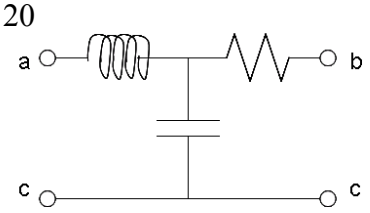

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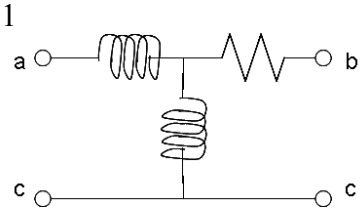

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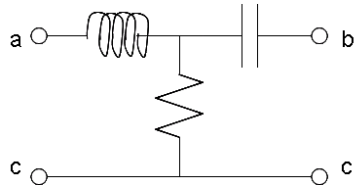

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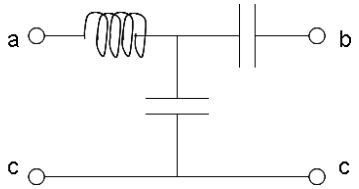

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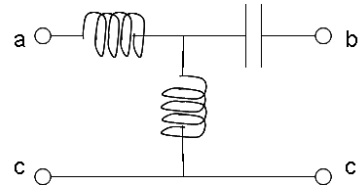

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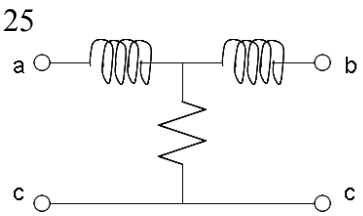

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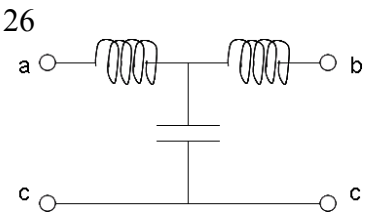

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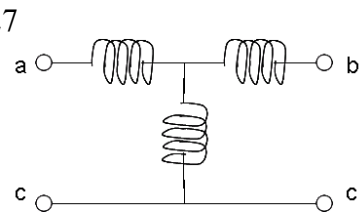

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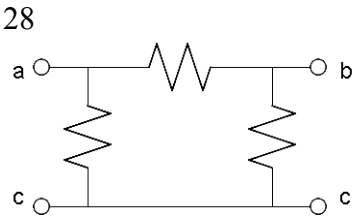

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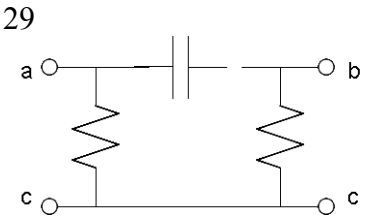

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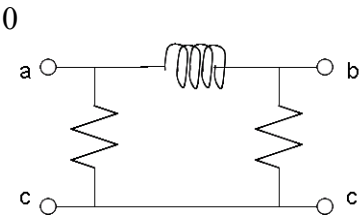

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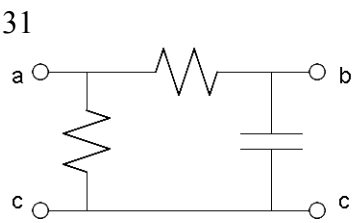

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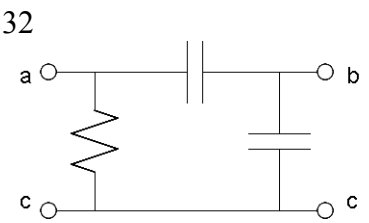

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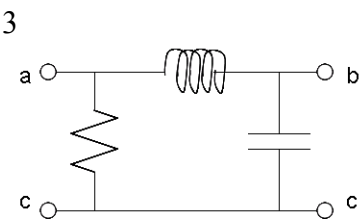

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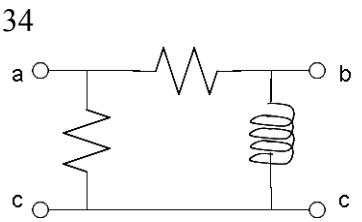

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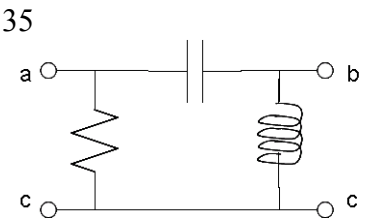

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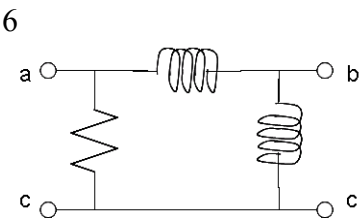

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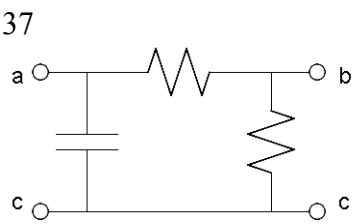

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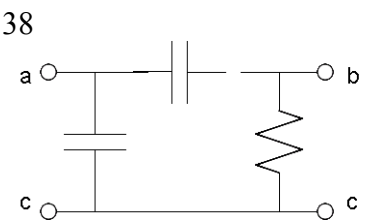

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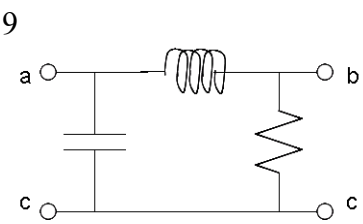

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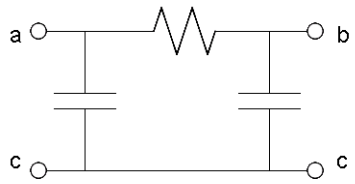

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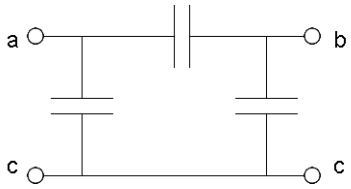

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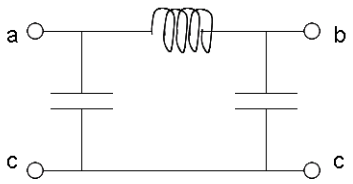

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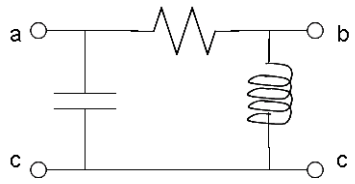

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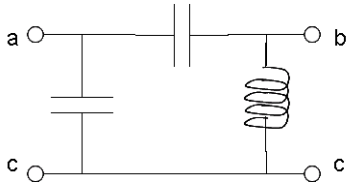

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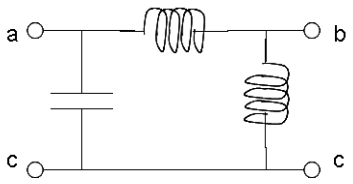

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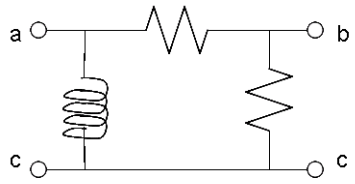

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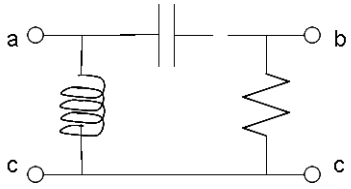

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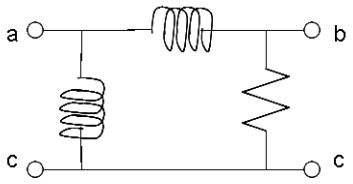

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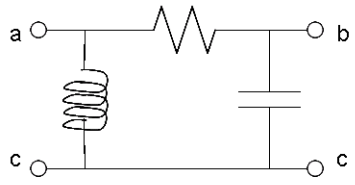

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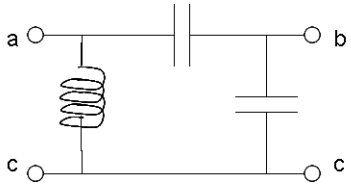

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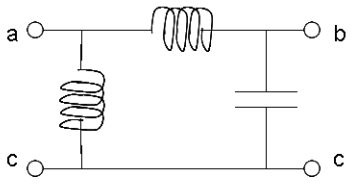

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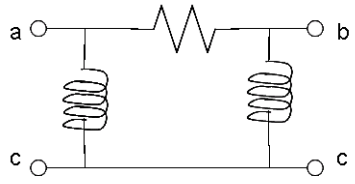

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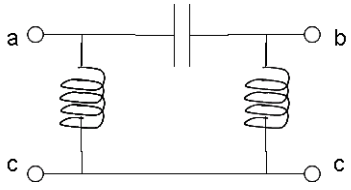

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