Operational Amplifiers

Goals:

1. Characterize basic open-loop op-amp behavior.
2. Design and characterize a basic inverting amplifier.
3. Confirm the effect of feedback in masking input resistance and output resistance.
4. Design, build and test a variable-gain instrumentation amplifier.

Preparation:

1. Carefully review this document.
2. Be sure to understand the analysis of the circuits to be built (covered in Prelab 3).
3. Review lecture slides on op-amps and differential amplifiers.
4. Start work on design of variable-gain instrumentation amplifier before coming to the lab.

Experiments:

Part 1:

1. Op-Amp's Open Loop Response

(a) **Get Parts and Built Test Circuit.** Obtain an op-amp from the parts bin. The pin out is given below in Fig. 1.

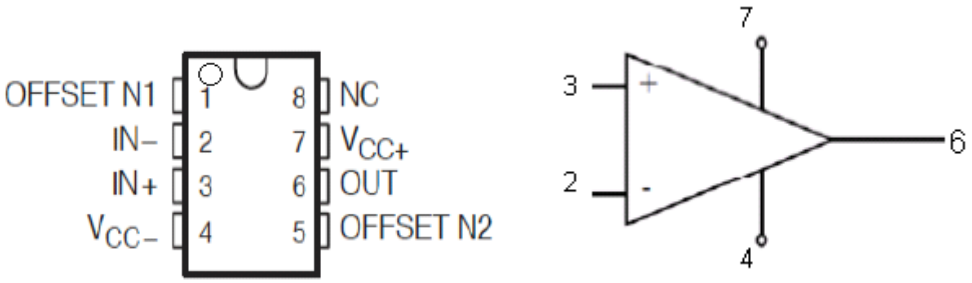

Fig. 1: Pin-out of UA741CN op-amp.

Now using a proto-board, assemble the open loop op-amp test circuit shown below in Fig. 2 with the UA741CN. The op-amp package (8 pin DIP) must be placed on the proto-board such that 4 pins are inserted on either side of the channel running down the center of the proto-board giving access to each of the 8 pins. Get help from the TAs if needed. Attach the SMUs as shown on the input and output terminals. Finally attach the dual dc power supply. To set this up, first ensure that the "common" voltage is shorted to ground as shown in Fig. 3. Use the +20 V and -20 V supplies, turn the "tracking ratio" nob to "fixed" (such that they are automatically equal and opposite) and adjust them to be +6 V and -6 V by choosing the appropriate button, and then turning the +/-20 V nob until the display shows 6 V. Confirm that the +20 V and -20 V outputs are in fact +6 V and -6 V with the DMM, and record the precise voltages.

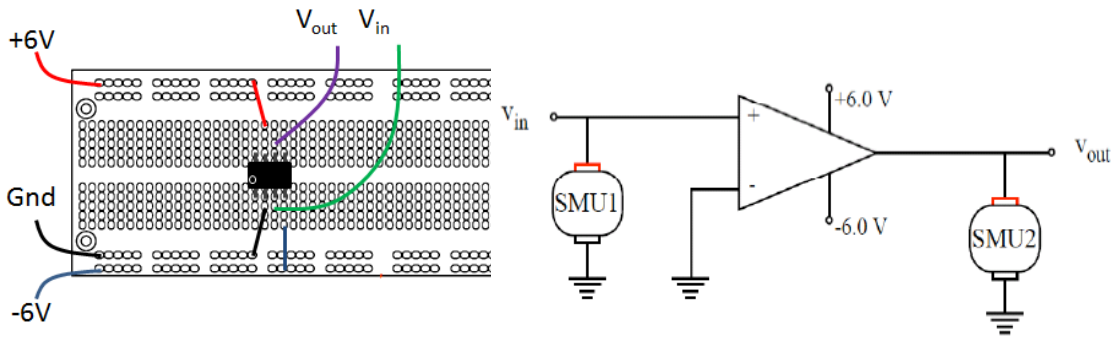

Fig. 2: Open loop test-setup.

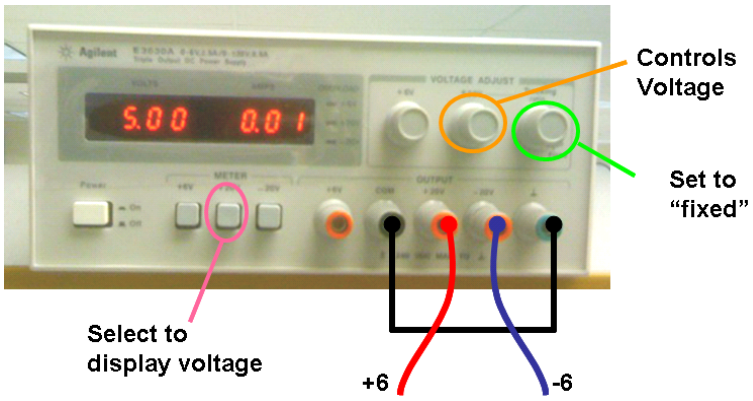

Fig. 3. Power supply arrangement to generate ±6 V: connect black to ground on your board.

(b) **Setup SMUs and Test**. Run the Keithley program for controlling the SMUs. **Start→All Programs→Keithley Instruments→Labtracer 2.0**. Program SMU1 to sweep voltage from -10 mV to +10 mV in 201 steps. Be sure to read back the SMU1 current. A 1 mA compliance on SMU1 is more than adequate. Select an integration time (NPLC) of 1. On SMU2, select a voltage meter on the Channel Function List. Set the compliance to 10 V. Energize and test the circuit: apply the dc power while performing the SMU sweep. Examine the voltage transfer function: plot V_{out} versus V_{in} for this circuit. For negative input signals the output voltage should be near the negative rail $-V_{cc}$ (or at least a voltage margin, V_{M-} away from the applied negative 6.0 volts). For positive input signals the output voltage should be near the positive rail $+V_{cc}$ (or at least a voltage margin V_{M+} away from the applied positive 6.0 volts). Save the raw data for the analysis – make sure SMU1 current and voltage are in the data as well as the SMU2 voltage.

(c) **Evaluate Selected Op-Amp Parameters**. From the data determine the input offset voltage (V_{IO}) (the input voltage where V_{out} passes through zero), the input bias current (I_{IB}, a constant current into/out of the op-amp's input), and the input resistance (R_I, related to the slope of the current into the op-amp as a function of V_{in}). Also estimate the maximum and minimum output voltage the op-amp can generate (one for the positive output signals and one for the negative output signals), and estimate the amplifier's gain from the peak slope of V_{out} vs. V_{in}. Note that this represents a lower limit on gain, which is almost certainly higher. Finally, load the output with a smallish resistance of 100 Ω to ground. Based on the output voltage, what is the maximum current the op-amp can source (positive) or sink (negative)?

2. Design and Build a Simple Inverting Amplifier with the 741 Op-Amp

We are now going to build the simple inverting amplifier with the UA741CN. This circuit will be tested with the SMUs in the same fashion as above.

(a) Choose resistor values to provide an amplifier, based on the circuit topology in Fig. 4, with an input resistance of 1 kΩ and gain of -100.

(b) Get parts and construct circuit. Obtain R_1 and R_2 from the parts bins. Measure the dc resistance of each resistor using the DMM. Record these values. Now with a proto-board assemble the following inverting amplifier circuit shown below in Fig. 4. Connect the SMUs as shown (same as used for open loop tests). Initially, do not include R_L. Remember to connect the 6-volt power supplies even though they are not shown in the schematic of Fig. 4.

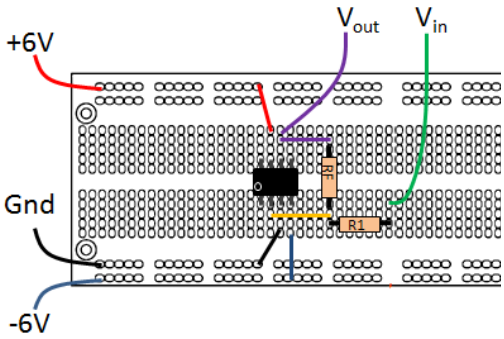

Fig. 4. Inverting amplifier circuit.

(c) Setup SMU and Test Amplifier. Program SMU1 to sweep voltage from -100 mV to +100 mV in 201 steps. Be sure to read back the SMU1 current. A 1 mA compliance on SMU1 is more than adequate, do not include any R_L. Select an integration time (NPLC) of 1. On SMU2, select voltage meter on the Channel Function List. Energize and test the circuit: the dc power must be applied while performing the SMU sweep. Examine the unloaded voltage transfer function – plot V_{out} versus V_{in} for this circuit. Explain how it differs from that obtained from the open loop circuit (looking for 2 major differences). Save the raw data (of the voltage transfer characteristic) for the analysis. Also examine (and plot) the input current vs input voltage.

(d) Evaluate the Closed Loop Gain and Input Impedance. Based on your voltage transfer function plot, find the range of input voltages where the amplifier is said to be linear (i.e., $V_{out} = GV_{in}$, where G is constant), and not in saturation near one of the rail voltages. Also record the output voltage for each saturated regime. From the data evaluate the nominal value of the magnitude of the voltage transfer function (the voltage gain, G). Based on the relationship between input current and input voltage, what is the effective input resistance when the circuit is not saturated?

3. Effect of Feedback on Input and Output Resistance

(a) Build the non-inverting amplifier from Fig. 5a. This can be done simply by swapping V_{in} and Gnd of the inverting amplifier in Fig. 4 (NOTE: Leave R_1 and R_2 connected to the IN- terminal of the op-amp, just connect V_{in} to IN+ and GND to R_1). Perform 2 sweeps. In the first, sweep SMU1's voltage from -100 mV to +100 mV and read-back

current, while configuring SMU2 as a voltmeter. In the second, set SMU1 as a voltage source (V = 0 V) set to read-back current, with current compliance of 100 mA and sweep the current from SMU2 from -25 mA to 25 mA, 101 steps. Set its voltage compliance to 5 V. Save the data from both sweeps.

(b) Insert two 1000 Ω resistors (R_{in}, R_{out}) across the input and output of the op-amp as shown below in Fig. 5b (also measure their resistance with the DMM). Perform the same sweeps as in part 3(a). Consider: do the input impedance and gain change when the op-amp is in linear operation? When it is saturated? ***When you complete this section, remove the resistors, but leave the op-amp wired to power.***

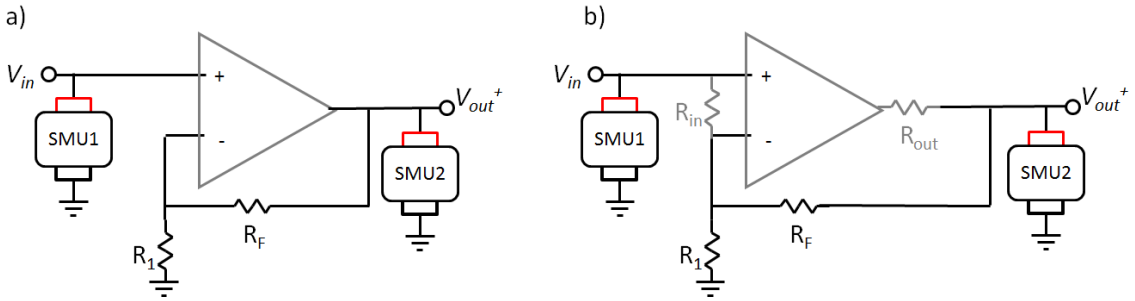

Fig. 5. Inverting amplifier circuit with explicit R_{in} and R_{out}.

Part 2: Design and Build a Differential, Variable-Gain Instrumentation Amplifier with Maximum CMRR

It is often the case that interesting signals (biological signals, for example) are small, differential measurements buried in a much stronger common-mode signal. The goal here is to build an amplifier to boost a small differential signal (with peak-to-peak voltage of anywhere between 5 mV_{pp} and 50 mV_{pp}) from a large source resistance (~100 kΩ) up to at least 1 V_{pp}, while suppressing a much stronger (~500 mV_{pp}) common-mode signal to < 20% the amplitude of the output from the differential input. To do this your amplifier should have the following properties:

(i.) **High input impedance**: R_{in} >> 100 kΩ

(ii.) **High, variable gain**: Compute the required gain range so that it can be adjusted for V_{out} > 1 V_{pp} for 5 mV < $|V_{in}|$ < 50 mV, but adjustable so the amplifier never saturates. Gain can be controlled with a variable resistor called a "potentiometer." We have potentiometers that range from ~< 10 Ω to > 2 kΩ.

(iii.) **High common mode rejection:** Be sure you can suppress the common mode to be less than 20% the differential output in all cases.

4. Design the Amplifier

Some seed topologies are shown in Fig. 6. Combine these circuits or the tricks they use as you see fit (not all are useful). You can collaborate with other groups and get help from TAs.

(a) Work out the required differential gain range and common mode gain to meet the above specs. Over-design your gain range a bit.

(b) **Design the amplifier on paper** by choosing the location(s) of the variable resistor(s), and the nominal value of the various resistors. If the amplifier is multi-stage, decide on the gain distribution between the stages (look at the scoring rubric below as you do this).

(c) **Choose specific resistor values**, and write out the differential and common mode gain as a function of every resistor value.
(d) Finally, **estimate the impact of worst-case 5% resistor mismatch** (look at your prelab for this).
(e) **Run your design past a TA** before continuing.

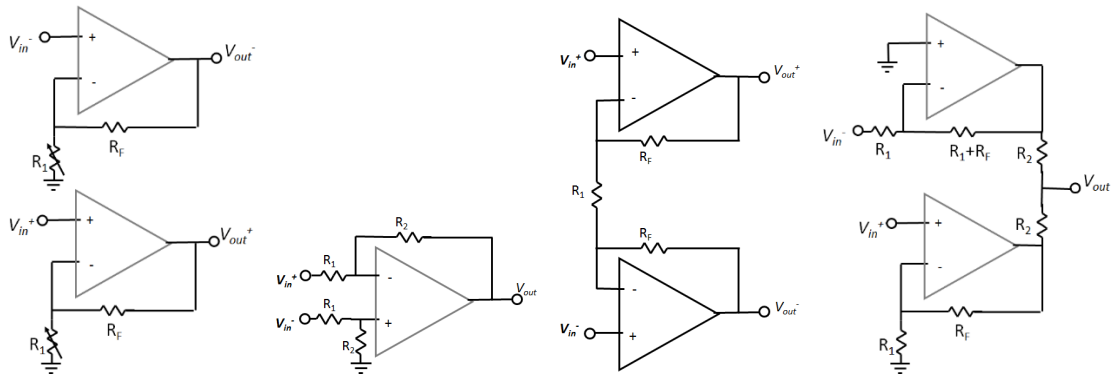

Fig. 6. Some amplifier topologies that you may find useful.

5. Build the Amplifier

Below are some tips:

(i.) **Build modularly:** If there is an easy way to break the structure up into separate sub-circuits, do so, and work in parallel (on separate proto-boards).
(ii.) **Test as you go:** Ensure each op-amp works before building stuff around it. Ensure each sub-circuit behaves as expected. To test common-mode gain short your inputs together and drive them with the same signal. For differential gain, ground on input and drive the other.
(iii.) **Color code your wires for easier debugging**: For example: red=V_{CC+}, black=Gnd, blue=V_{CC-}, green=V_{in+}, orange=V_{in-}, and purple=V_{out}. Use these wires to connect to your resistive network.
(iv.) Only when all your subcircuits work as expected, **hook them together**.

6. Test the Amplifier

(a) For a differential input of 5 mV_{pp} at 1 kHz, choose your gain setting (with the potentiometer(s) for a 1 V_{pp} output. Capture both input and output on the oscilloscope for your report. What is the gain?
(b) Increase the input to 50 mV_{pp}, without changing the gain, and capture input and output. What do you notice about the output?
(c) Now turn down the gain with your potentiometer(s) until the output is ~1 V_{pp} and save your data.
(d) Now, short your inputs together, and drive with a 0.5 V_{pp} input. Record input and output. Show for both minimum and maximum gain, from above.
(e) Characterize the input resistance of the amplifier by connecting one input to Gnd and driving the other with an SMU, swept from -1 V to +1 V in 101 steps and plotting current vs. voltage.

7. **Verify the Amplifier**

   Request a TA to bring over the test setup, and verify function when both differential and common mode are present; this will involve a differential 1 kHz sinewave and common mode 10 kHz squarewave. Also show maximum and minimum gain with and without common mode present. Have the TA sign off.

8. **Scoring Rubric**

   Scoring for performance (out of 20 points: over 20 = bonus): if the score comes out negative, we will round off to 0.

   (a) points for maximum differential gain without distortion (with a 5 mV_{pp} input) = $G_{dmax}/2$ (max pts = 20)

   (b) points for differential gain range (without distorting under 5 mV_{pp} input) = $5*\log_{10}(G_{dmax}/G_{dmin})$ (max pts = 20)

   (c) points for CMRR (worst case between G_d = 200, G_d = 20): $10*\log_{10}(G_d/G_c)$ (max pts = 20)

   (d) points for the ratio of G_{max} to G_{min}:
   $\mathbf{G_{max}}$: maximum 1 kHz output without distortion when *500 mV_{pp} 10 kHz common mode is present*: for a 5 mV_{pp} 1 kHz differential input vs
   $\mathbf{G_{min}}$: minimum 1 kHz output that is still 5x the 10 kHz square-wave output when *500 mV_{pp} 10 kHz common mode is present*: for a 5 mV_{pp} 1 kHz differential input
   Points = $20\log_{10}(G_{max}/G_{min})$

   (e) -2 point for every resistor in your design, -4 points for every op-amp, -6 points for every potentiometer.

Wind down:

Clean up around your bench and return any components back to their storage bins. Be sure all data is collected and placed on your own storage media. Delete all files on your desktop or at least organize them in a folder. ECE makes no guarantee that these files left on your desktop will remain over time.

Analysis:

1. Open Loop Op-Amp Response. Plot the open loop voltage transfer characteristics (V_{out} vs. V_{in} on linear scales) of the UA741CP. Given the measurement parameters used, what is the maximum open loop voltage gain that can be measured?
2. Op-Amp's Input Current and Input Resistance. Estimate the input resistance and nominal value of input bias current for the 741. Compare results with spec sheet.
3. Op-Amp's Input Voltage Offset and Voltage Margins. From your measured open loop response, determine the input voltage offset for the Op Amp and compare with the spec sheet. For the ±6.0 Volts power supplies, determine the maximum and minimum output voltages for each amplifier.
4. Inverting Amplifier Transfer Characteristic. Plot the voltage transfer characteristics (V_{out} vs. V_{in} on linear scales) of the UA741CP inverting amplifier. Also plot I_{in} for the same sweep of V_{in}.

5. For the non-inverting amplifier, overlay plots of V_{out} vs. V_{in}, without and with R_{in} and R_{out} included. Also plot I_{in} for the same two scenarios.
6. Compute the gain, input resistance and output resistance of the amplifier when the explicit 1-kΩ R_{in} and R_{out} are absent, and present. Also discuss and try to explain the impact of these elements on the output saturation voltage and current, and the behavior of I_{in}, I_{out} and V_{in}, when the amplifier is saturated.

For the differential amplifier:

7. Compute the agreed upon specifications for the amplifier (differential gain range, max common mode gain), and describe how you found them.
8. Describe your design process, and include a diagram of your final design. Label your resistors R_1, R_2, etc, and tabulate their design values.
9. Provide the measured values of R_1, R_2, etc.
10. Plot the measured input and output waveforms of your amplifier for a 5 mV_{pp} differential input, for a 50 mV_{pp} differential input (with and without adjusted gain), and for a 500 mV_{pp} common-mode input. In each case compute the gain.
11. Compute the input impedance based on the input I-V curve.
12. Finally include (easily readable) screen-shots of the output for the TA-administered tests.
13. Compute your performance score (we will check your math).

Design and build a differential, variable-gain instrumentation amplifier with maximum CMRR.

It is often the case that interesting signals (biological signals, for example) are small, differential measurements buried in a much stronger common-mode signal.
The goal here is to build an amplifier to boost a small signal differential signal (anywhere between 5mVpp and 50mVpp) from a large source resistance (~100kΩ) up to at least 1Vpp, while suppressing a much stronger (~500mVpp) common-mode signal to <20% the amplitude of the output from the differential input. To do this your amplifier should have the following properties:
High input impedance: Zin>>100kΩ

High gain: compute the required gain range so that it delivers Vout>1Vpp for 5mV<|Vin|. This means differential gain should be at least 200,

High common mode rejection: be sure you can suppress the common mode to be less than 20% the differential output. In words, this means common mode gain should less than 0.2.

1) ***Design your amplifier***: Some seed topologies are shown below, combine these circuits or the tricks they use as you see fit (not all are useful).
a. **Design the amplifier on paper**, choosing the location(s) of the resistor(s), and nominal value of the various resistors. If the amplifier is multi-stage, decide on the gain distribution between the stages
b. **Choose specific resistor values**, and write out the differential and common mode gain as a function of every resistor value.
c. **Run your design past a TA** before continuing.

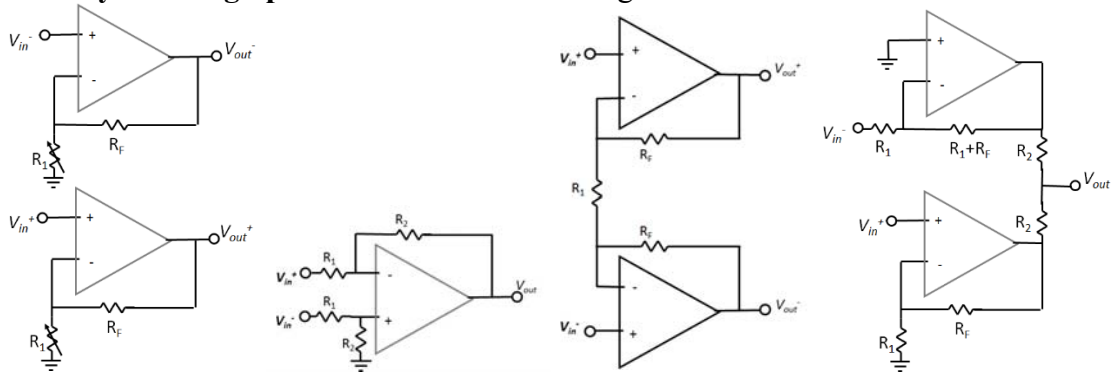

Figure 6. Some amplifier topologies that you may find useful.

2) ***Build the amplifier***. Some tips:
a. **Build modularly:** If you have multiple stages, build and test each stage separately, then connect them together once each stage operates as expected.

b. **Test as you go:** To test common-mode gain short your inputs together and drive them with the same signal. For differential gain, ground on input and drive the other.
c. **Color code your wires for easier debugging**: For example: red=VCC+, black=GND, blue=VCC-, green=Vin+, orange=Vin-, and purple=out. Use these wires to connect to your resistive network. The extra 5 minutes you spend on neat wiring will save you 2 hours of begugging.
d. Only when all your subcircuits work as expected, **hook them together**.

3) Test your circuit:

a. Use the signal generator to create a 5mVpp sine wave at 1 KHz. For a differential input of 5mVpp at 1kHz, confirm your gain creates a 1Vpp output. Capture both input and output on the oscilloscope for your report. What is the gain?
b. Optional: Increase the input to 50mVpp, without changing the gain, and capture input and output. What do you notice about the output?
c. Now, unground the one input, and connect the two differential inputs together. This is a common mode signal. Adjust the signal generator to input a 0.5Vpp input. Record input and output. This is the common mode gain.
d. Characterize the input impedance of the amplifier by connecting one input to gnd and driving the other with an SMU, swept from -1V +1V in 101 steps and plotting current vs voltage.

Scoring for performance (out of 20 points: over 20 = bonus): if the score comes out negative, we will round off to 0.

- Differential gain should exceed 200 (5 pts)
- There should be no visible distortion for V0 when it is 1V pp (5 pts)
- Common mode gain should be less than 0.2. (5pts)
- Input impedance should be greater than 100 kHz
- Bonus: Common mode gain less than 1% +3pts, measured max input before distortion is observed +3 pts

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Analysis (to be included inside the template)

1) Open Loop Op Amp Response. Plot the open loop voltage transfer characteristics (vout vs. vin on linear scales) of the UA741CP. Given the measurement parameters used, what is the maximum open loop voltage gain that can be measured?
2) Op Amp's Input Current and Input Resistance. Estimate the input resistance and nominal value of input bias current for the 741. Compare results with spec sheet.
3) Op Amp's Input Voltage Offset and Voltage Margins. From your measured open loop response, determine the input voltage offset for the Op Amp and compare with the spec sheet. For the ±6.0 volts power supplies, determine the maximum and minimum output voltages for each amplifier.

4) Inverting Amplifier Transfer Characteristic. Plot the voltage transfer characteristics (vout vs. vin on linear scales) of the UA741CP inverting amplifier. Also plot Iin for the same sweep of Vin.
5) For the non-inverting amplifier, overlay plots of Vout vs Vin, without and Rin and Rout included. Also plot Iin for the same two scenarios.
6) Compute the gain, input impedance and output impedance of the amplifier when the explicit 1kΩ Rin and Rout are absent, and present. Also discuss and try to explain the impact of these elements on the output saturation voltage and current, and the behavior of Iin, Iout and Vin, when the amplifier is saturated.

For the differential amplifier:

7) Show a schematic of your differential amplifier, along with all resistor values. Describe why you chose the specific architecture for the differential amp that you built.
8) Show the calculations you used to determine the resistor value, and the expected performance of the amplifier in terms of common mode and differential gain.
9) Plot the measured input and output waveforms of you amplifier for a 5mVpp differential input, and for a 500mVpp common-mode input. In each case compute the gain.
10) Compute the input impedance based on the input I-V curve.