ECE 2300
Digital Logic & Computer Organization

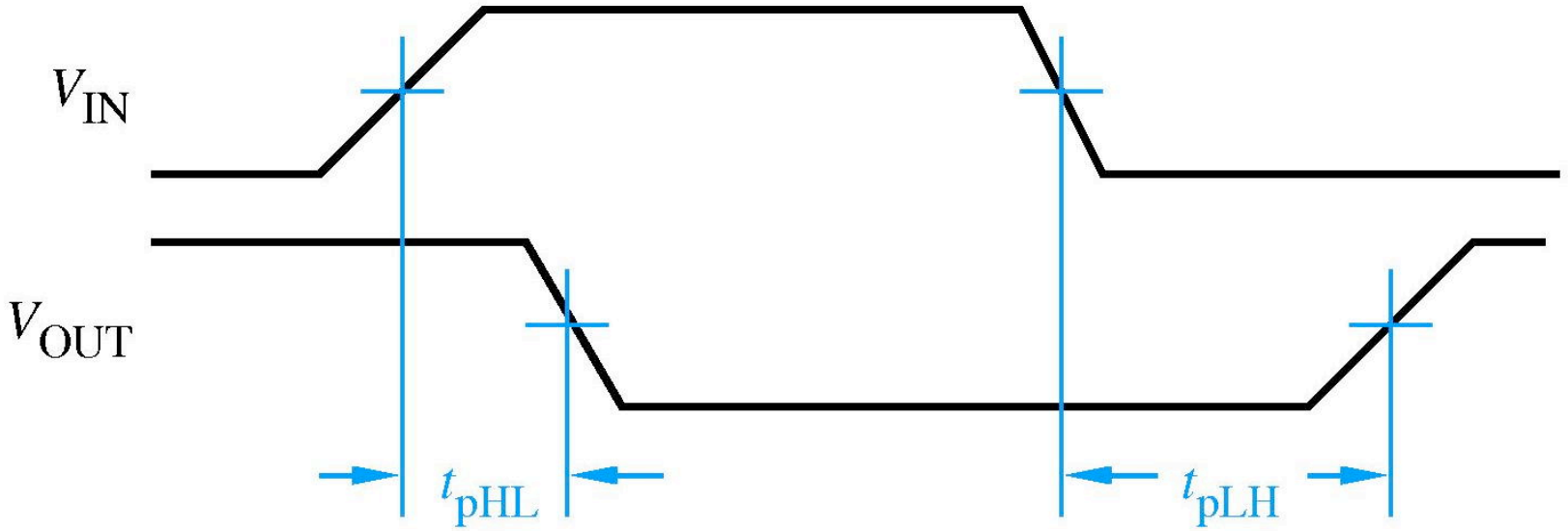
Fall 2016

Hazards, Timing, Clocking

Cornell University

Propagation Delay

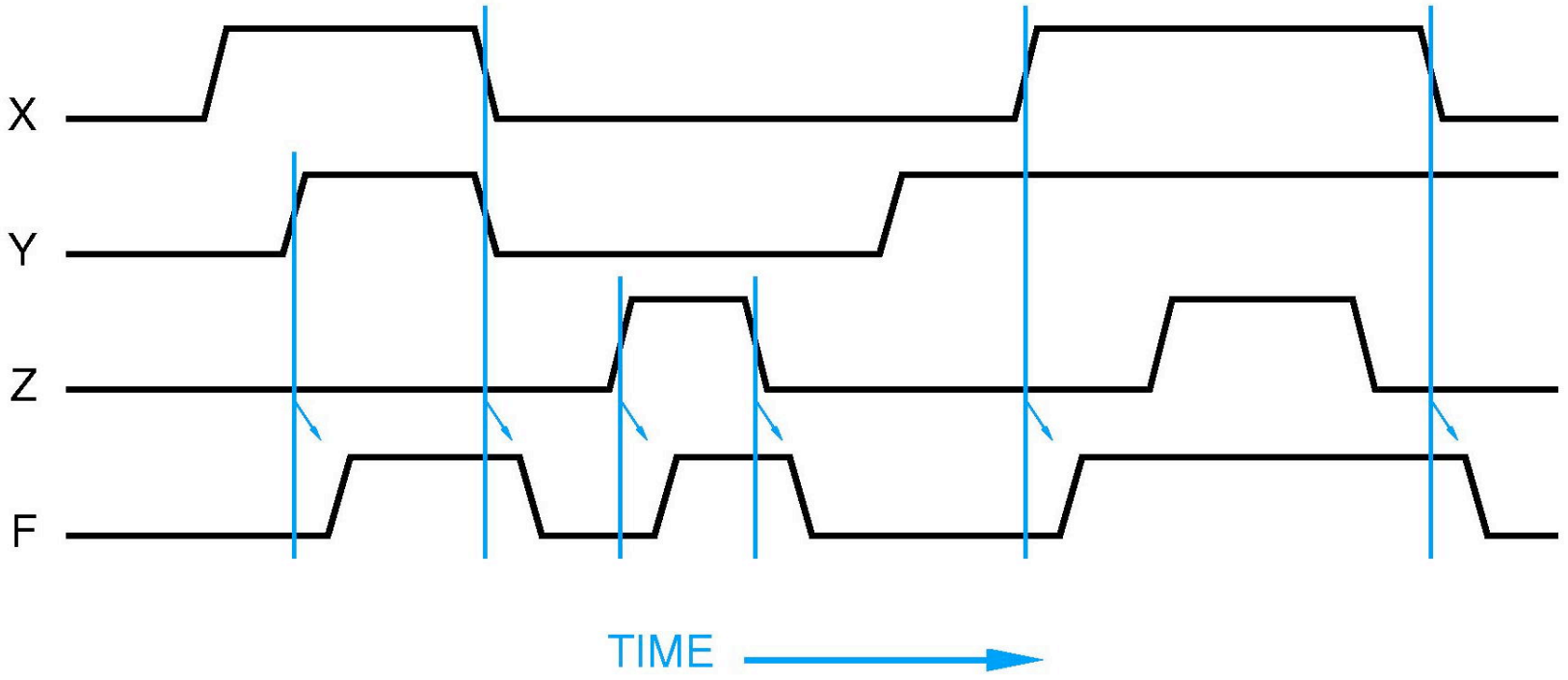
- Time for change in input to change the output
- Typically specified between 50% points



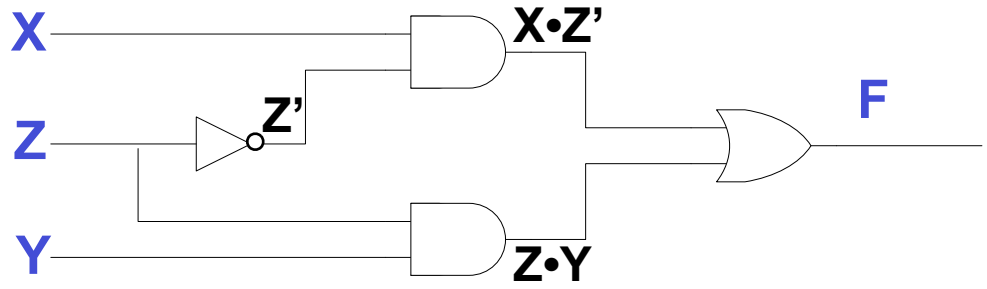
- Circuits have *minimum* and *maximum* propagation delays
  - Minimum sometimes called the *contamination delay* and maximum the *propagation delay*

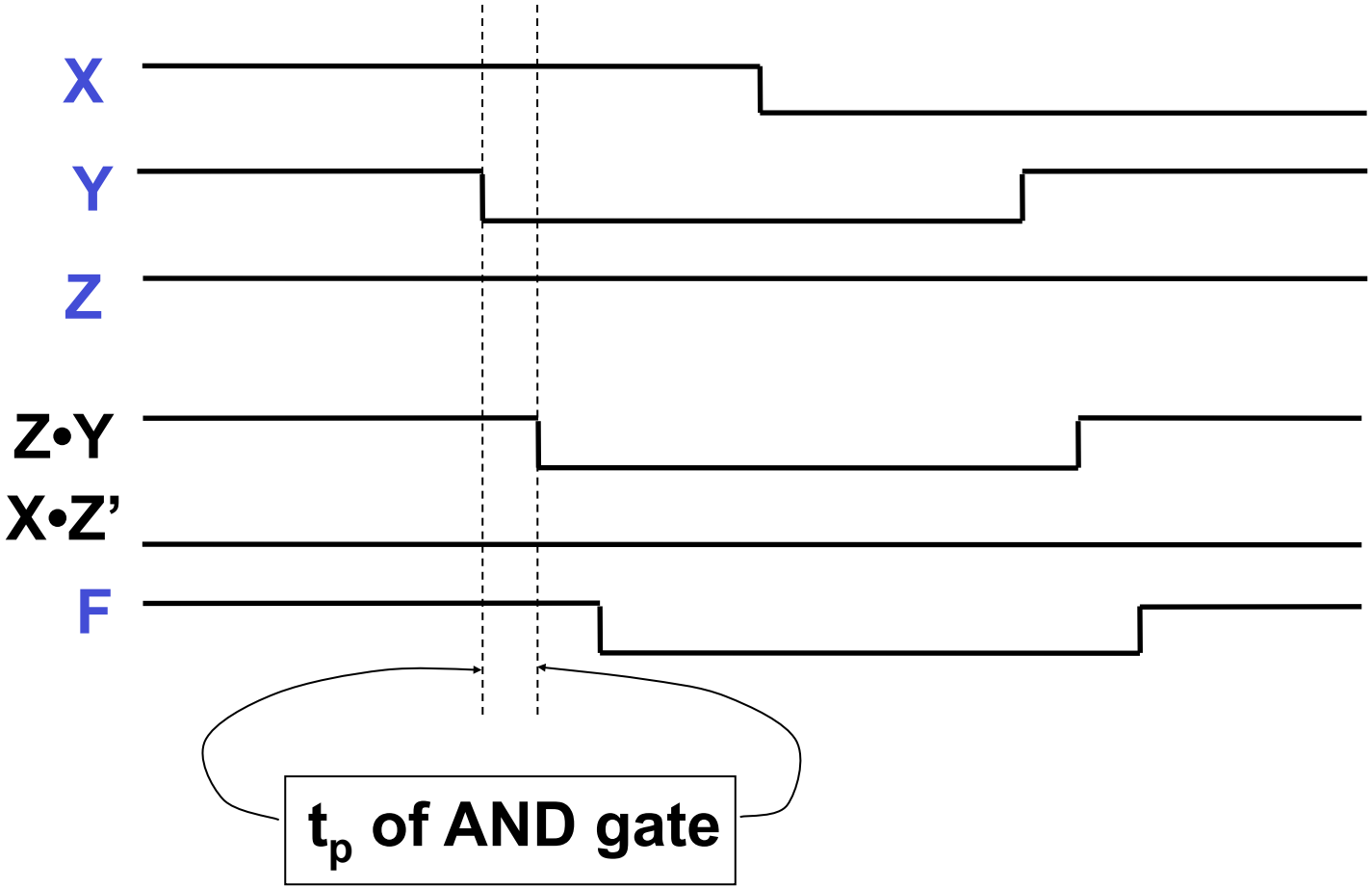
Timing Diagram

- **Shows how outputs respond to changes in inputs over time**



Timing Diagram



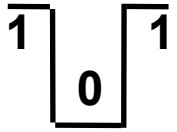


Hazard (*Glitch*)

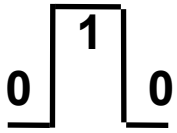
- Unplanned momentary switching of an output
- Occurs when different paths through circuit have different propagation delays

Types of Hazards

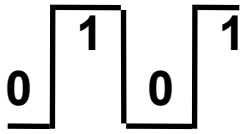
- **Static 1-hazard**
  - Input change causes output to go from 1 to 0 to 1 (should have stayed 1)

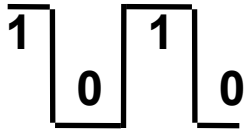


- **Static 0-hazard**
  - Input change causes output to go from 0 to 1 to 0 (should have stayed 0)



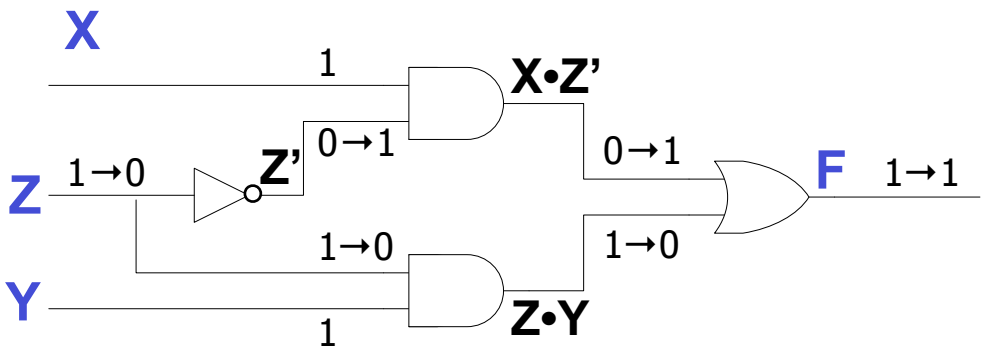
- **Dynamic hazards**
  - Input change causes a change from 0 to 1 to 0 to 1 or from 1 to 0 to 1 to 0 (there should be just one change)





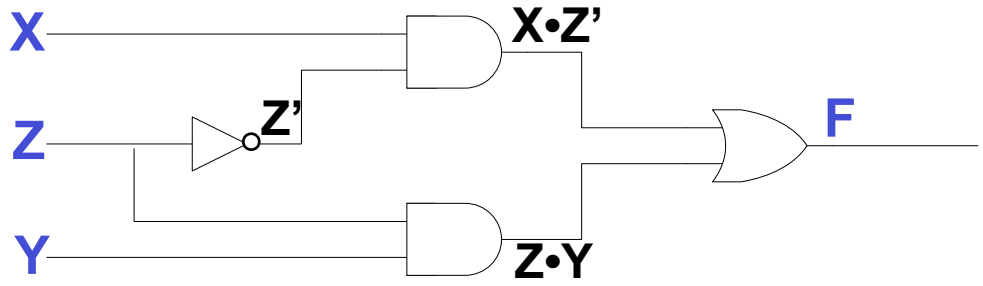
Static 1 Hazards

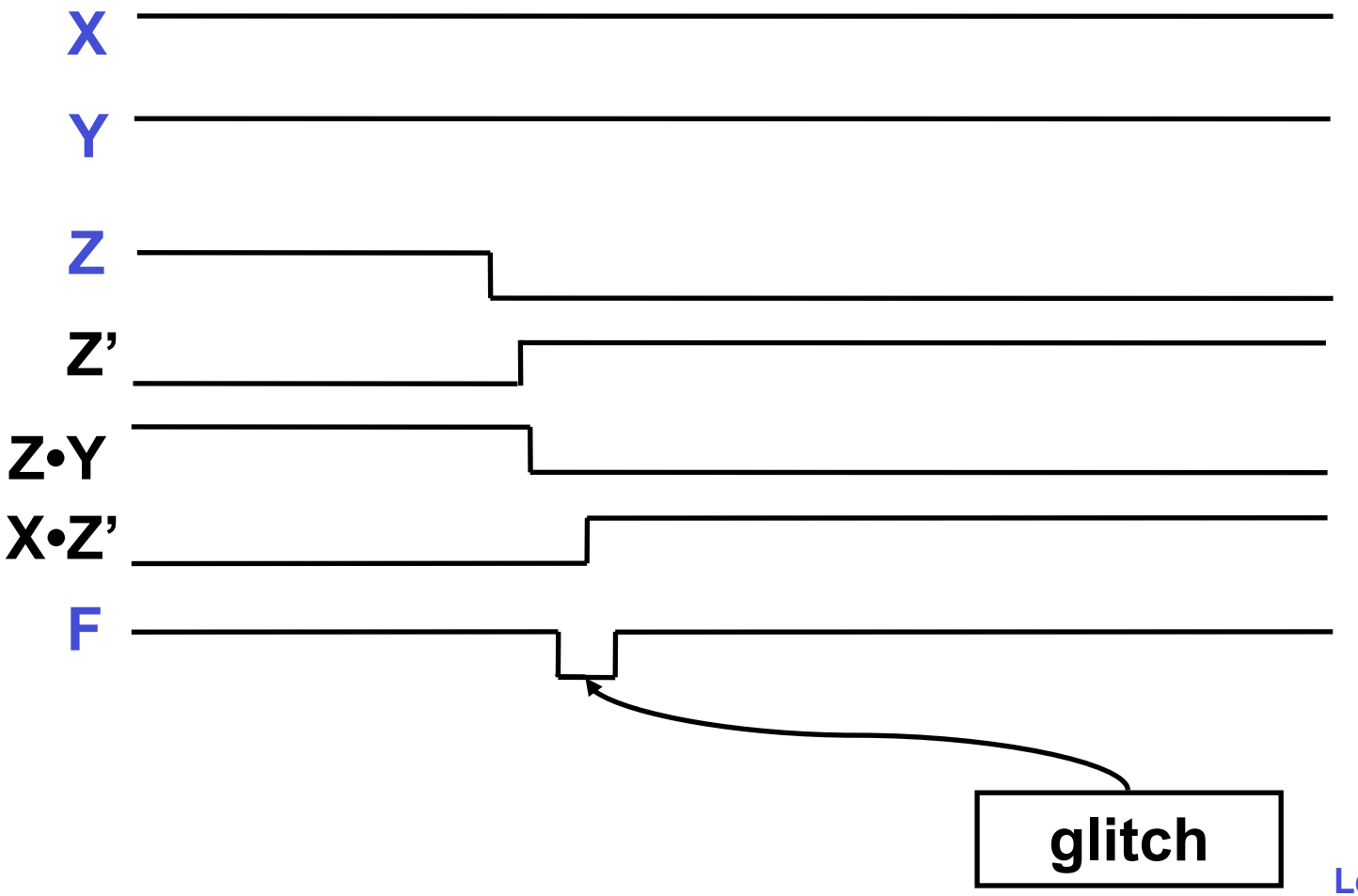
- Glitches due to unequal signal propagation delays through the circuit
- Output signal should stay at 1, but shows a transient 0 value



Assume X and Y are 1
Z changes from 1 to 0

Timing Diagram Showing Glitch





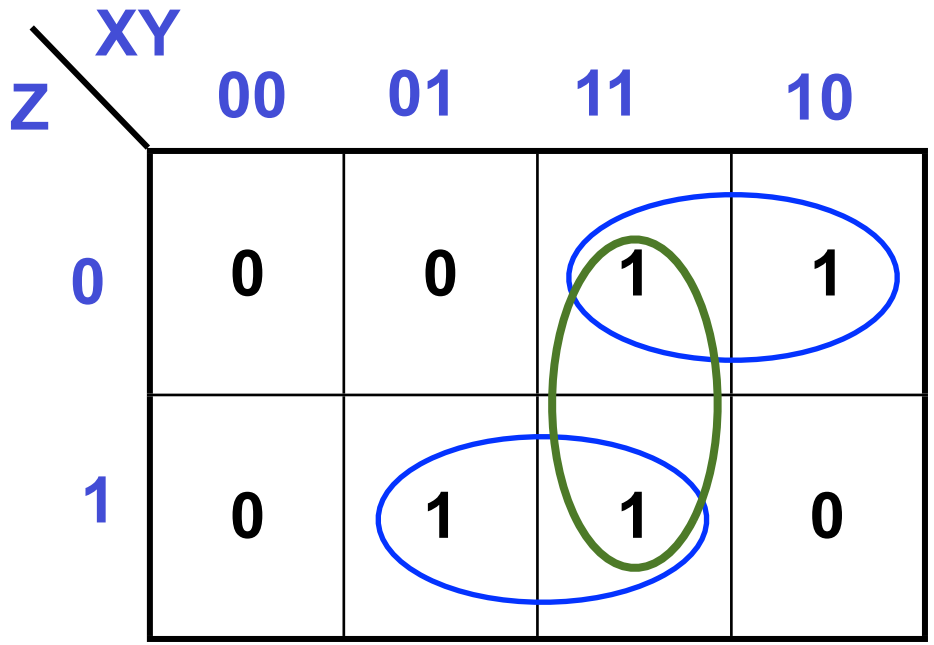
Eliminating Static 1 Hazards

- Identify prime implicants that are not overlapping in Karnaugh map
- Include consensus terms to cover transitions between product terms

Hazard Detection and Elimination

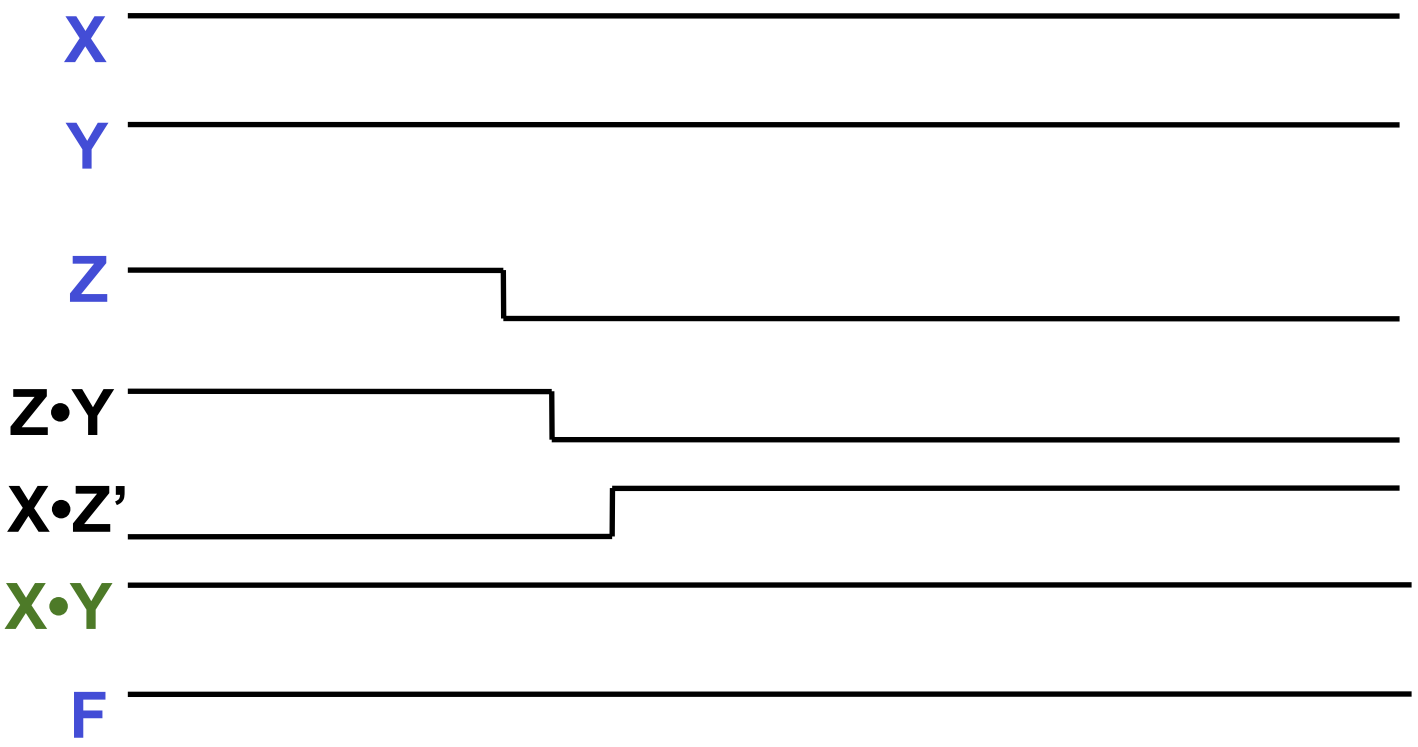
$F = X \cdot Z' + Y \cdot Z$

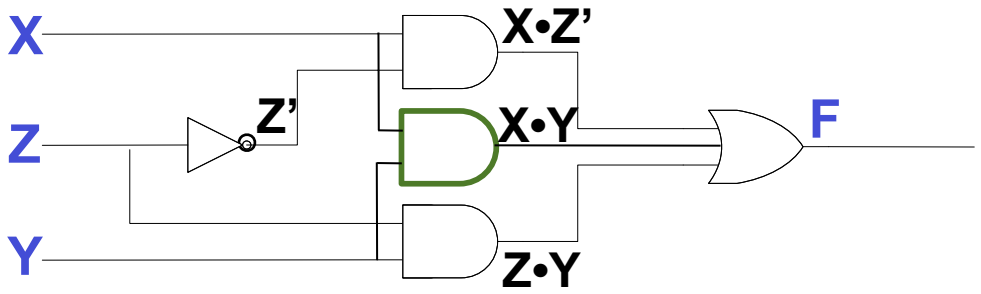
$F = X \cdot Z' + Y \cdot Z + X \cdot Y$



Adding a consensus term

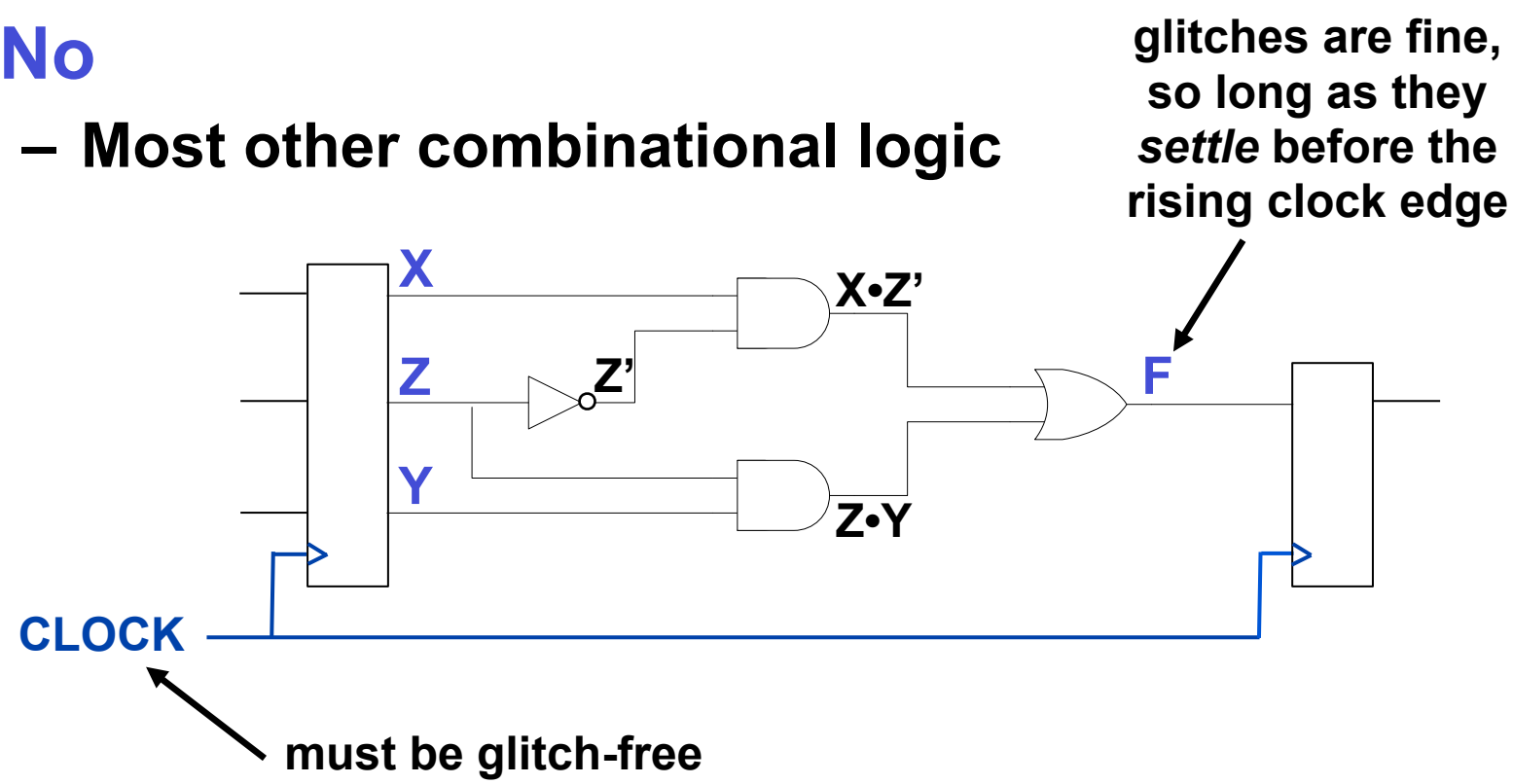
Glitch-free Design Timing Diagram





Do Glitches Matter?

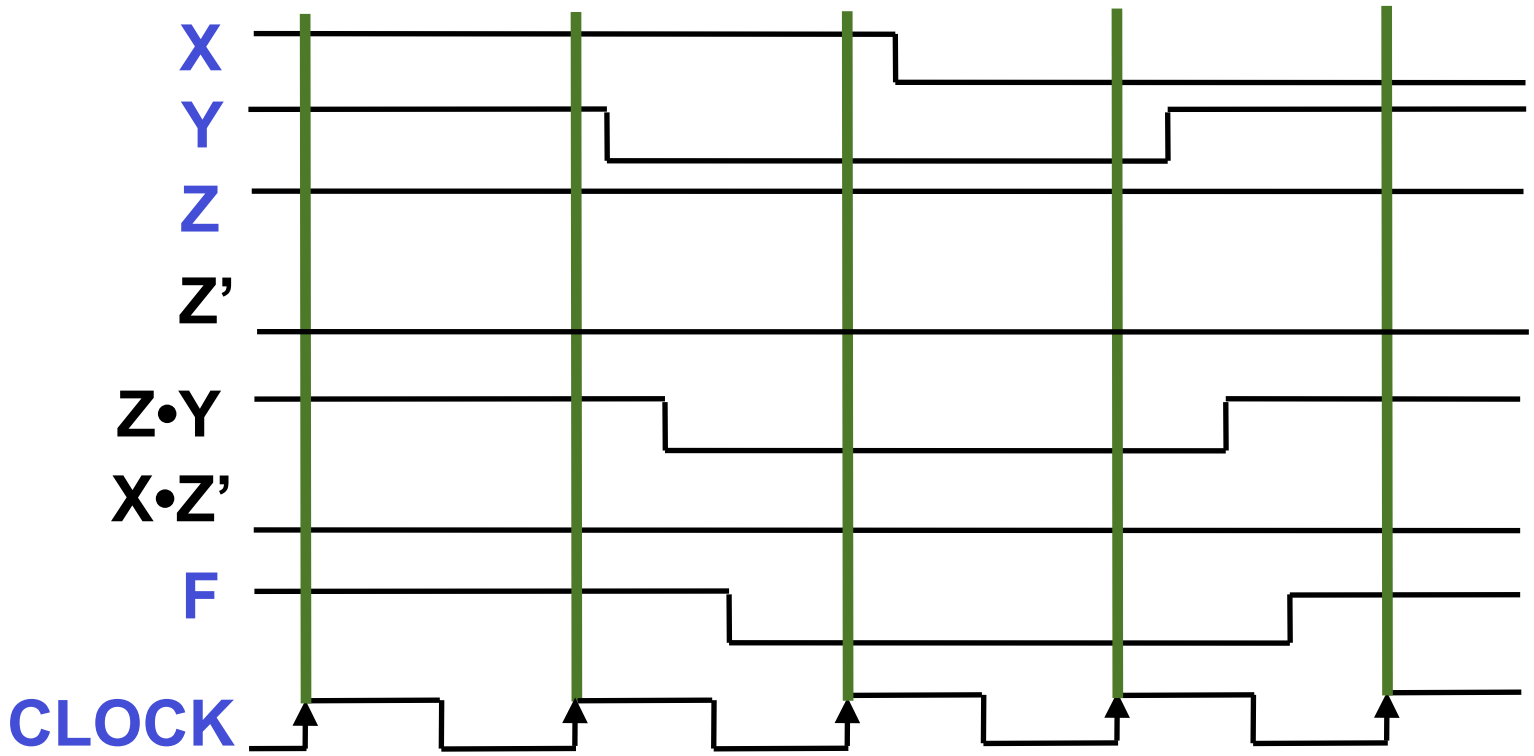
- **Yes**
  - FF clocks and latch enables (and asynch resets!)
- **No**
  - Most other combinational logic

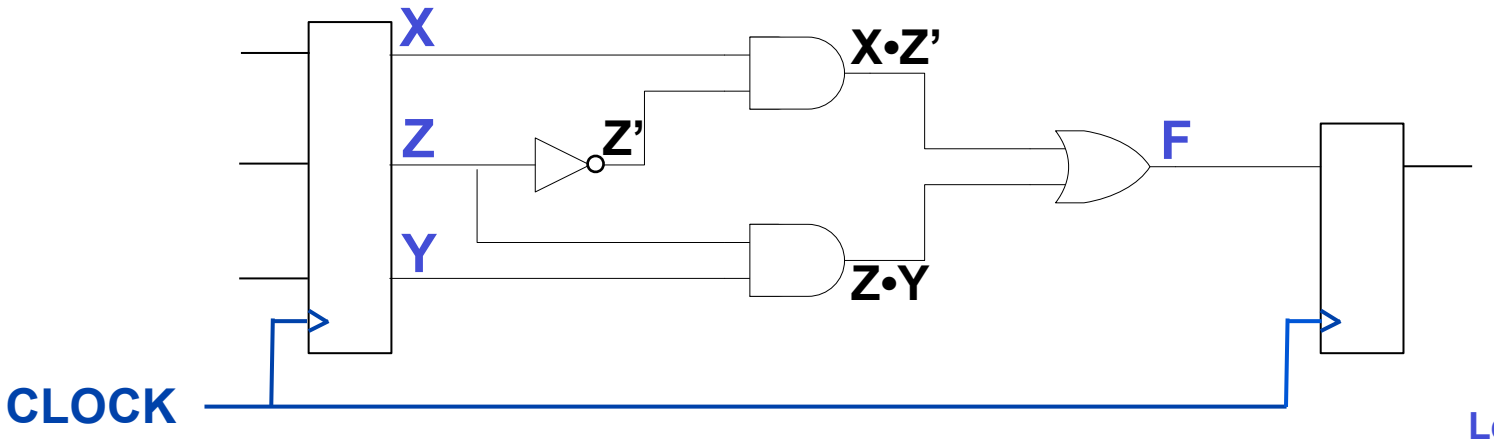


Sequential Circuit Timing

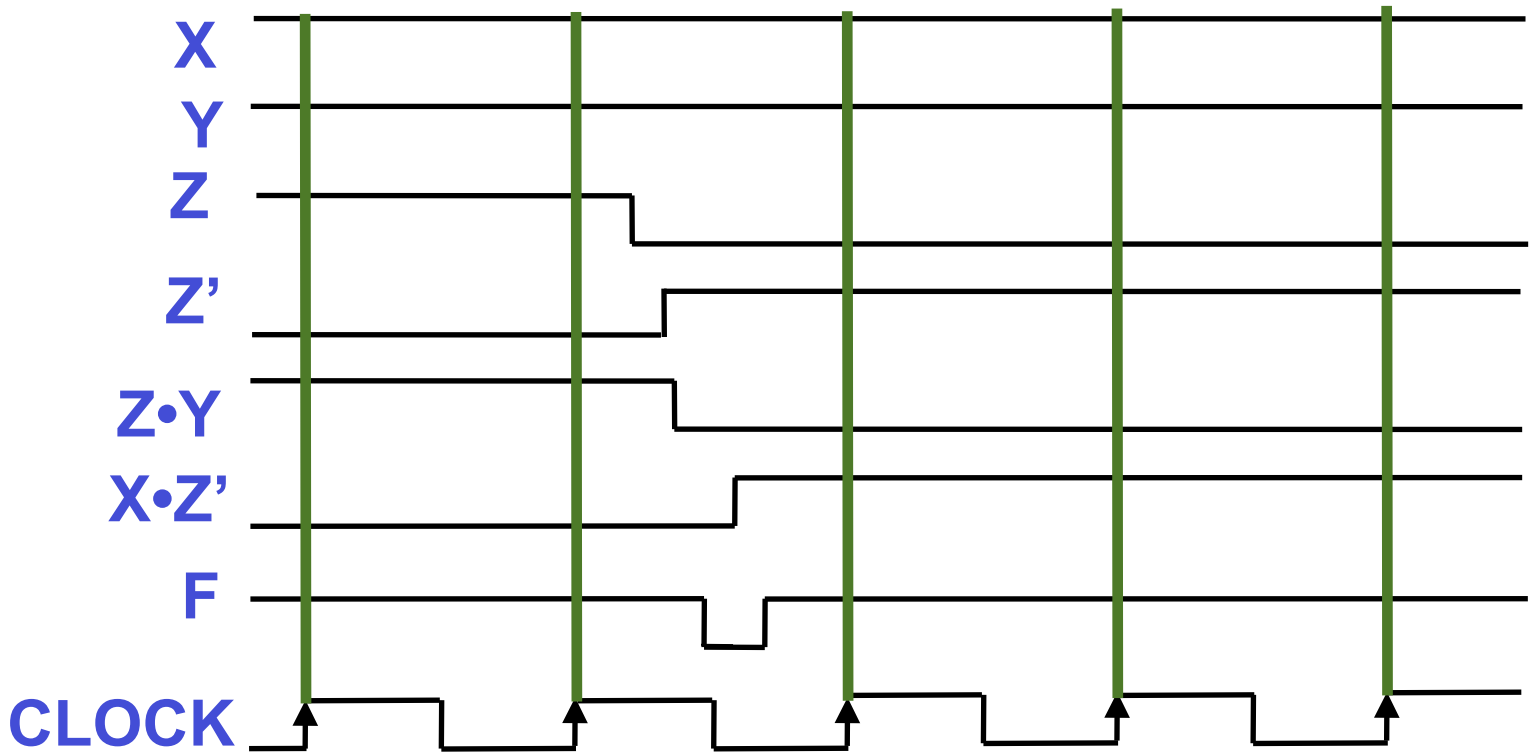
- FFs and latches must meet specified *setup time* and *hold time* requirements
- The *worst case setup time* (*longest timing path*) determines the maximum clock frequency
- *Timing analysis* involves calculating the time delays between all FF pairs within the circuit
  - To determine the maximum operating frequency
  - To ensure that hold time requirements are met

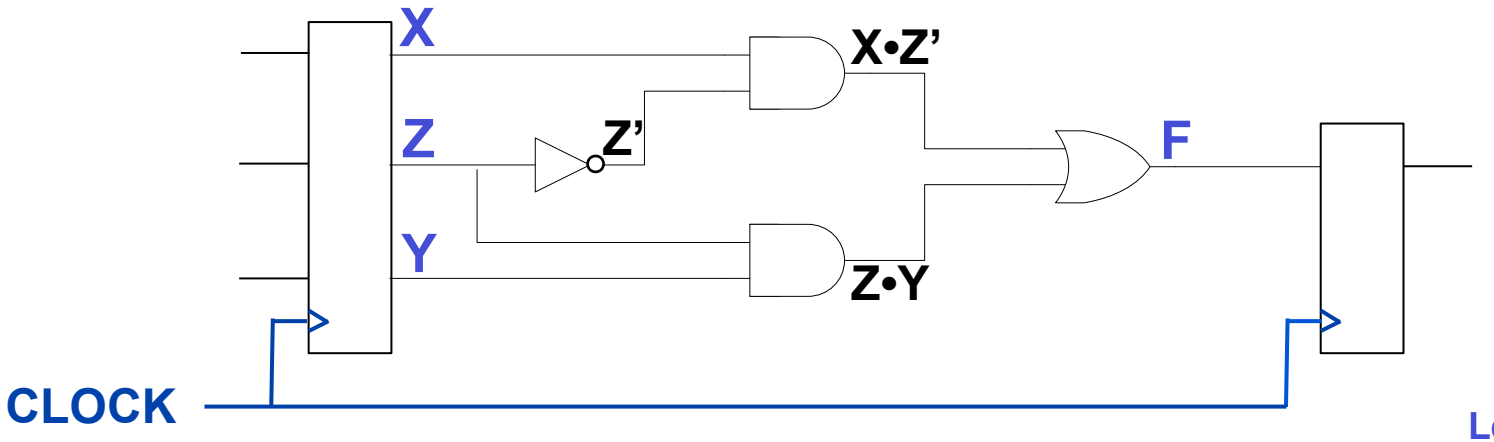
Sequential Circuit Timing



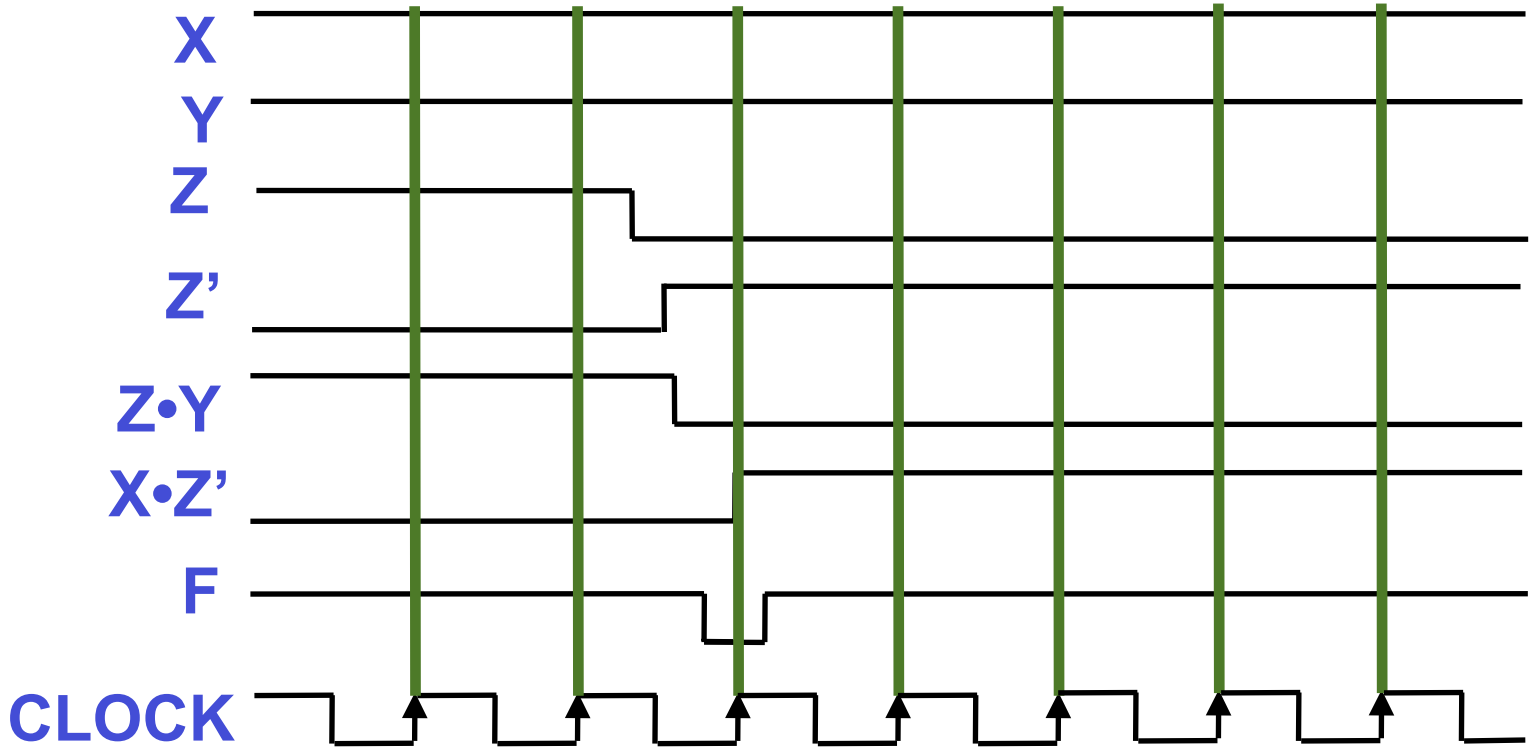


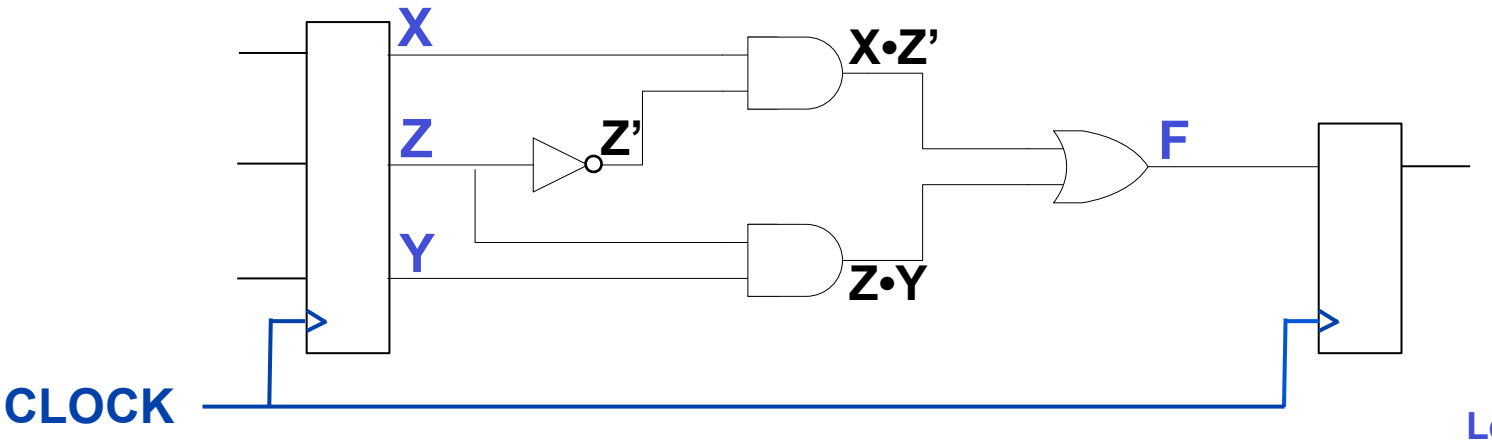
Glitch on F: No Problem



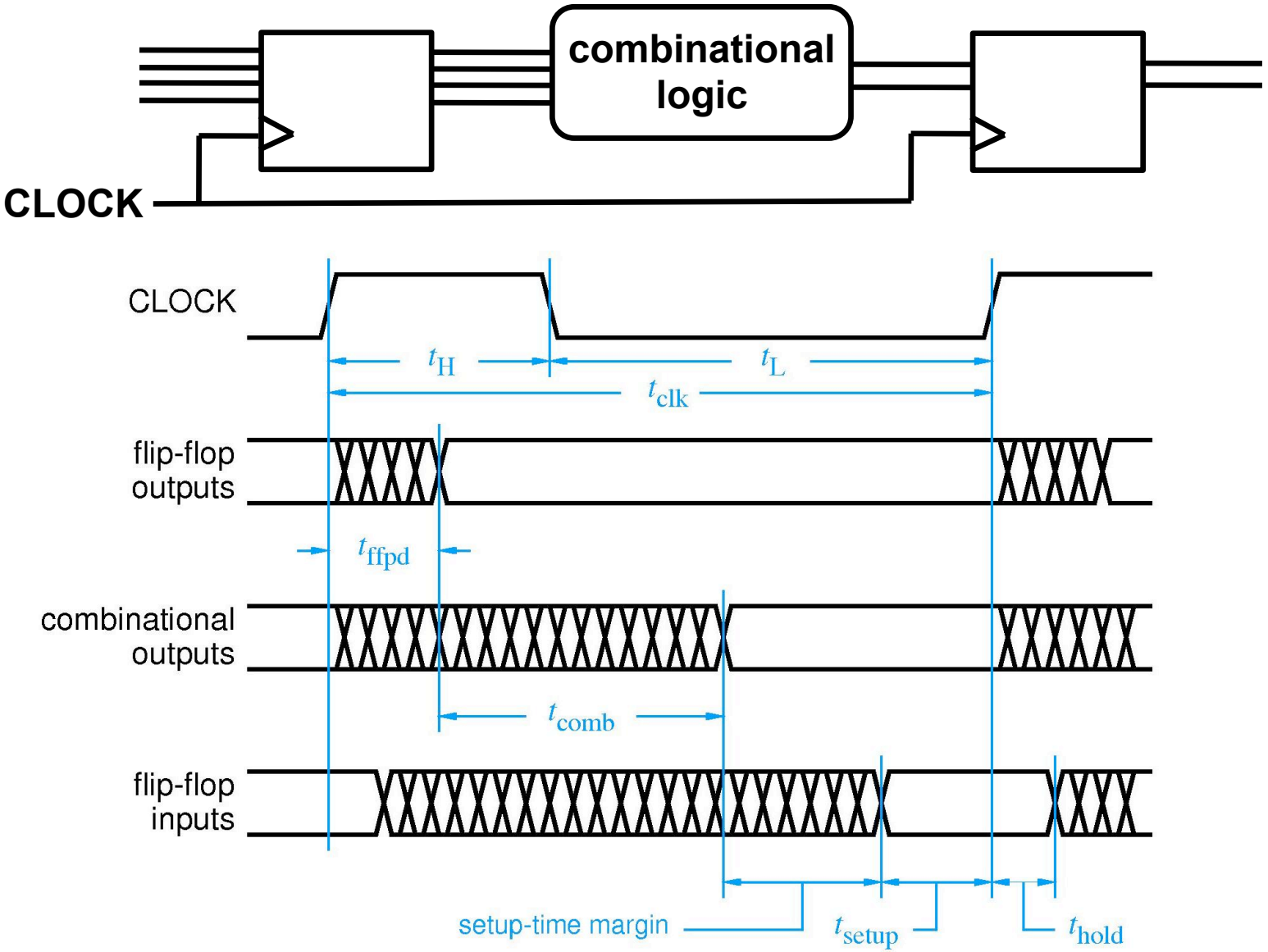


But What About This Situation?



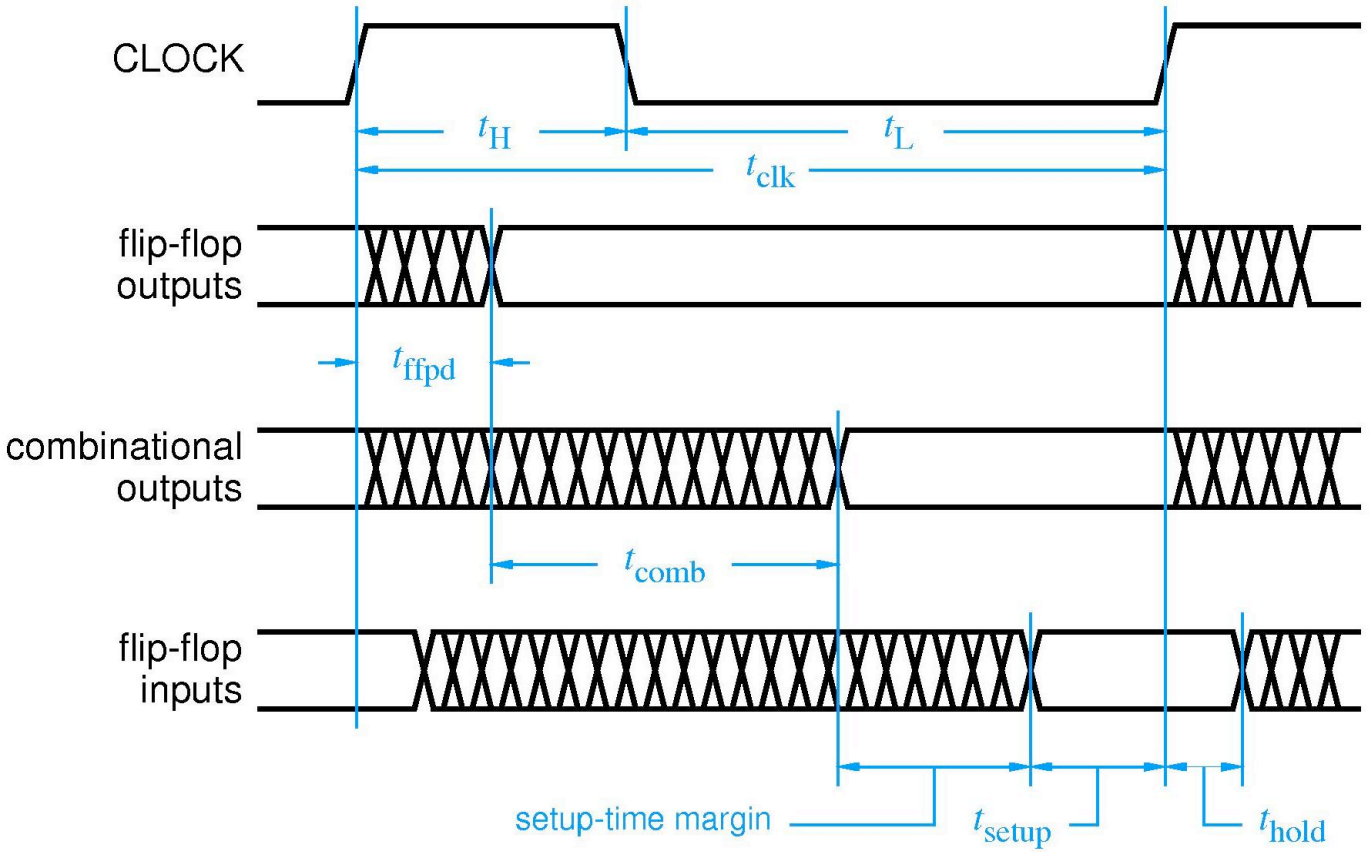


Setup and Hold Time

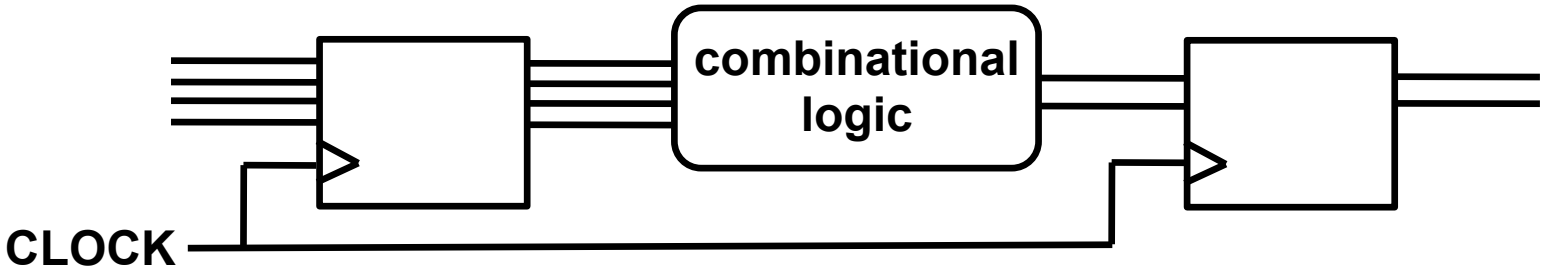


Setup Time

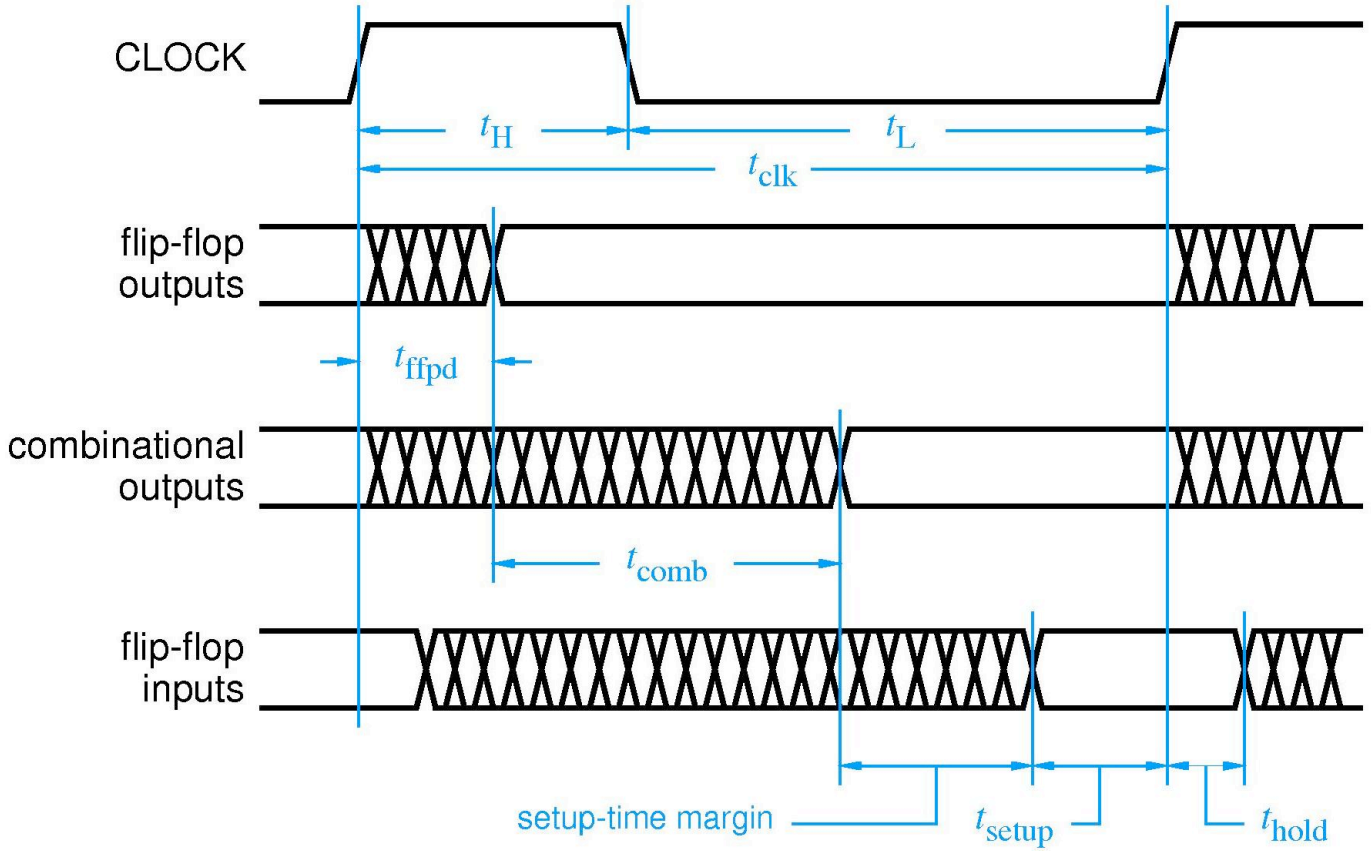
- **FF input must be stable t_{setup} before the triggering FF clock transition**



Setup Time Determines Clock Frequency



$$t_{clk} \geq t_{ffpd(max)} + t_{comb(max)} + t_{setup}$$

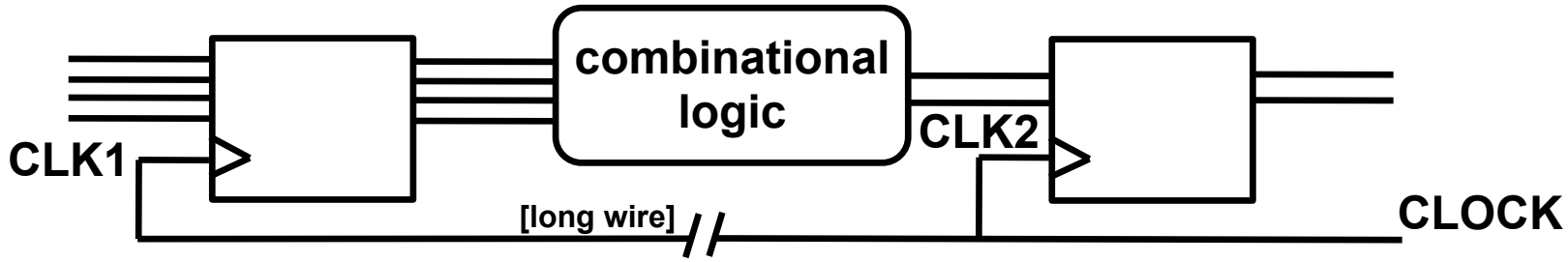


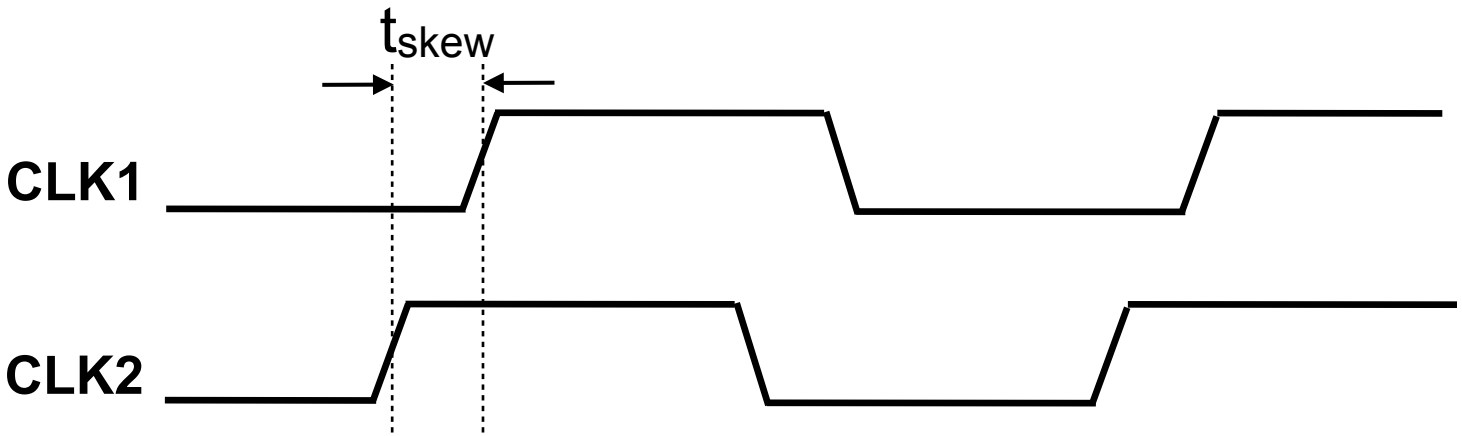
Setup Time Determines Clock Frequency

- $t_{clk} \geq t_{ffpd(max)} + t_{comb(max)} + t_{setup}$
- Every circuit path between every pair of FFs must satisfy the above equation to run the circuit at a frequency of $1/t_{clk}$
- The *worst case* situation is assumed
  - Longest delay through the circuit
  - Worst case temperature and voltage
  - Worst case manufacturing variations

Clock Skew May Make Matters Worse

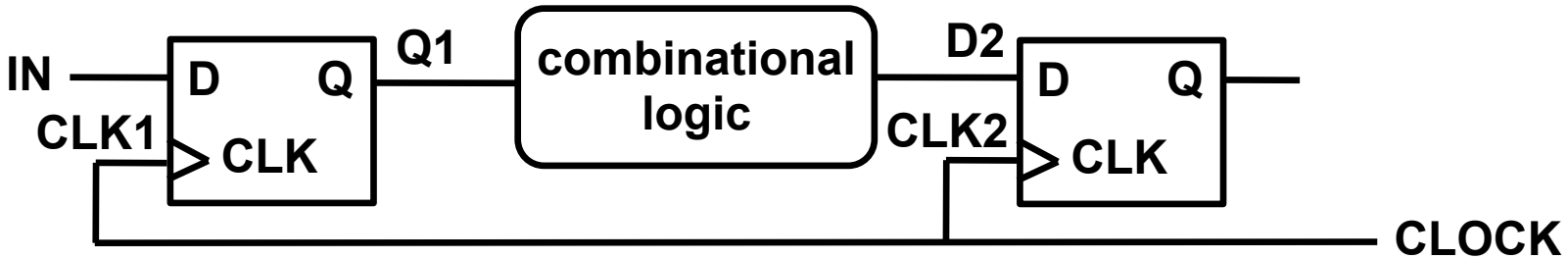
- Clock may not reach all flip-flops simultaneously

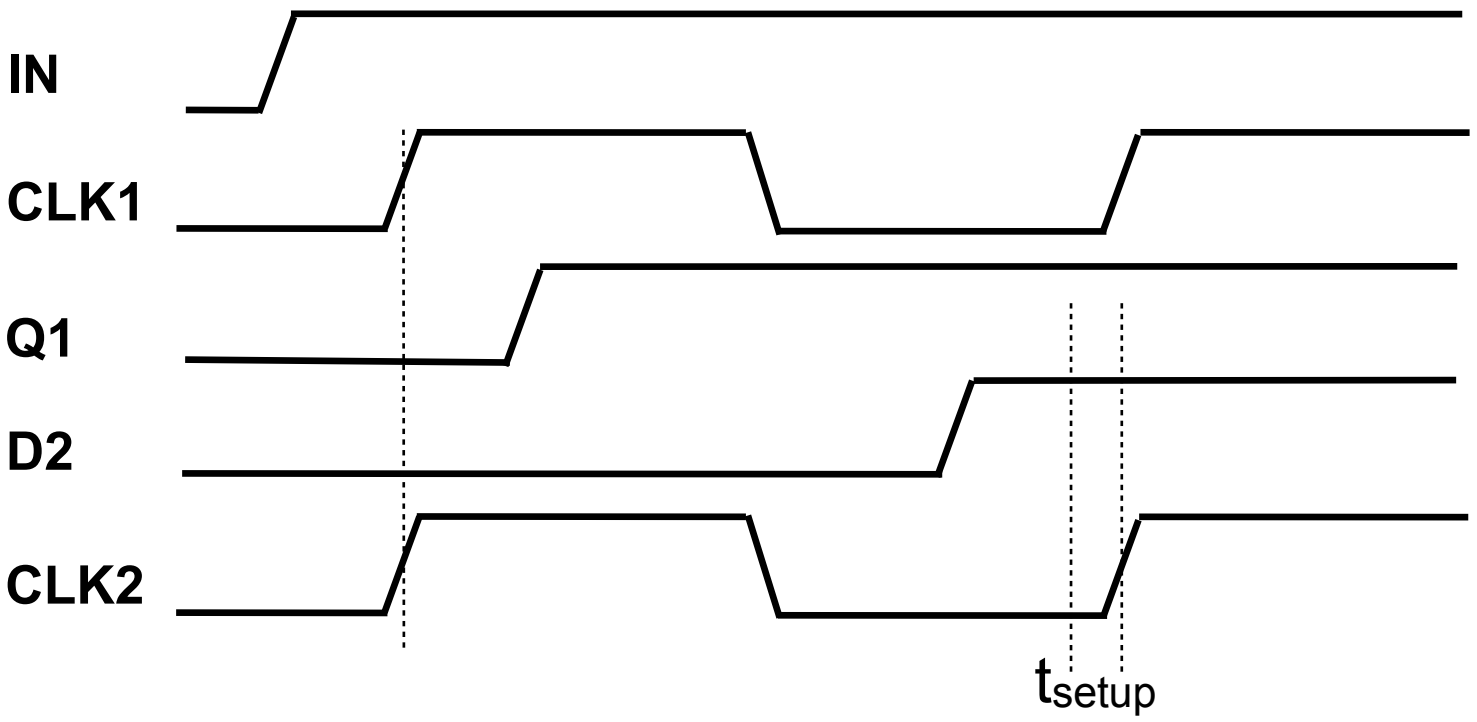




- We assume the worst case clock skew situation when calculating setup and hold time

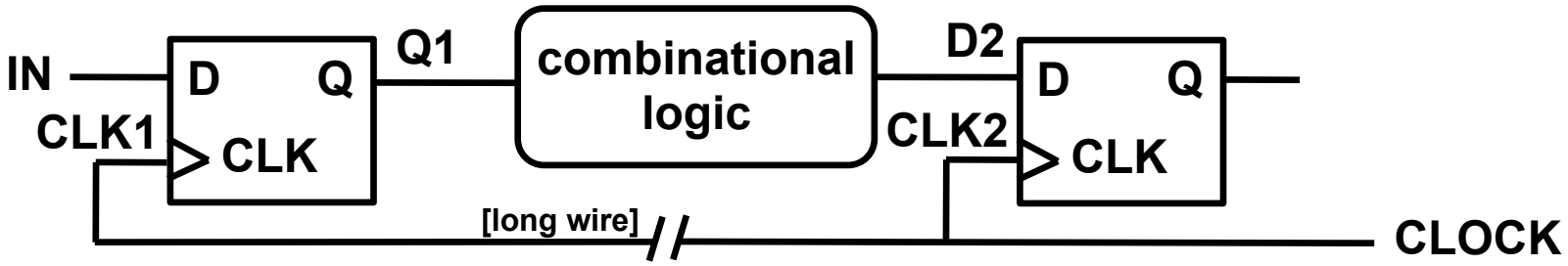
Setup Time Without Clock Skew

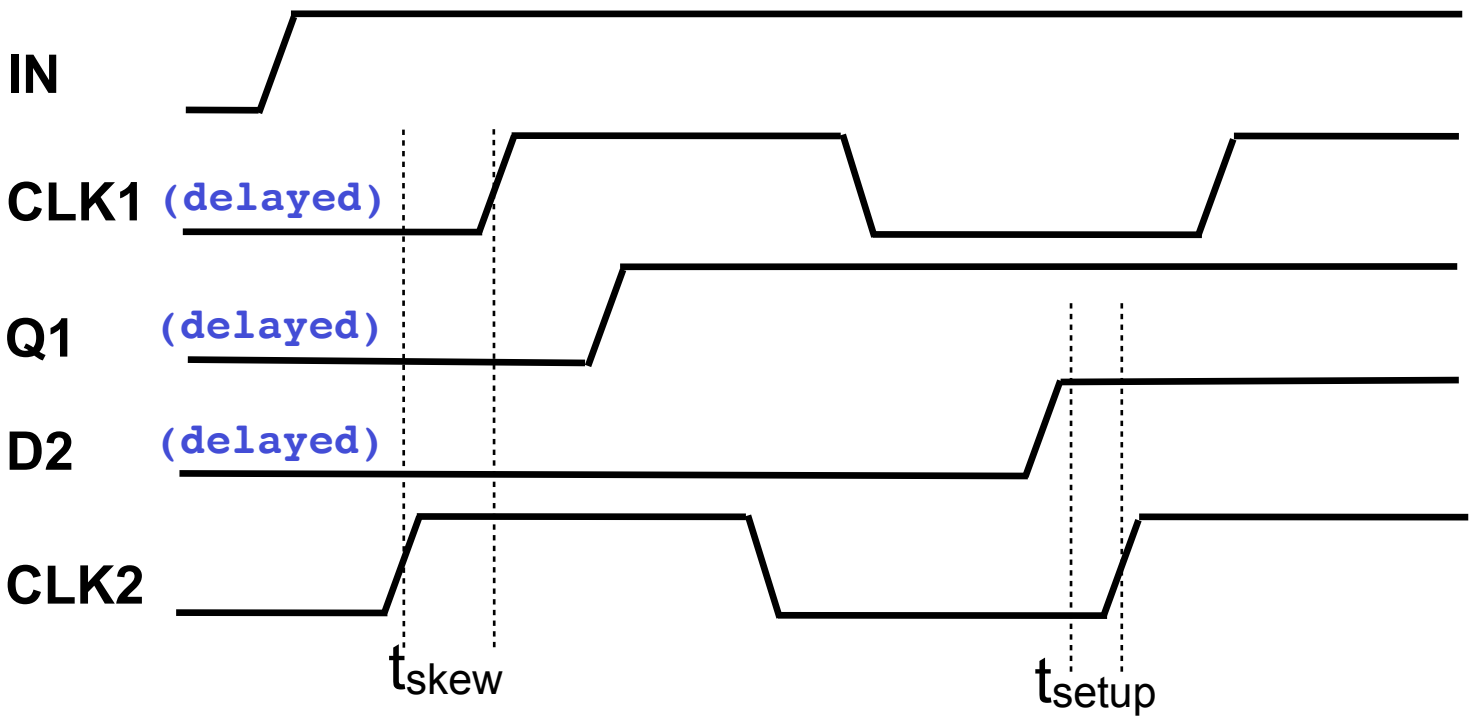




$$t_{clk} \geq t_{ffpd(max)} + t_{comb(max)} + t_{setup}$$

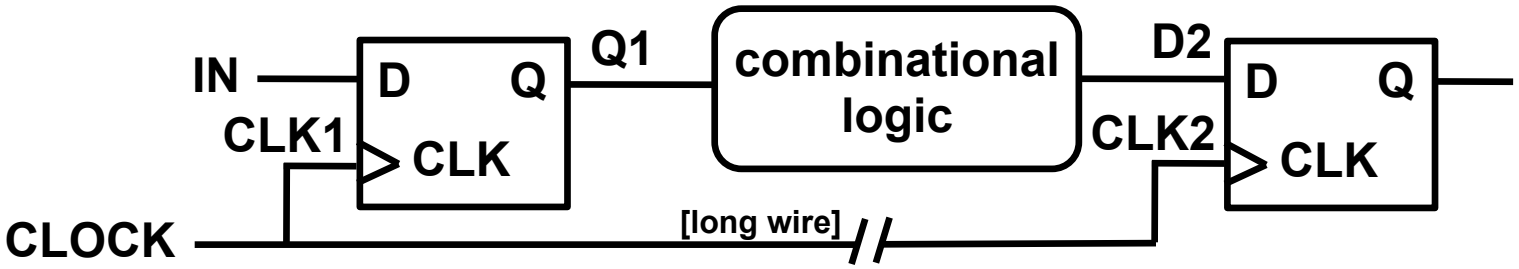
Setup Time With Worst Case Clock Skew

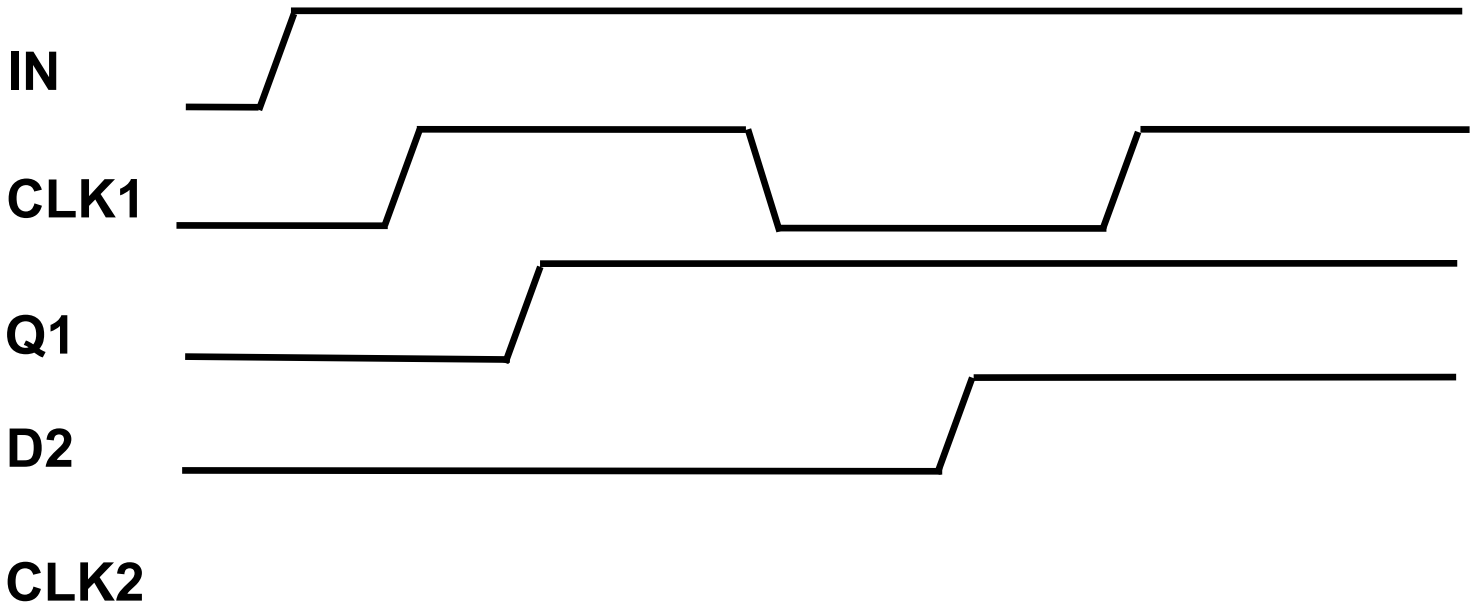




$$t_{clk} \geq t_{ffpd(max)} + t_{comb(max)} + t_{setup} + t_{skew(max)}$$

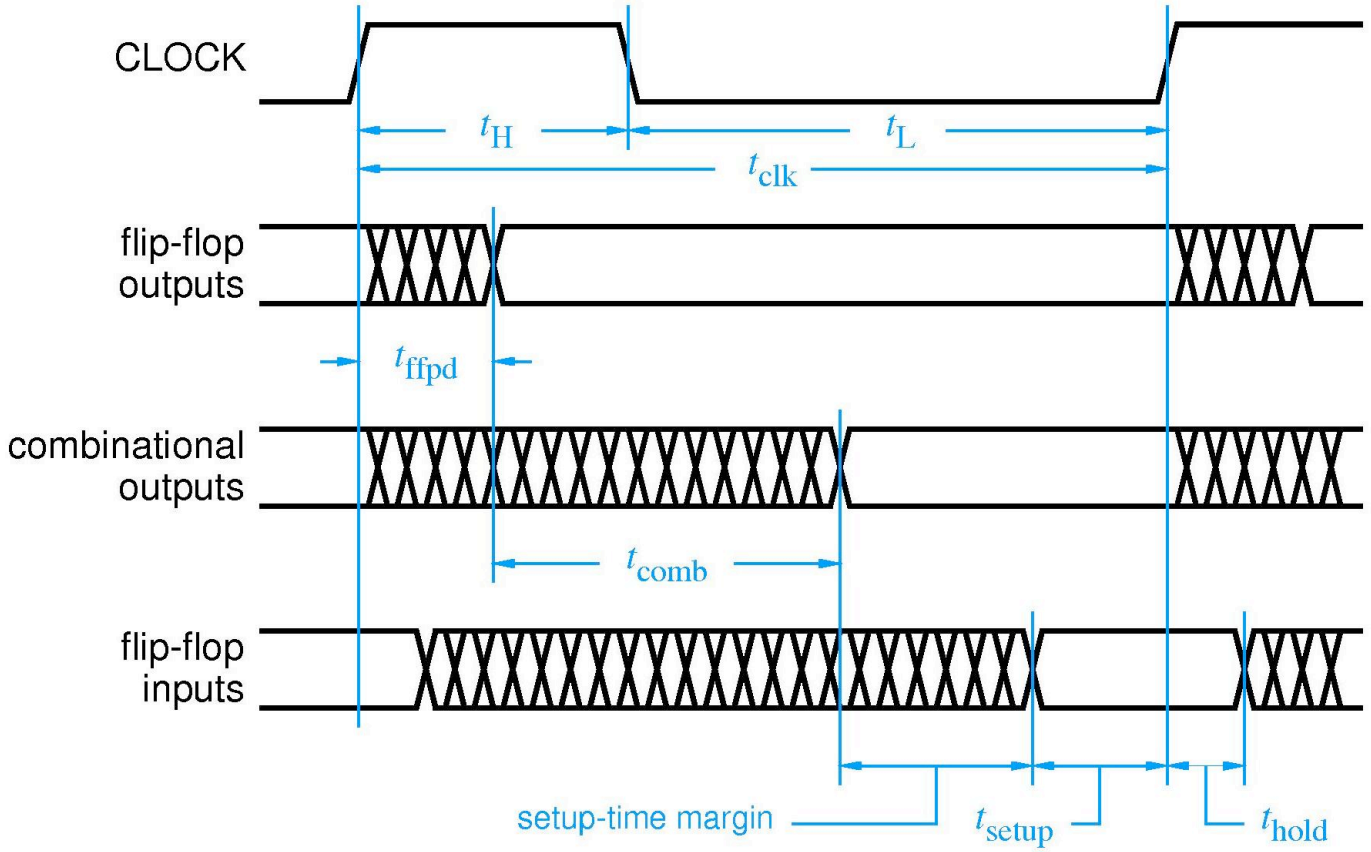
What About This Situation?



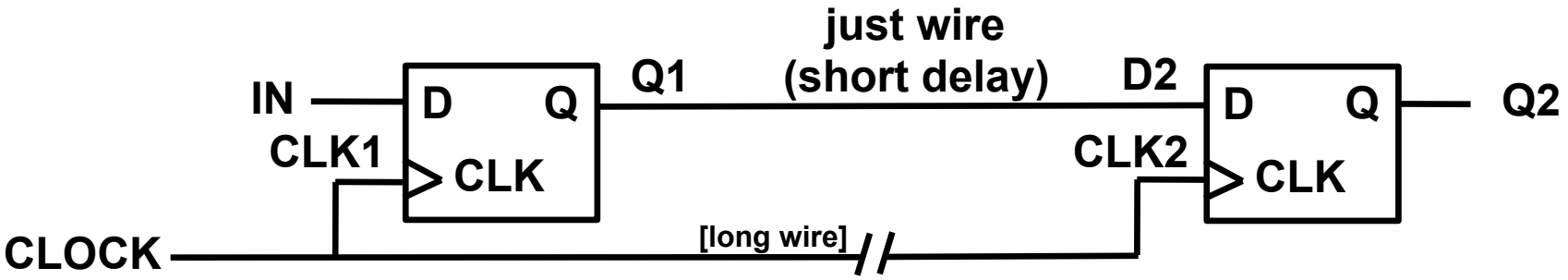


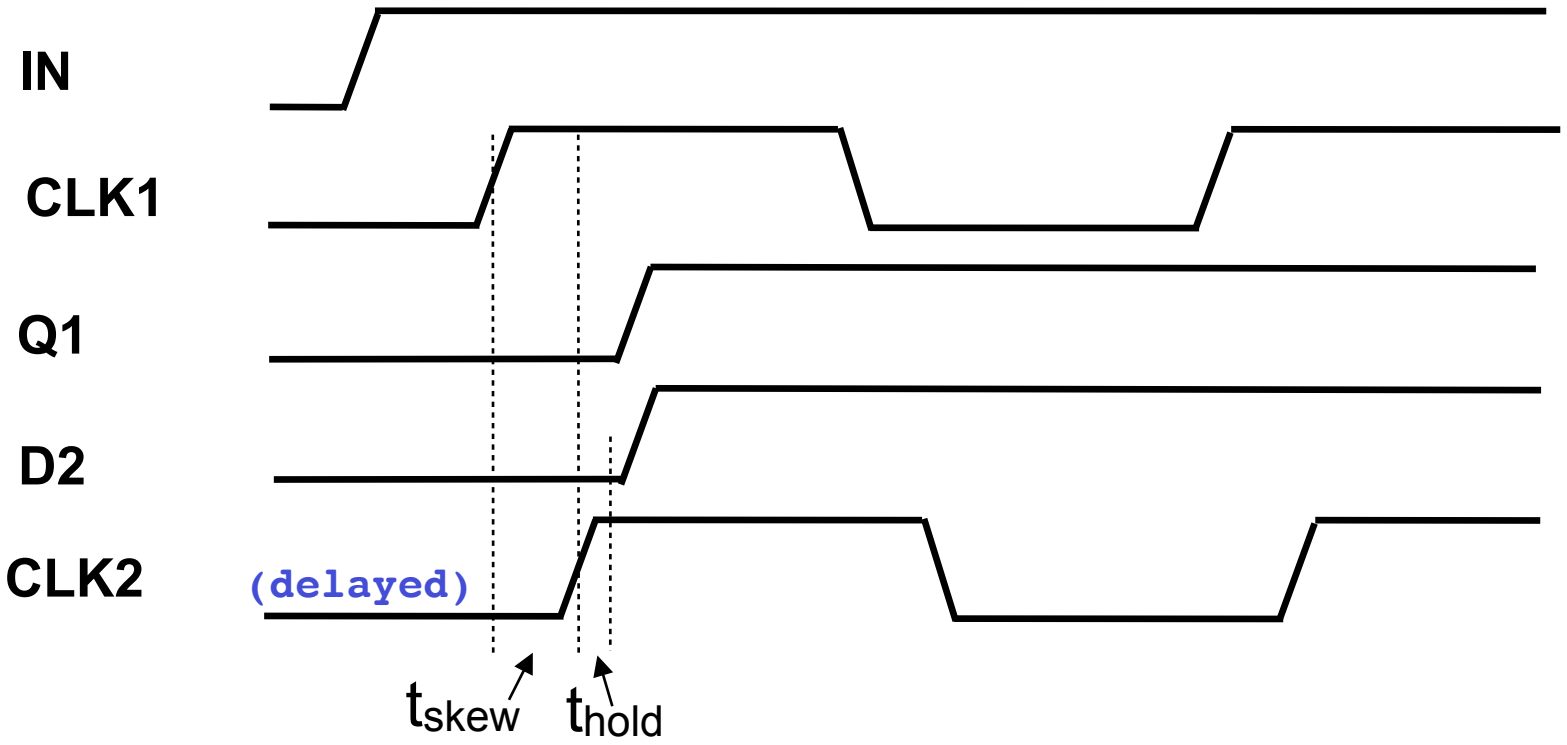
Hold Time

- **FF input must stay stable t_{hold} after the triggering FF clock transition**



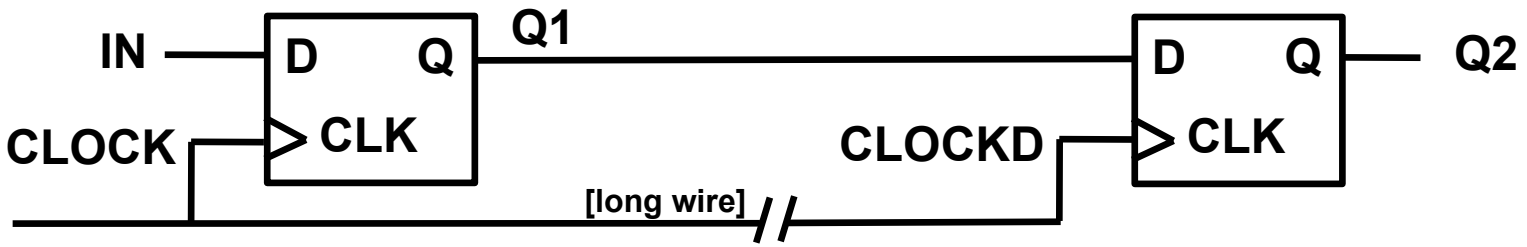
Hold Time With Clock Skew

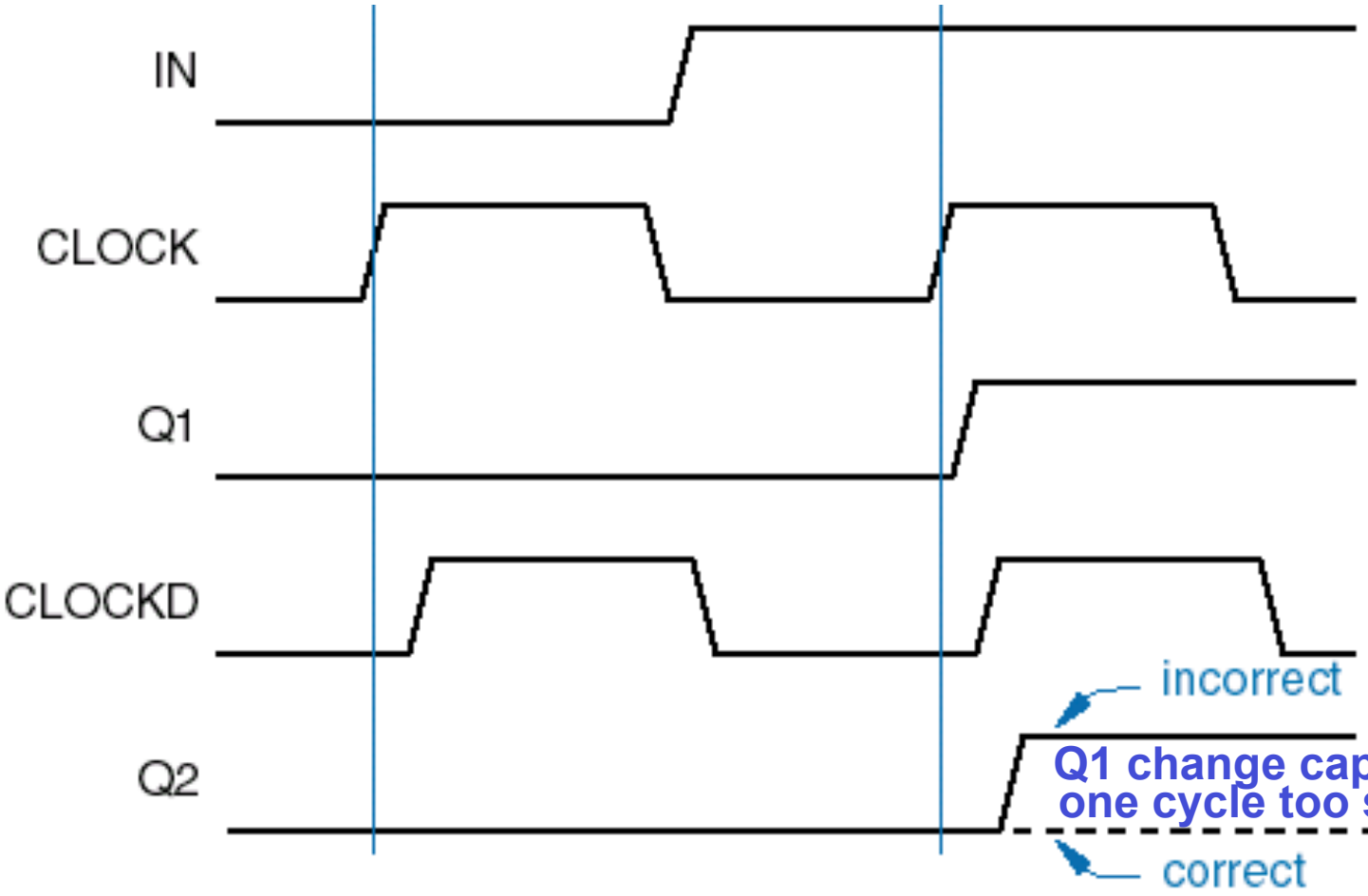




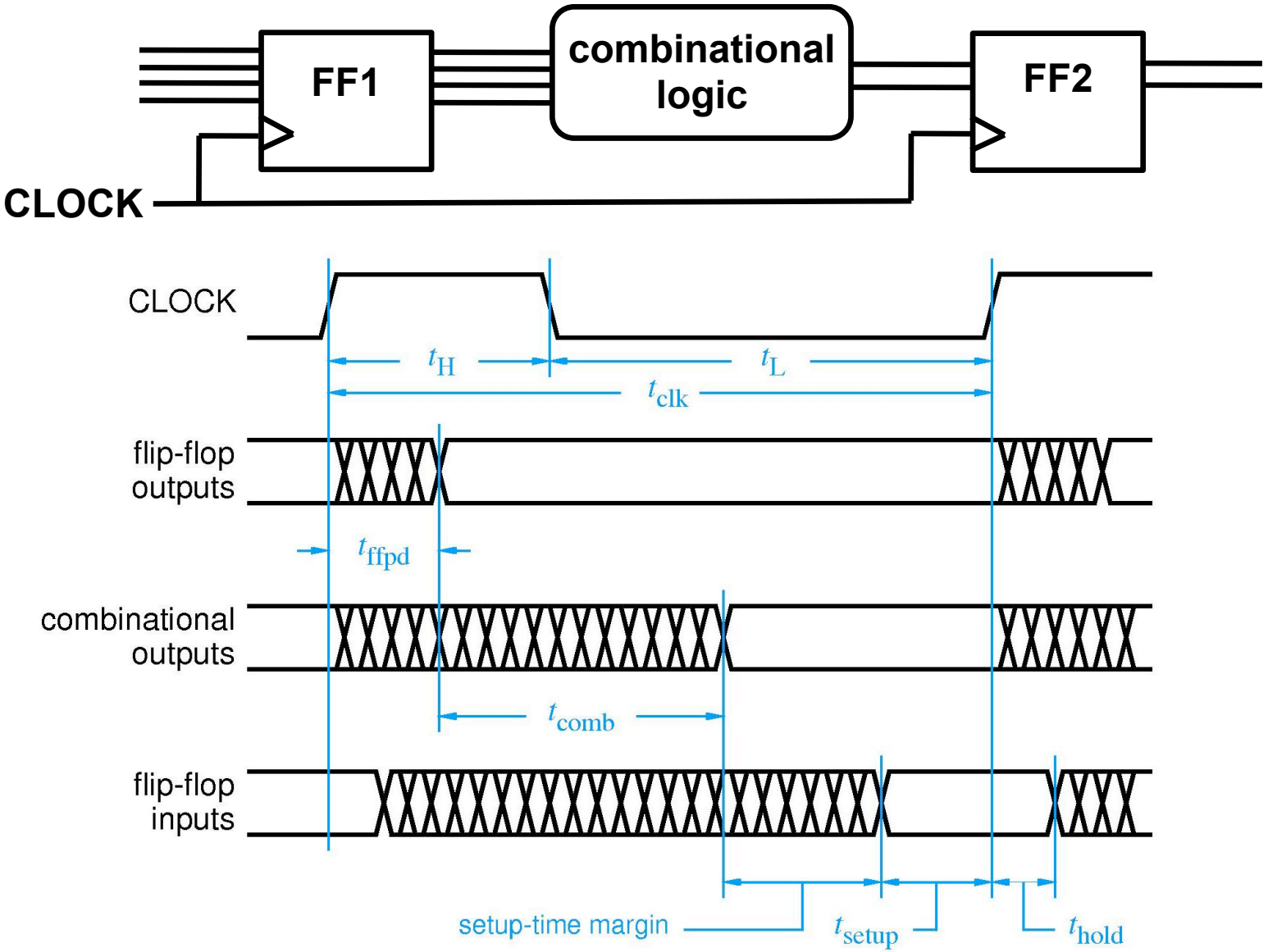
$$t_{ffpd(min)} + t_{comb(min)} - t_{hold} - t_{skew(max)} \geq 0$$

Could Even Clock the Wrong Data!

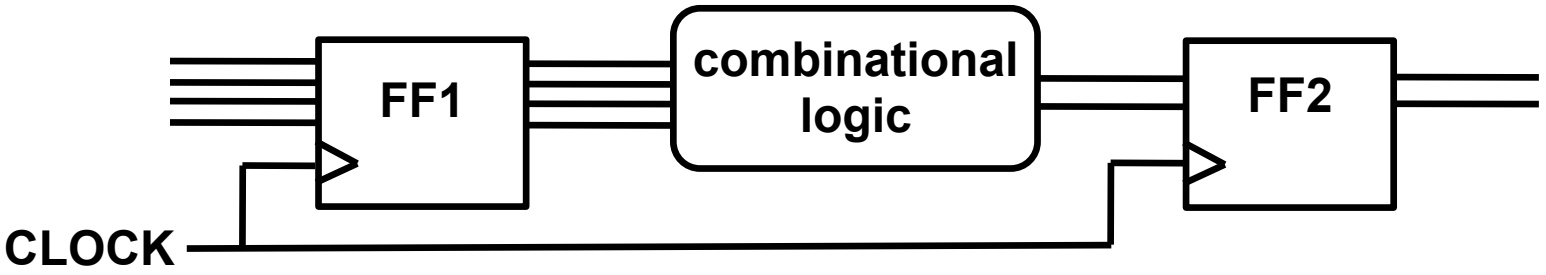




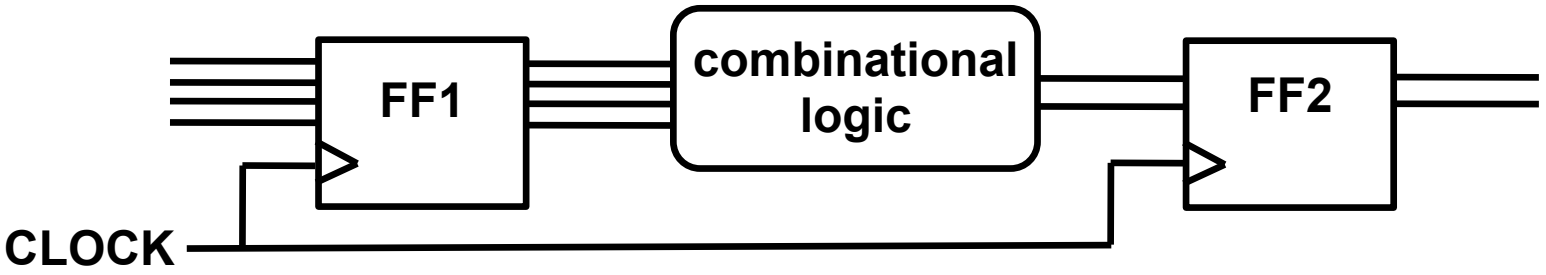
Setup and Hold Time Calculations



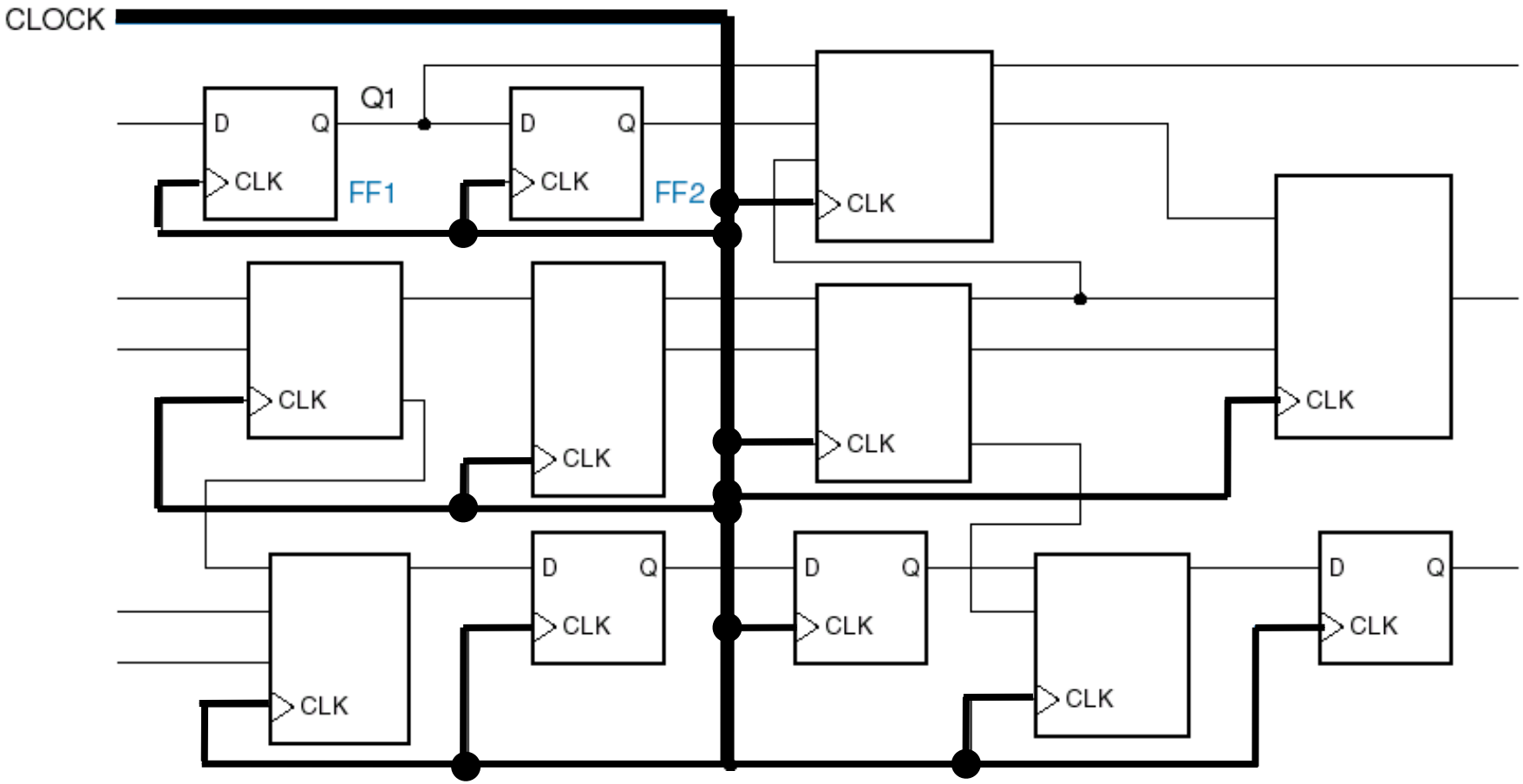
Setup and Hold Time Calculations



Setup and Hold Time Calculations

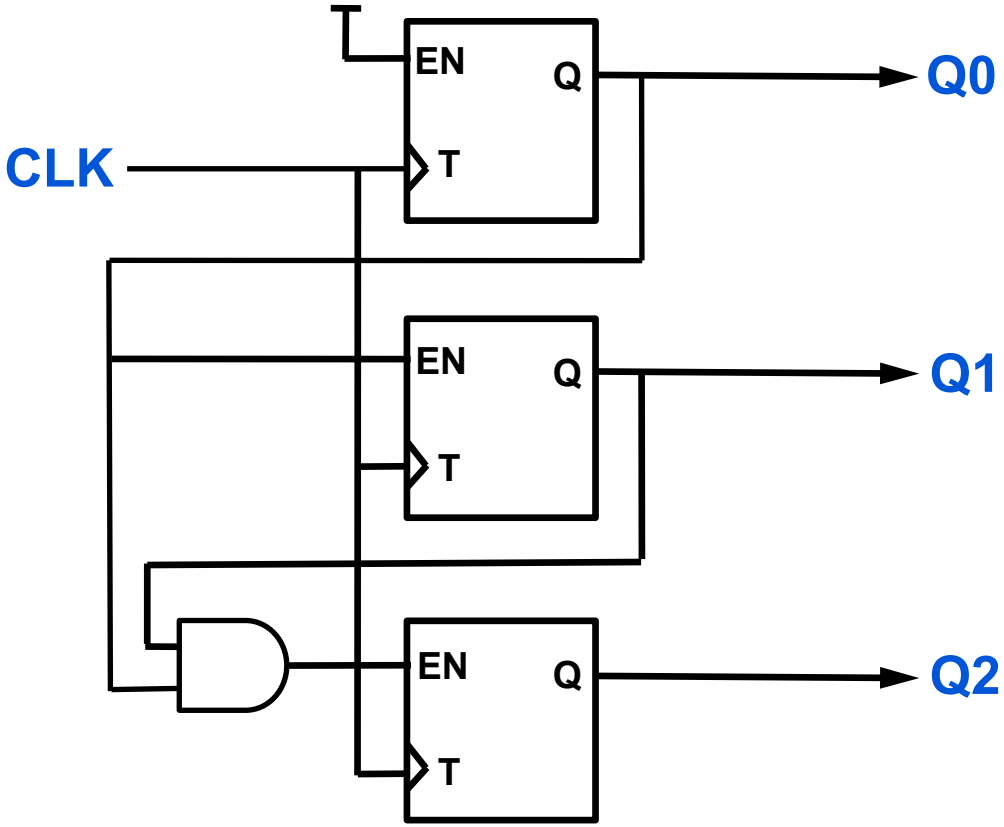


Clock Distribution



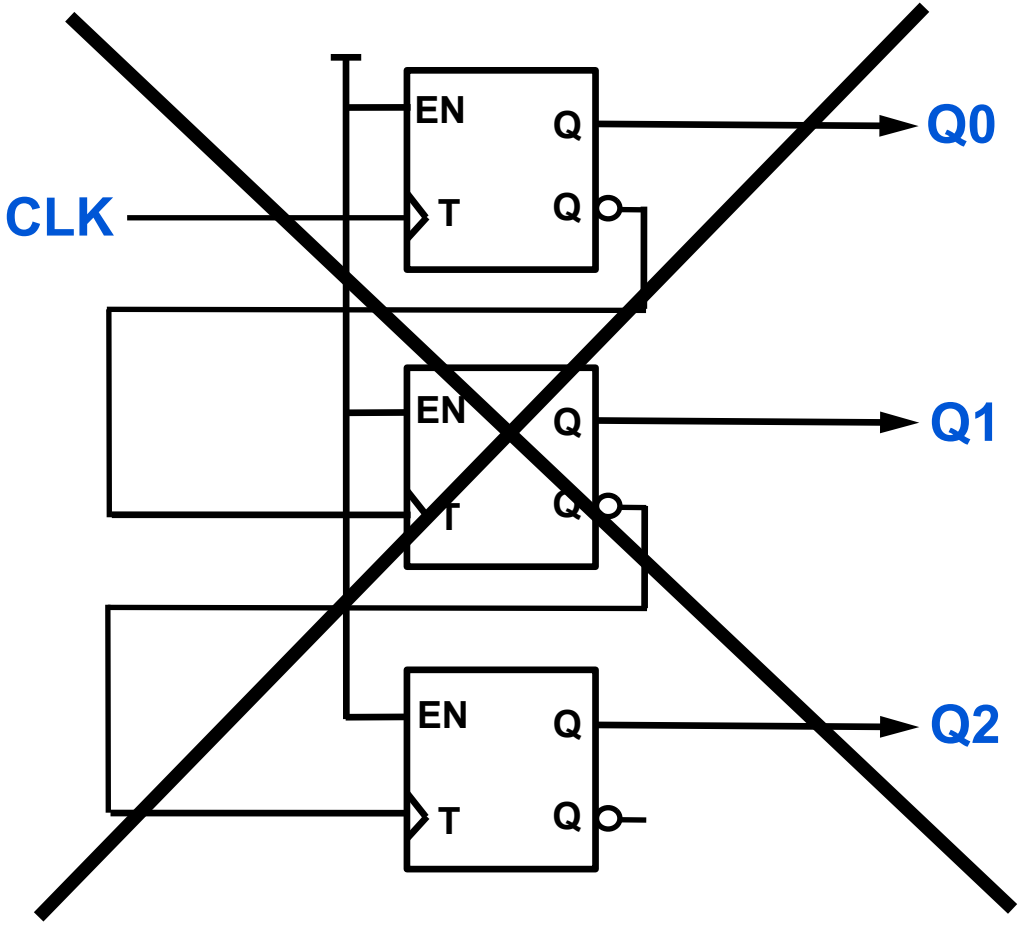
- Tree-like structure (often an “H-tree”)
- Dedicated metal layers (avoid noise, routing contention)
- Wide metal lines (low R ➔ low RC time constant)
- Clock buffers for large clock trees

Binary Up Counter Revisited



Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0
0	0	1

Binary Up Counter Revisited



Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0
0	0	1

Avoid the temptation to mess with the clock input!

Before Next Class

- H&H 1.4, 5.1-5.2.6

Next Time

Metastability

Binary Arithmetic