# ECE 5990

## Note 7

## Circuit Components in UHF Tags

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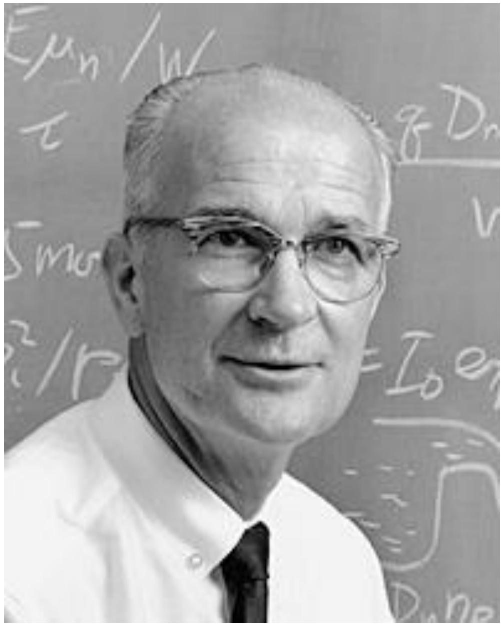
# Outline

- Tag architecture
- Analog, RF and digital circuit components
- RF-to-DC converter and voltage regulator
- Random number generator
- Baseband circuits and considerations
- Frequency strategy in mod/demod

# Quotable Quotes

“Frequently, I have been asked if an experiment I have planned is pure or applied science; to me it is more important to know if the experiment will yield **new and probably enduring knowledge** about nature. If it is likely to yield such knowledge, it is, in my opinion, good fundamental research.  This is more important than whether the motivation is purely aesthetic satisfaction on the part of the experimenter on the one hand, or the improvement of the stability of a high-power transistor on the other.”



William Shockley
(1910 - 1989)

# Tag Classification

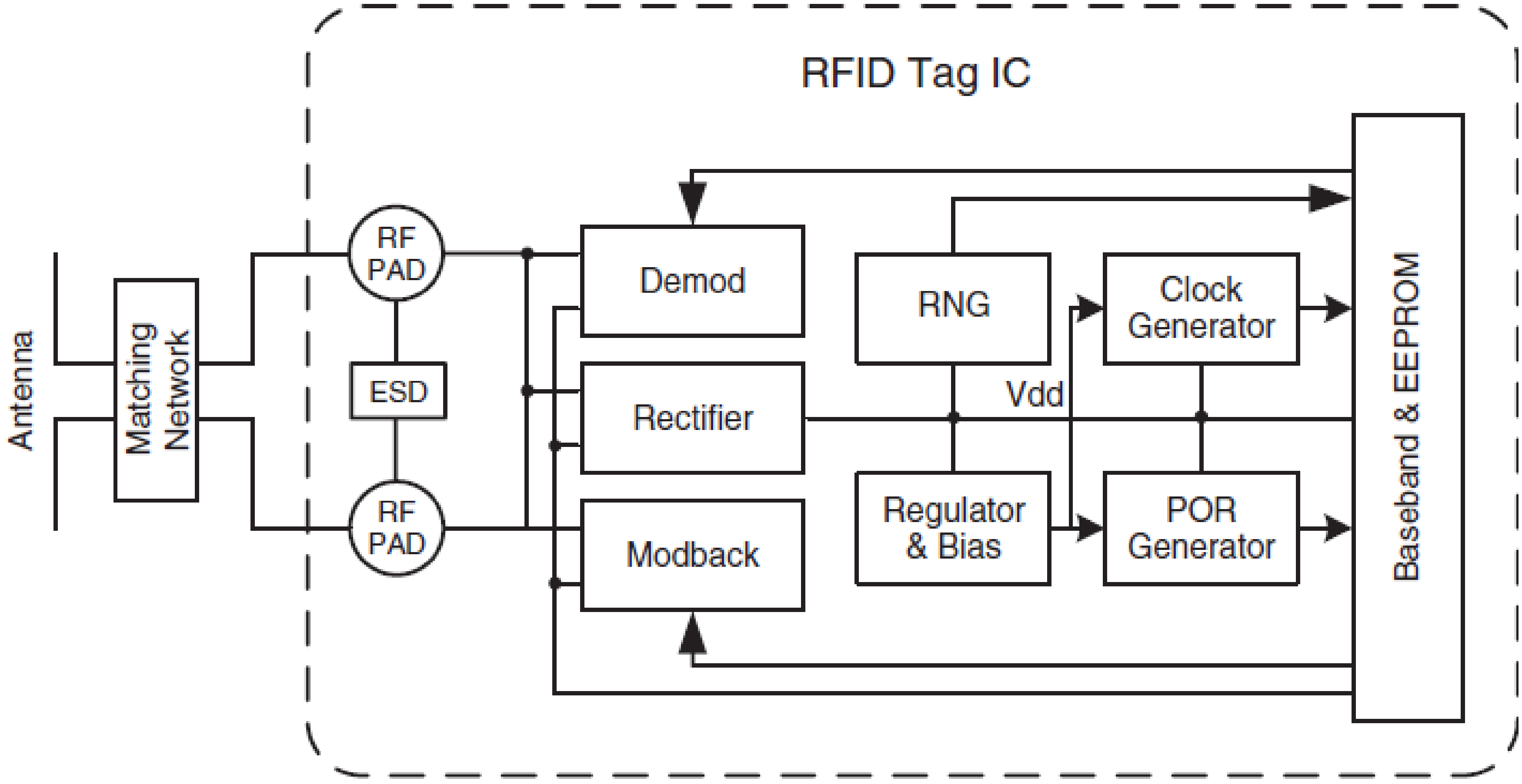
- Class 1: Identity tags
  - An electronic production code (EPC) identifier
  - A "kill" function permanently disable the tag
  - Optional password protected access
  - Optional tag memory
- Class 2: Higher functionality tags
  - An extended tag ID (128 – 1,024 bits)
  - Extended user memory
  - Authenticated access control
  - Extendable features (such as locating)
- Class 3: Semi-passive tags
  - An integral battery or stable power source
  - Sensor integration interface
- Class 4: Active tags
  - Protocols for tag-to-tag communications
  - Active communications in channel selection
  - Protocols to support advanced Ad hoc network

Each higher-class tag has backward compatible features

# System Requirements of UHF Tags

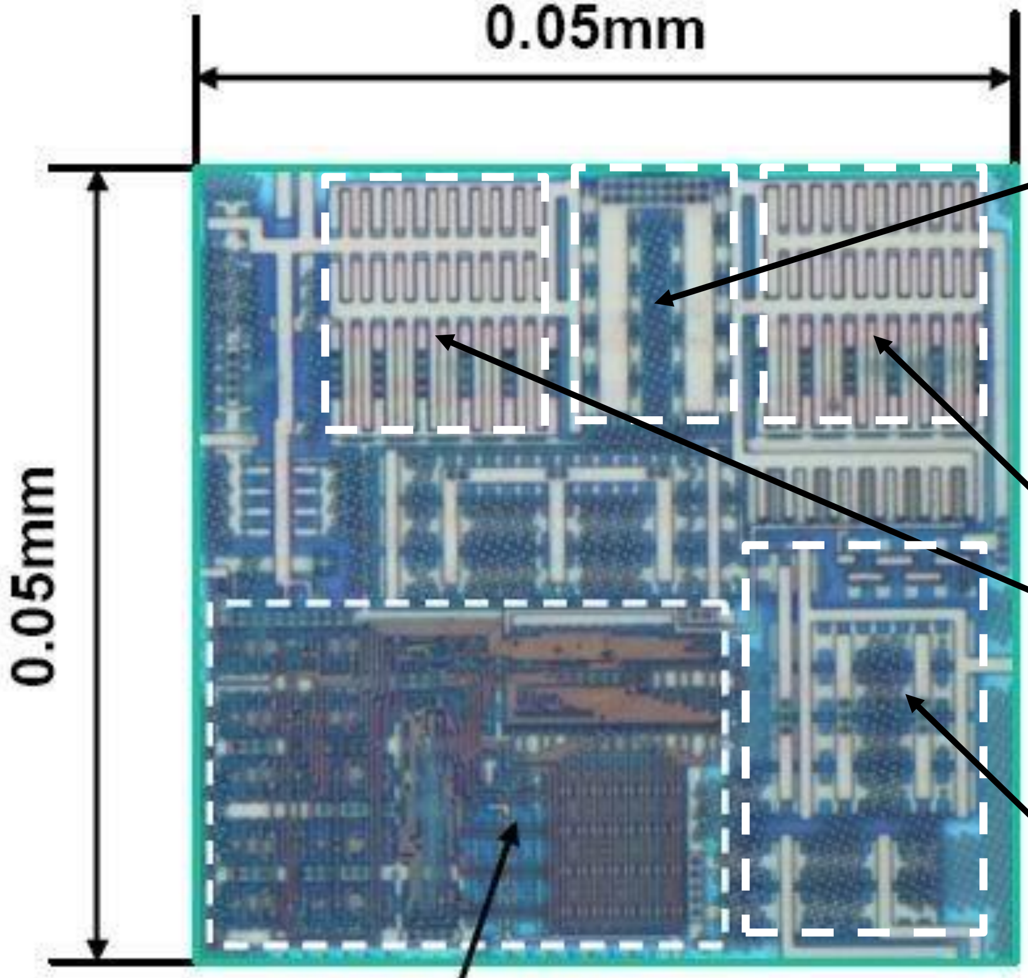
- Very low power consumption
  - Passive (scavenging RF power to DC): the tag power consumption most often sets the tag sensitivity and hence read range
  - Active (include a small battery for long-life operation)
- Very low prices for applications of logistics, tickets, and personal ID.
- Small size and weight

# Architecture for UHF RFID Tags



- As few contact pads as possible (save packaging cost)
- Mixed-signal (RF, analog, eNVM and digital: complex and difficult voltage discipline.

# Layout Example of A UHF Tag Chip



Contact vias and ESD protection

Top metal layer not shown

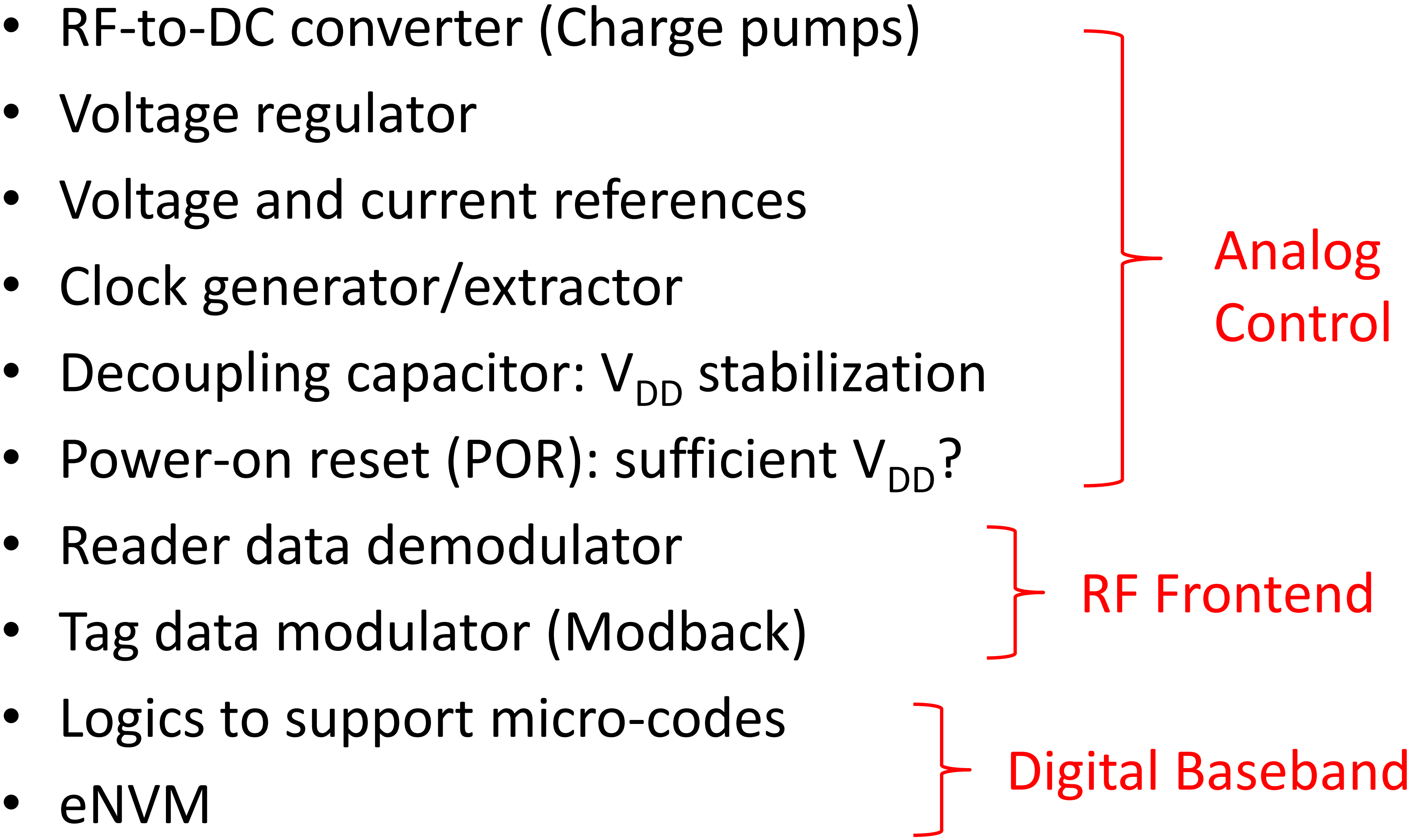
Inductive matching network

Digital logic

128-bit Specific EEPROM (21μm×32μm); Cell area: 3.96μm$^2$

SMIC 180nm CMOS

# Circuit Components on RFID Tags



- RF-to-DC converter (Charge pumps)
- Voltage regulator
- Voltage and current references
- Clock generator/extractor
- Decoupling capacitor: $V_{DD}$ stabilization
- Power-on reset (POR): sufficient $V_{DD}$?

Analog Control

- Reader data demodulator
- Tag data modulator (Modback)

RF Frontend

- Logics to support micro-codes
- eNVM

Digital Baseband

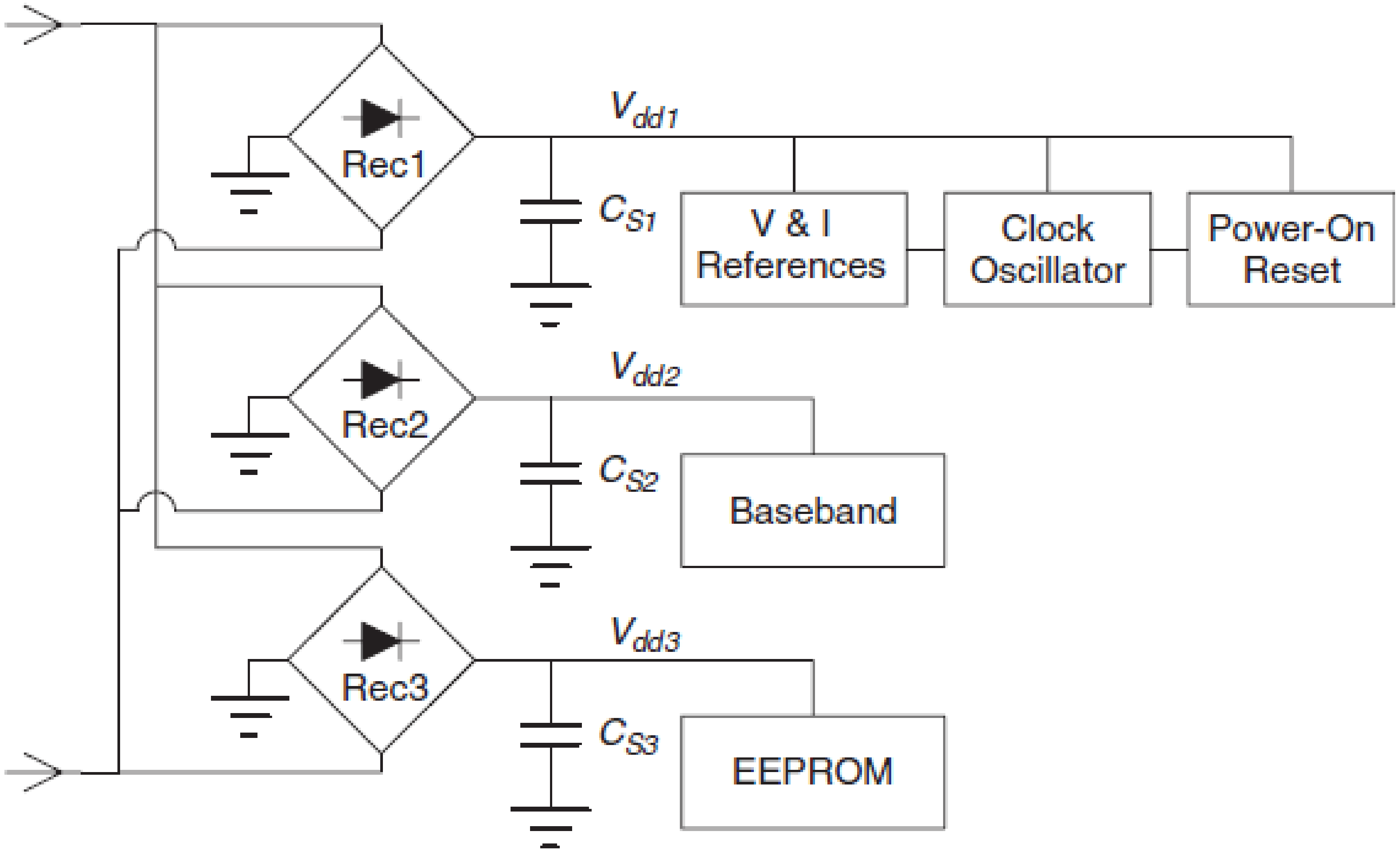
# Low-Power Frontend Tag Circuits

- A typical tag sensitivity at -18dBm: 16$\mu$W (28 mV $V_{pp}$ for 50$\Omega$)
- Power conversion efficiency of 50% gives only 8$\mu$W to frontend circuits
- In addition to fitting the total power budget over the long time, the peak power is severely limited
  - Battery system just needs to prolong the battery life and can allow large peak power with small duty cycle
  - Tags can only have limited decoupling capacitor

$$V_{op} \cdot I_{op} \propto \frac{1}{d^2}$$

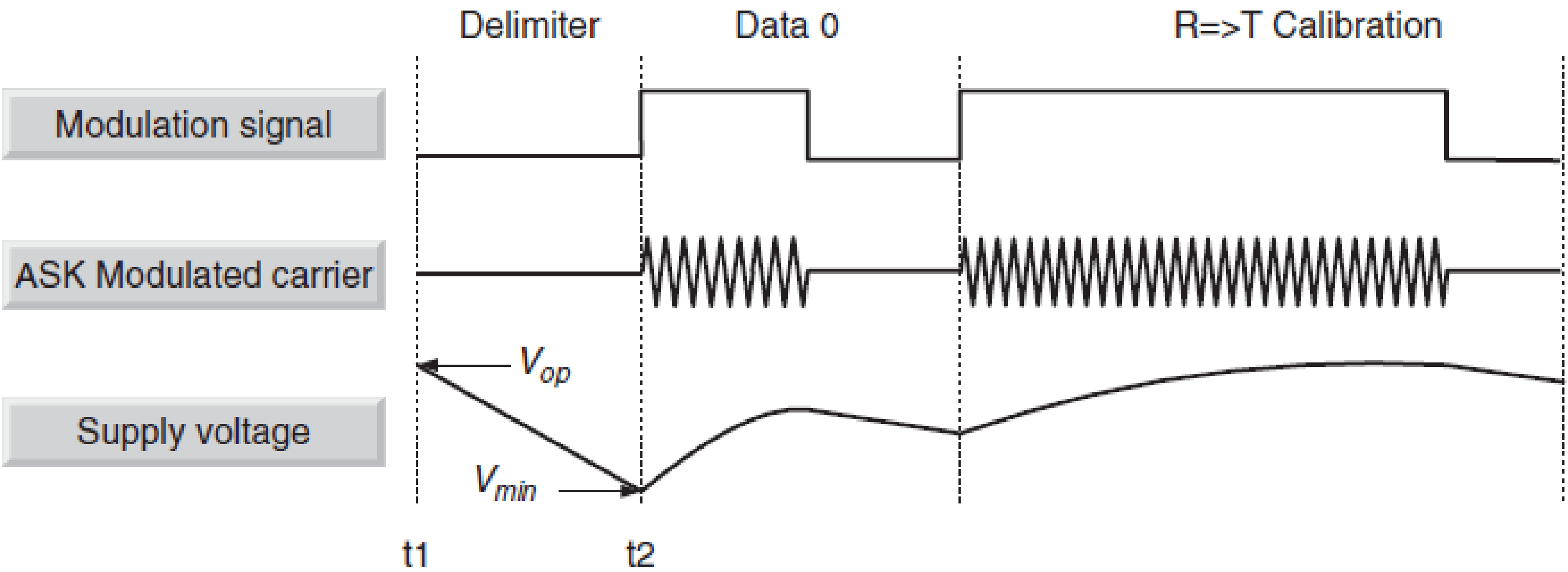
$$I_{op} \leq I_{allowed}$$

# Multi-Level Power Supply



- Power discipline: turn on at different time; less cross line-noise interference;

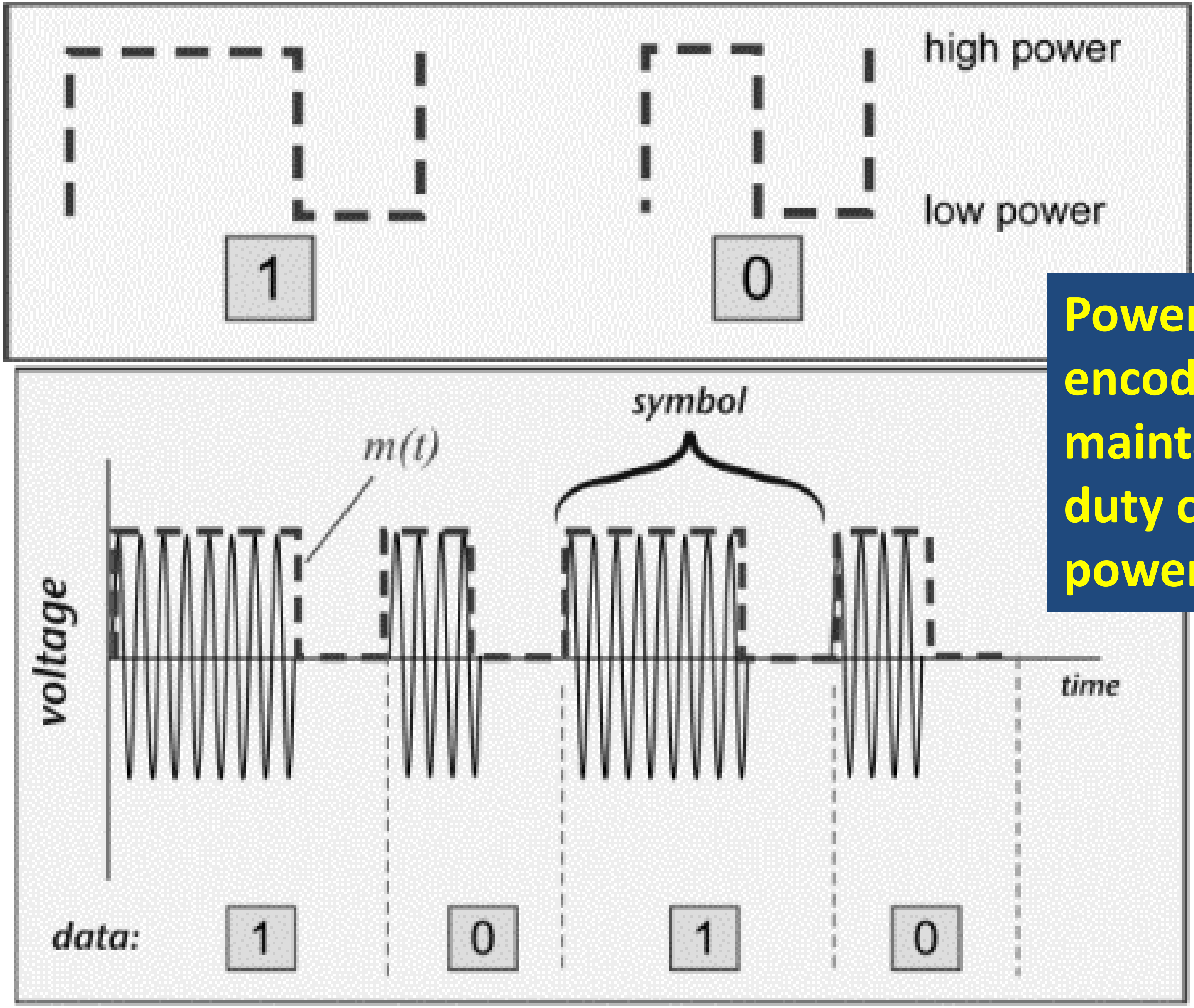
# “Frame Synchronization” Power Scheme



$$C_s\left(V_{op} - V_{\min}\right) = \int_{t1}^{t2} I_{op}\,dt$$

- $V_{min}$ for each block is the minimum voltage to maintain operation without error.
- Low $V_{min}$ can extend range and reduce required $C_s$

# ASK or PIE Modulation in RFID



Power interval encoding (PIE) to maintain > 50% duty cycle for power harvesting

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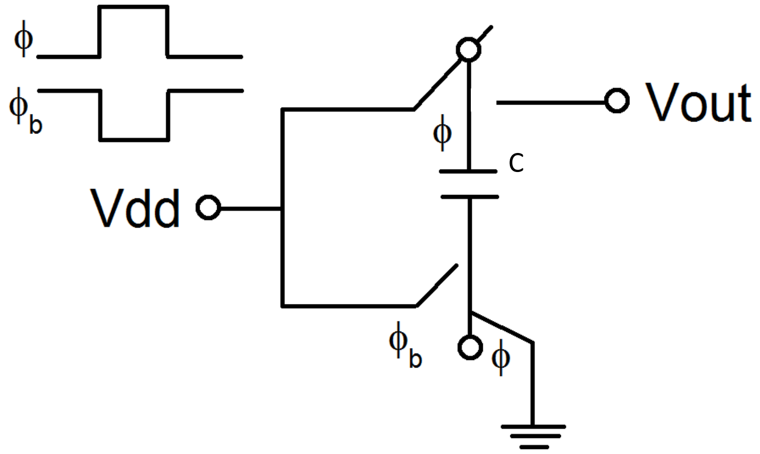
# Bucket Capacitor



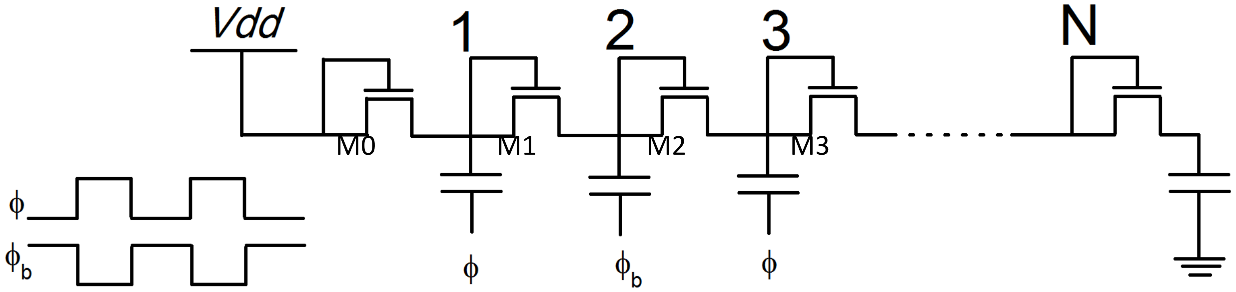
Each time during ϕ is high, and $\phi_b$ is low, the capacitor can assume

$$Q = C \cdot V_{dd} = C \cdot \left(V_{out} - V_{dd}\right)$$

When $\phi_b$ (bottom of the bucket capacitor) is raised to $V_{dd}$, $Q$ will be dumped to $V_{out}$ to increase. $V_{out}$ will stop increasing when after switching, the transfer change will be zero.

$$C \cdot V_{dd} = C \cdot \left(V_{out} - V_{dd}\right) \Rightarrow \quad V_{out} = 2V_{dd}$$

# Dickson N-Stage Charge Pump



$$\Delta V = V_{n+1} - V_n = V_\phi - V_{th}$$

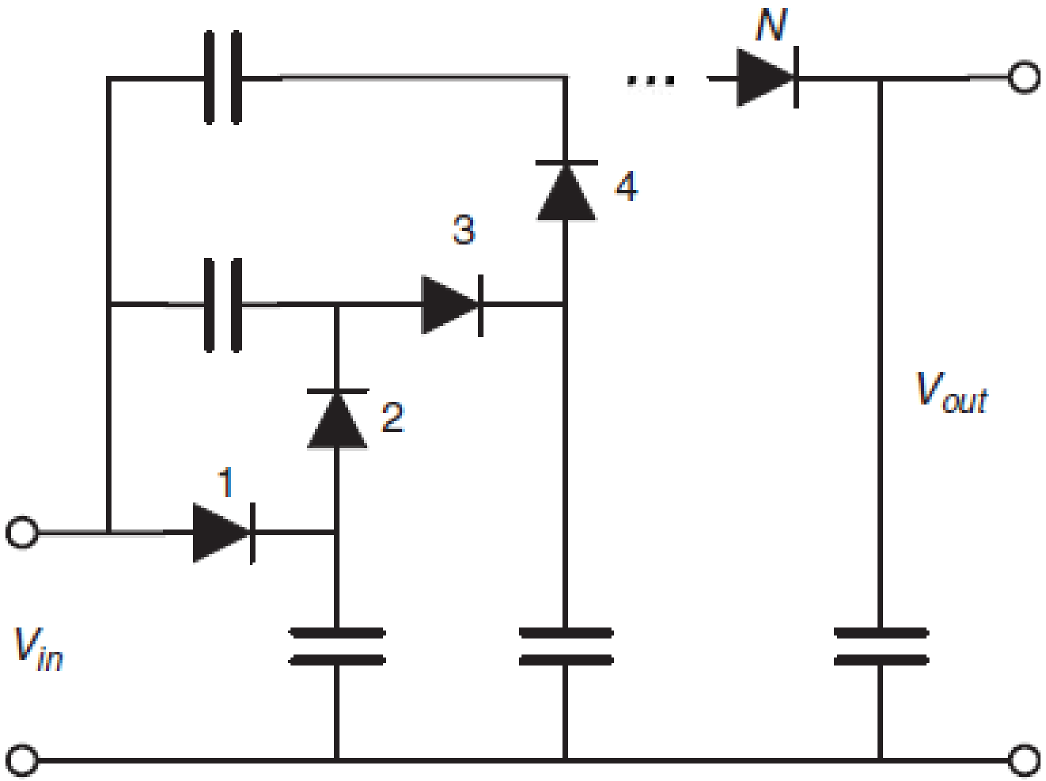
$$V_1 = V_{dd} + V_\phi - V_{th}$$

$$V_2 = V_{dd} + \left(V_\phi - V_{th}\right) - V_{th}$$

$$V_{out} = V_{dd} + N\left(V_\phi - V_{th}\right) - V_{th}$$

$$V_{out} = V_{dd} + N\left(V_\phi - V_{th} - \frac{I_{out}}{C \cdot f}\right) - V_{th}$$

# Single-Clock Dickson N-Stage Charge Pump



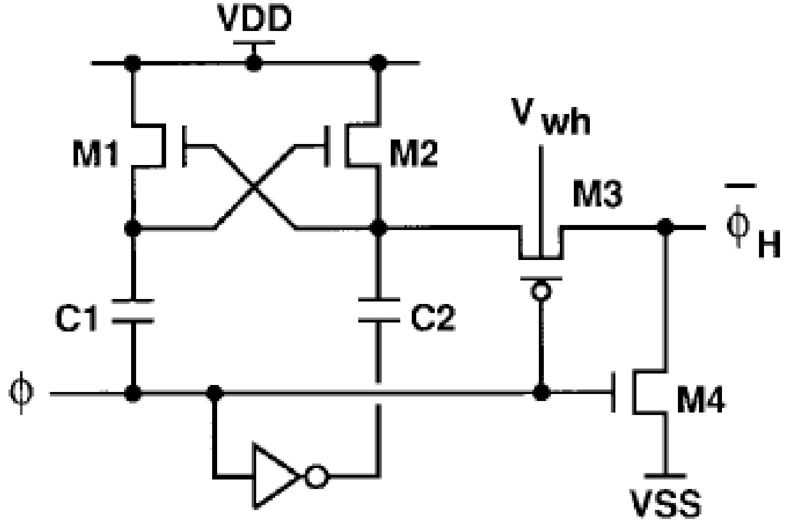
Penalty for single clock

$$V_N = N\left(V_\phi - \boxed{2}V_{th} - \frac{I_{out}}{C\cdot f}\right) + V_{th}$$

Check when no load: $V_1 = V_\phi - V_{th};\ V_2 = 2V_\phi - 3V_{th}$

# Hierarchical Charge Pump

- Dickson has linear growth per stage, and can be too slow (stage increase =$V_{\phi} - V_{th}$)
- Hierarchical clock: Use a generated stable DC to give a new clock with higher amplitude
- With ideal diodes (zero leakage and ON-resistance), hierarchical pump per generated clock will give progressive increase as Fibonassi numbers: 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, etc.

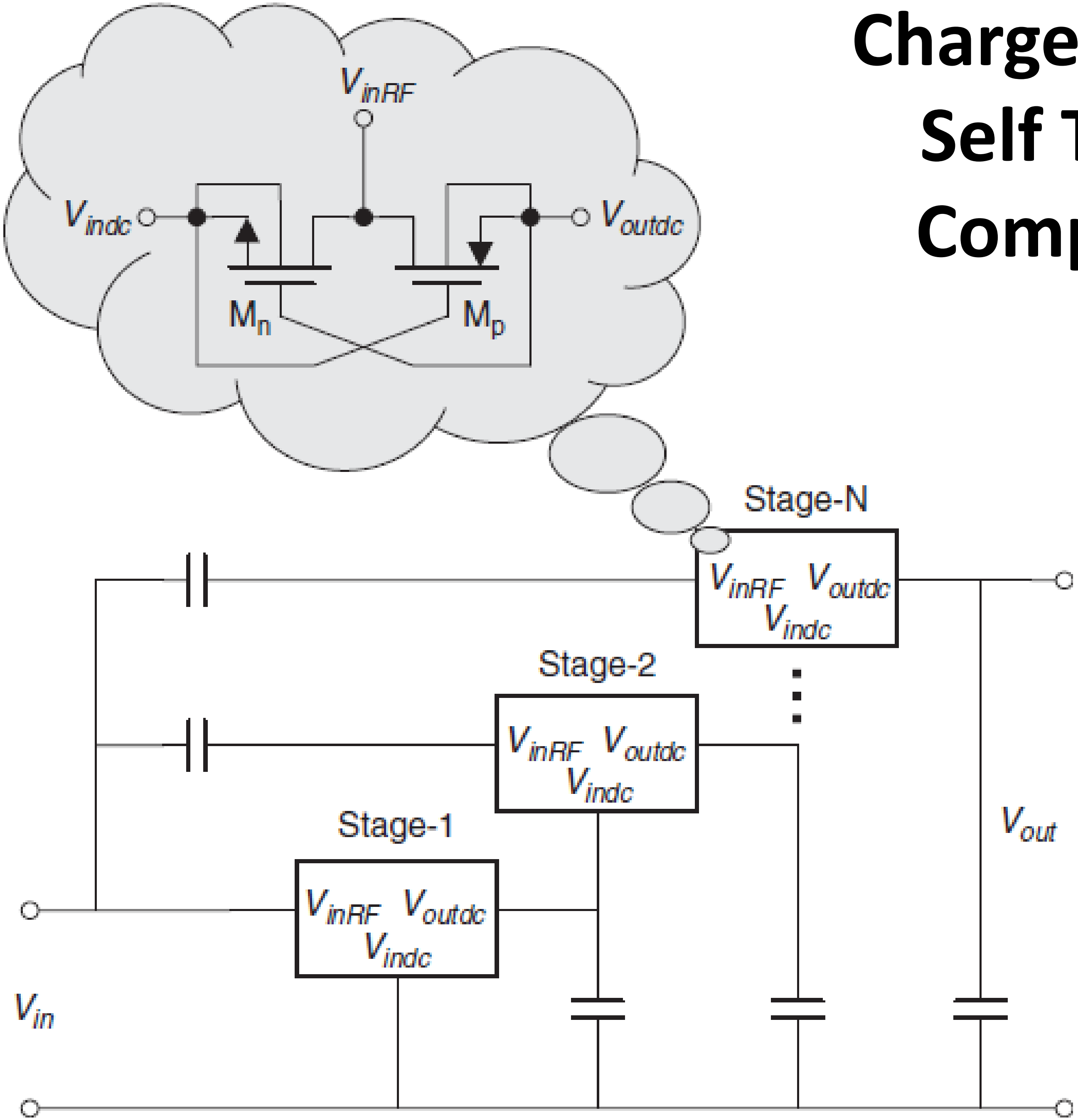


**High-voltage clock generator**

# Critical Charge Pump Parameters

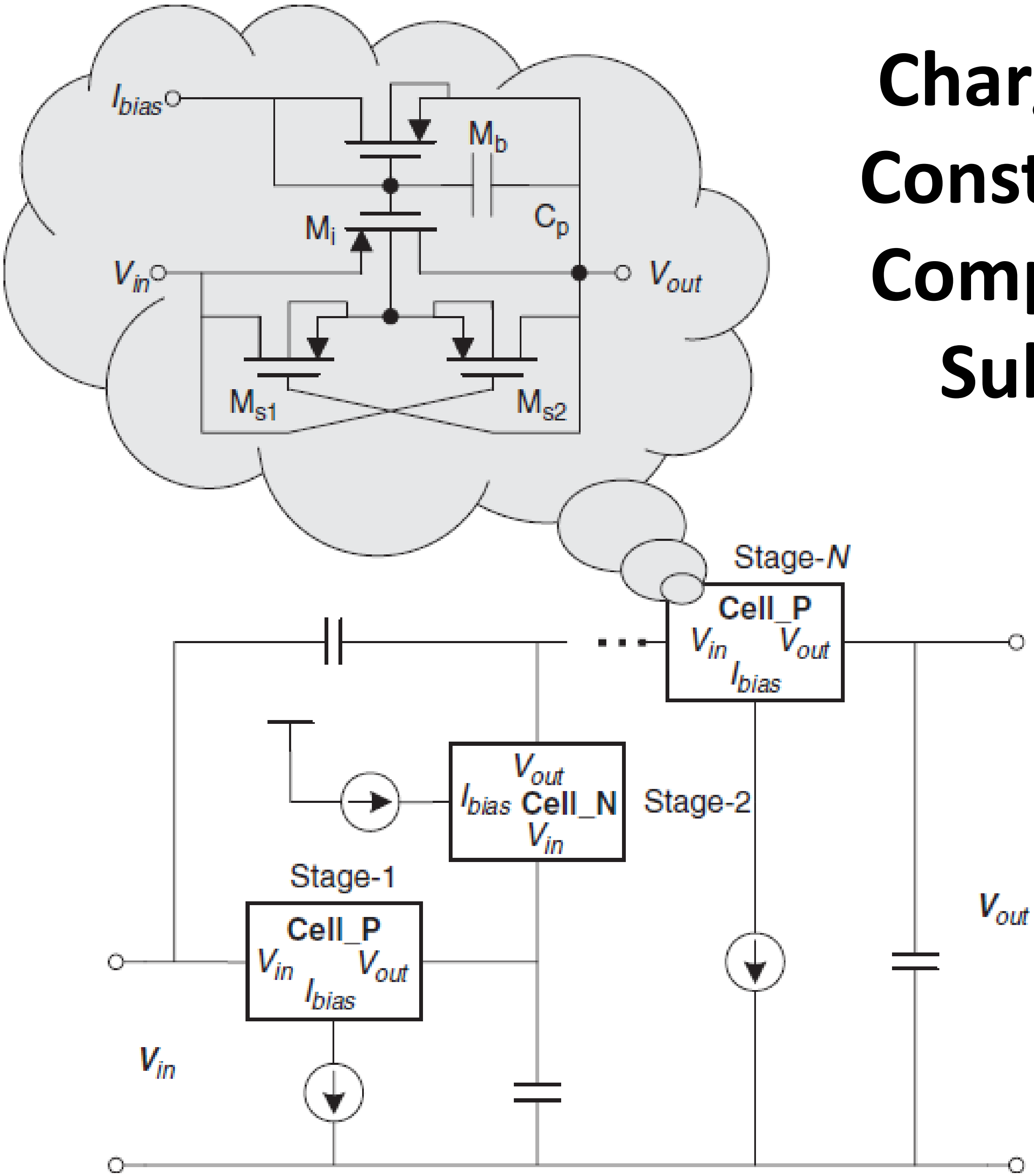
- ON voltage or $V_{th}$ of diode-connected MOSFET (as close to zero as possible)
- Magnitude of $V_{in}$
- Diode reverse leakage current at block voltage $(V_i - V_{i-1})$
- Capacitor leakage current at $V_i$
- Load resistance at $V_{out}$
- ON resistance for diode
- Magnitude of $C_i$ and Frequency of $V_{in}$ (time to reach output saturation)

# Charge Pump with Self Threshold Compensation



- Still needs very low $V_{th}$ to start
- $M_n$ and $M_p$ in the linear regions: less voltage loss
- Leakage when $V_{inRF}$ is low

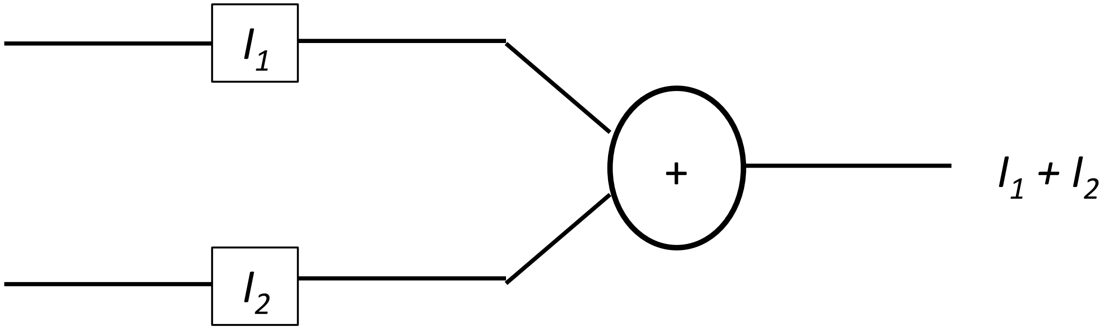
# Charge Pump with Constant Threshold Compensation and Substrate Shift



- Alternating P and N stages
- Require reference voltage and current sources: not suitable for passive tags.

# Group Exercise: System Stability

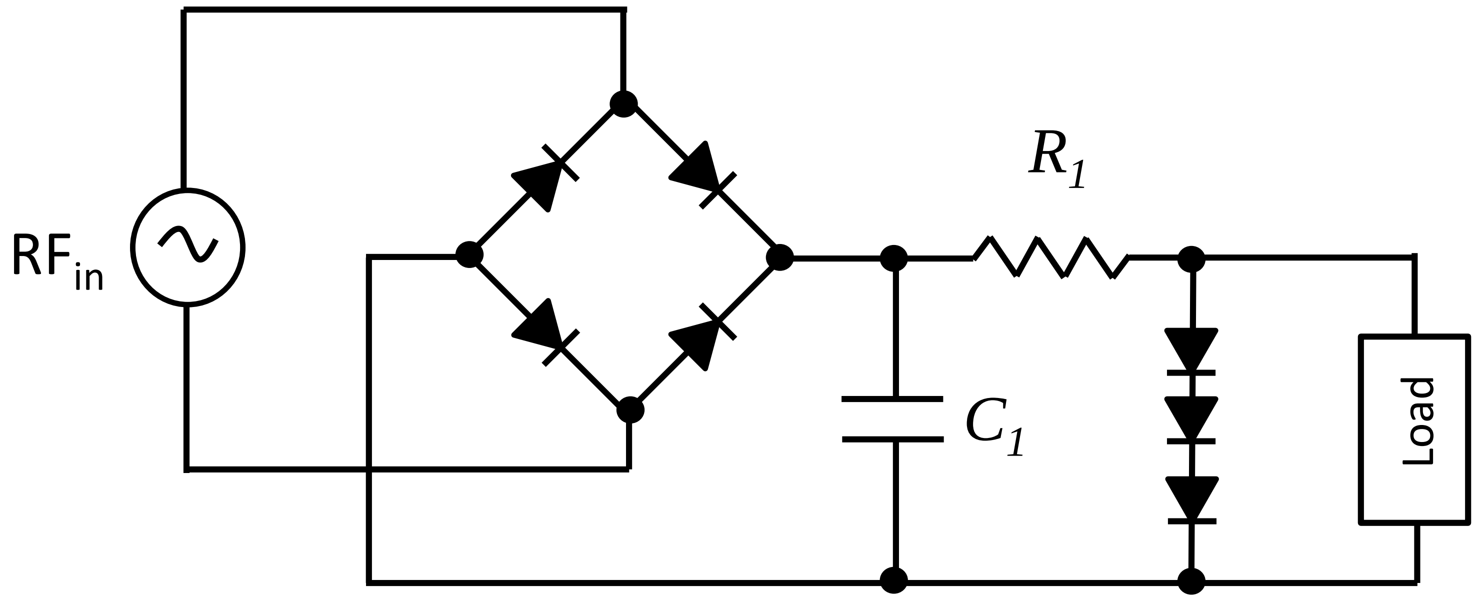
- Stable condition: $I_1 \cong I_2$
- $I_1 = I_{10} + \Delta I_1$; $I_2 = I_{20} + \Delta I_2$
- $\Delta I_1(S_{common}, S_{indep1})$; $\Delta I_2(S_{common}, S_{indep2})$;



# Voltage Regulator

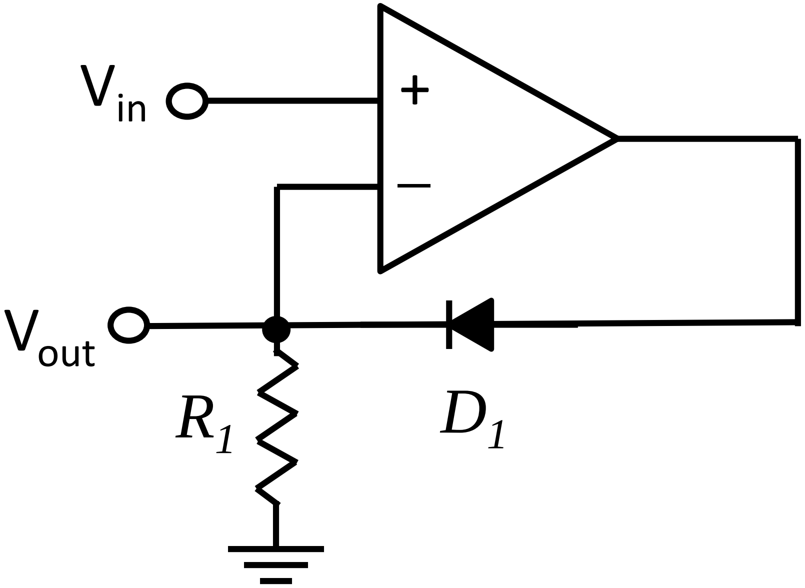
- Stabilize the supply voltage $V_{DD}$ to be less dependent of the load current.
- Minimal temperature coefficient for $V_{DD}$ under various current load.
- Ensure operations (80% $V_{DD}$) for a period (EPC Gen 2 standard = 12.5µs) when RF input is shut.
- Generating power-on reset (POR) pulse during wake-up.

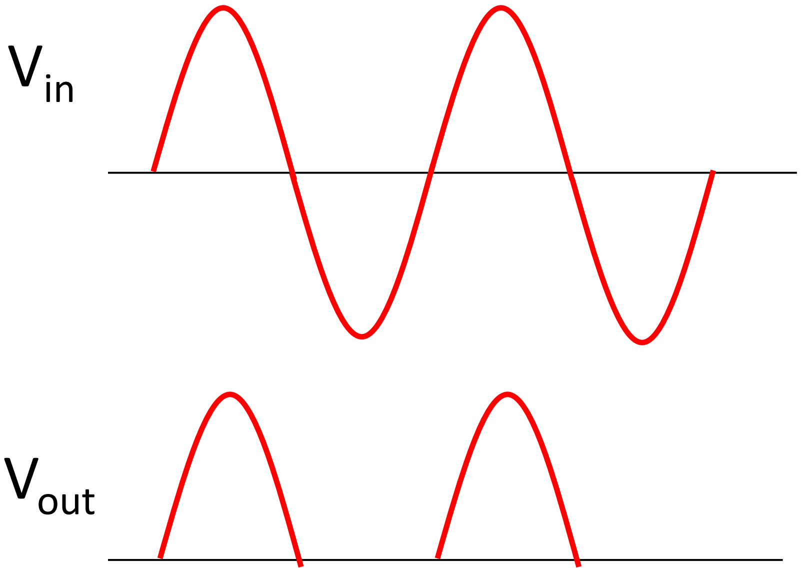
# Conventional Diode-Based Regulators



- The diodes in the bridge has near-zero $V_{ON}$; the diodes in the series has a reasonably large $V_{ON}$.
- Simple and passive in nature, but waste too much current
- Diode has very small series resistance.

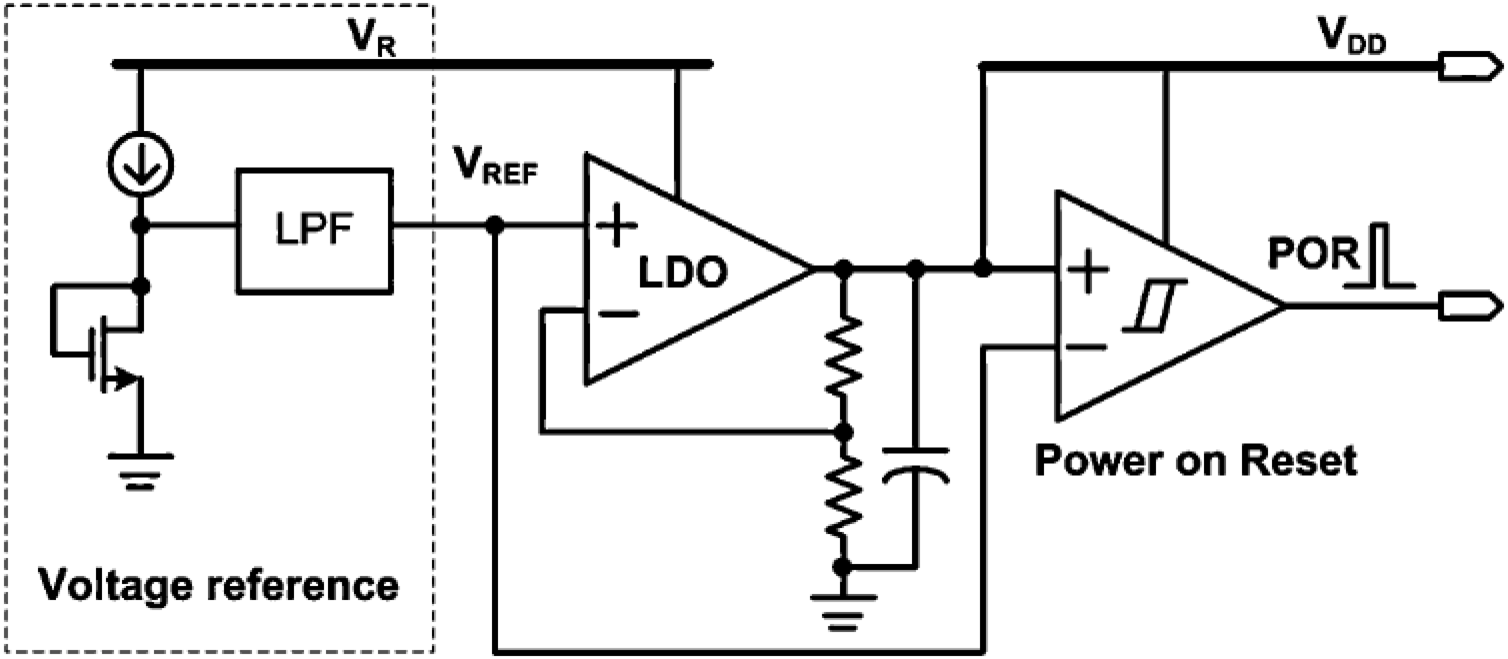
# Active Precision Rectifier





- Output independent of diode $V_{ON}$.
- Active circuits with large bandwidth OP AMP: impractical for RFID tags.

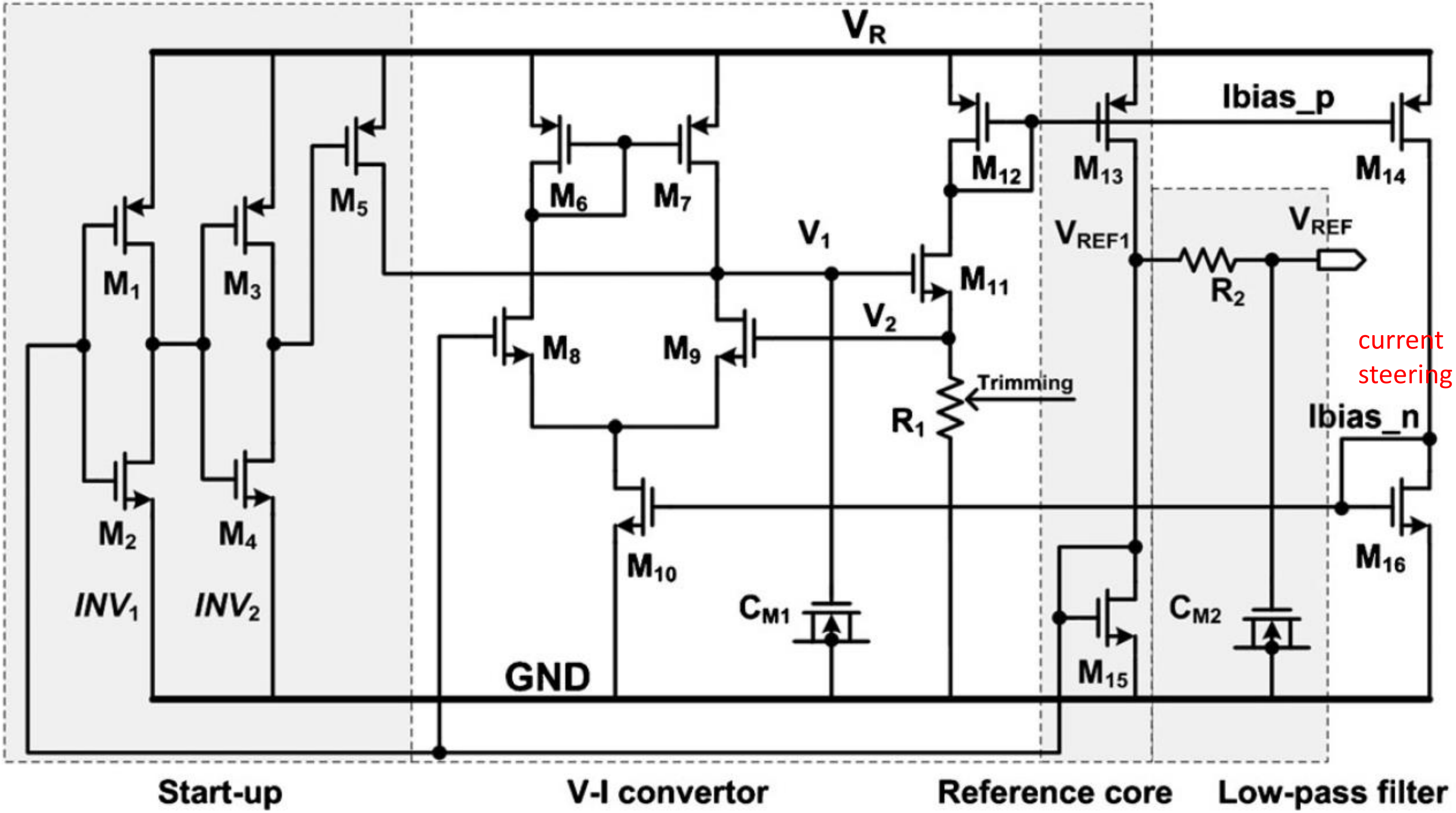
# RFID Voltage Regulator Design Exercises



- LPF: low-pass filter
- LDO: low drop-out: transfer stable $V_{REF}$ to $V_{DD}$.
- POR: power-on reset: whole-chip reset; sense $V_{DD}$ drop

J. Guo and K. N. Leung, “A CMOS voltage regulator for passive RFID tag ICs”, Intl. J. Circ. Theor. Appl., vol. 40, pp. 329 – 340, 2012.

# CMOS Voltage Regulator Circuits



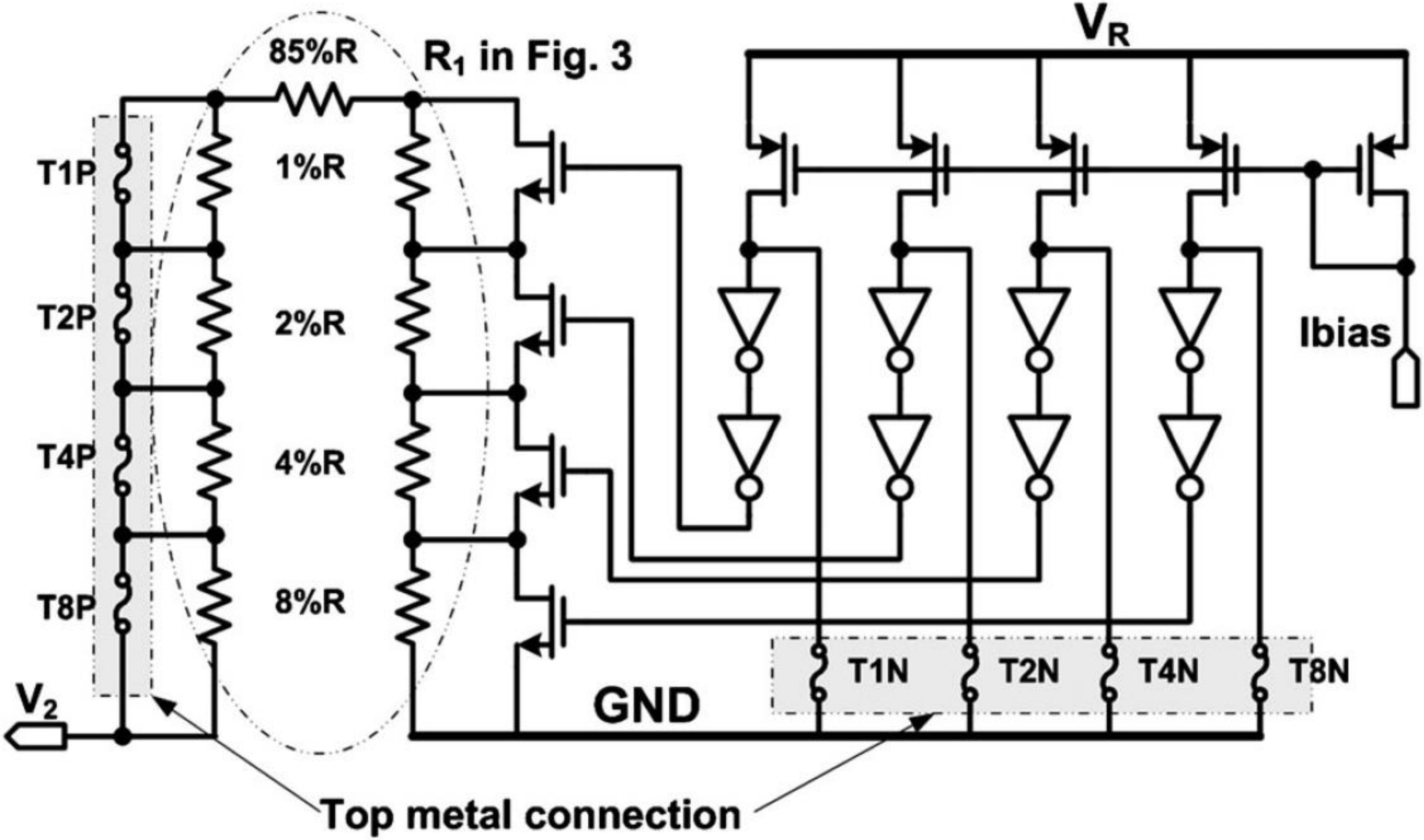
current steering

Generate $V_1$ to kick out of zero-current operating point

$V_{REF1}$ reaches the designed value (the switching threshold of $INV_1$), $M_5$ is off, all current mirror and steering will shut off.

$R_2$ and $C_{M2}$ form a LPF between $V_{REF1}$ and $V_{REF}$ to improve power supply rejection ratio and noise performance

# Process Variation and Temperature Compensation by Resistor Laser Trimming



# Temperature Compensation Strategy

From the current mirrors:

$$V_{REF} = V_{THN} + \sqrt{\frac{2I_{D15}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{15}}}$$

$$V_{REF} = V_{THN} + \sqrt{\frac{2V_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{15} R_1}}$$

Zero temperature coefficient (ZTC) for $V_{REF}$:

$$\frac{\partial V_{REF}}{\partial T} = 0 \quad \Rightarrow \frac{\partial V_{THN}}{\partial T} = \sqrt{\frac{I_{D15}}{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{15}}} \cdot \left(\frac{1}{\mu_n}\cdot\frac{\partial \mu_n}{\partial T} + \frac{1}{R_1}\cdot\frac{\partial R_1}{\partial T}\right)$$

Known temperature dependence:

$$V_{THN} = V_{THN0}\left(1 - t_{c1VT}\left(T - 25\right)\right)$$

$$\mu_n = \mu_{n0}\left(1 - t_{c1\mu}\left(T - 25\right)\right)$$

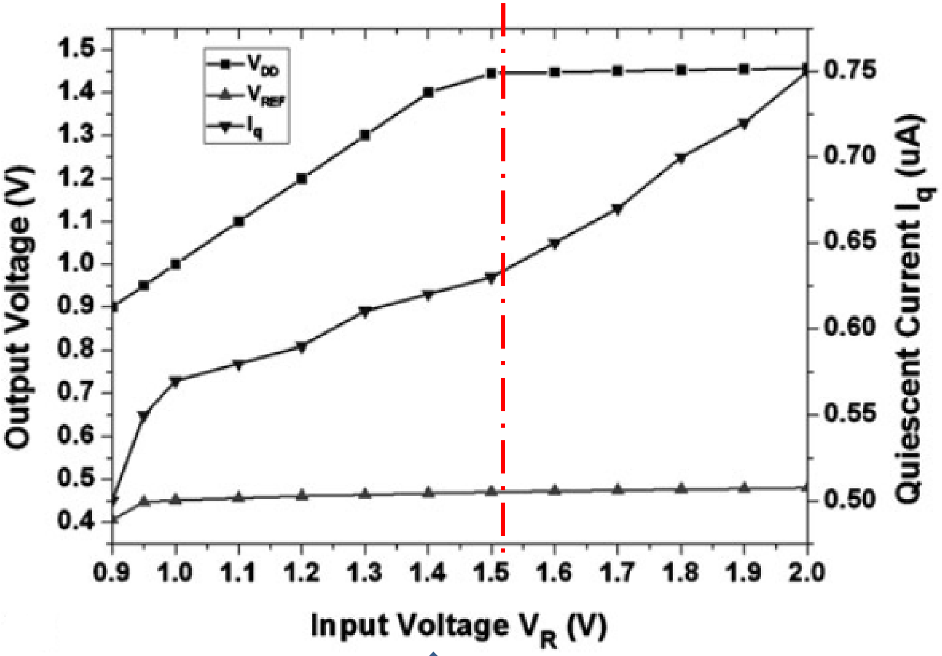
$$R_1 = R_{10}\left(1 + t_{c1R}\left(T - 25\right)\right)$$

Set:

$$\left(\frac{W}{L}\right)_{15} \equiv \frac{I_{D15}}{2\mu_n C_{ox} t_{c1VT}^2} \cdot \left(\frac{t_{c1\mu}}{\mu_n} + \frac{t_{c1R}}{R_1}\right)^2$$

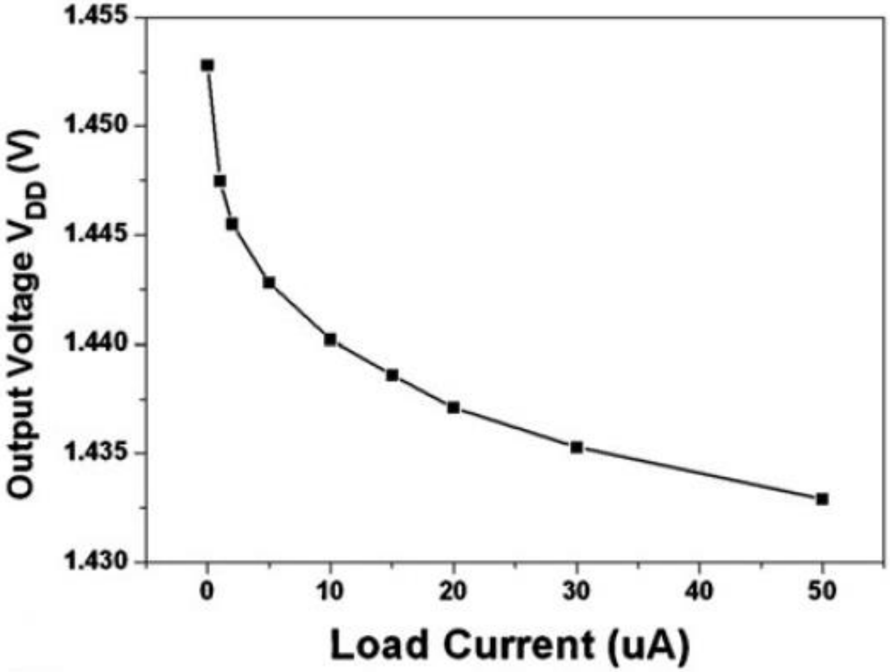
**Additional laser trimming of $R_1$ values after calibration!!!**

# Regulator Performance vs. $V_R$ and $I_{load}$

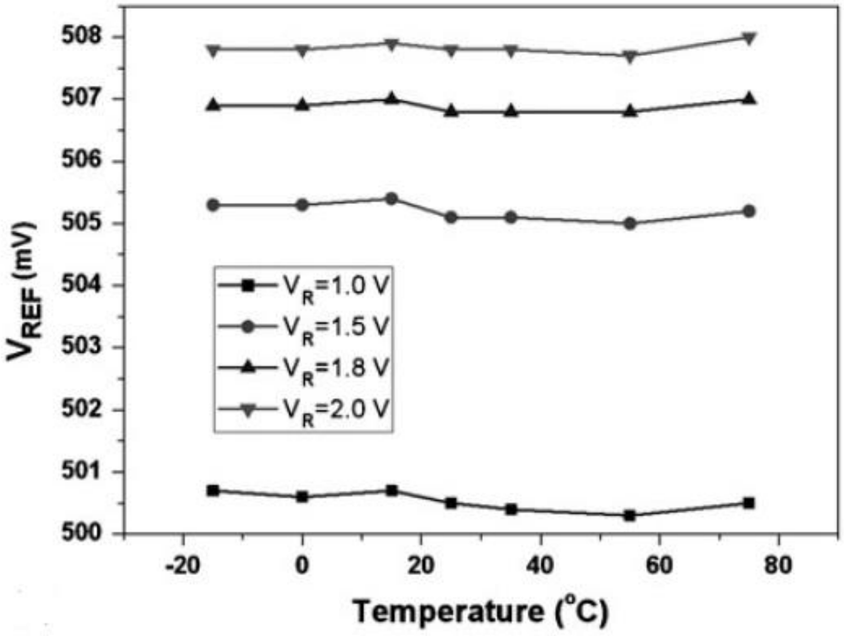


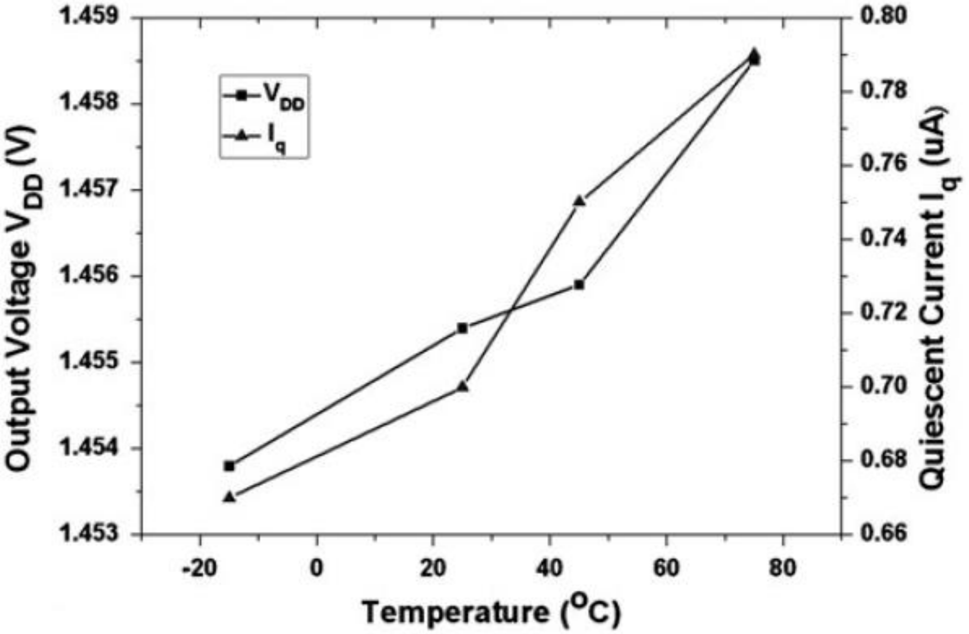
Charge pump/rectifier needs to output above 1.5V before $V_{DD}$ stabilized. Transistors with smaller $V_{th}$ can lower that requirement at the expense of larger $I_q$

$V_{DD}$ less than 10% variation for $I_{load}$ between 0A and 50μA



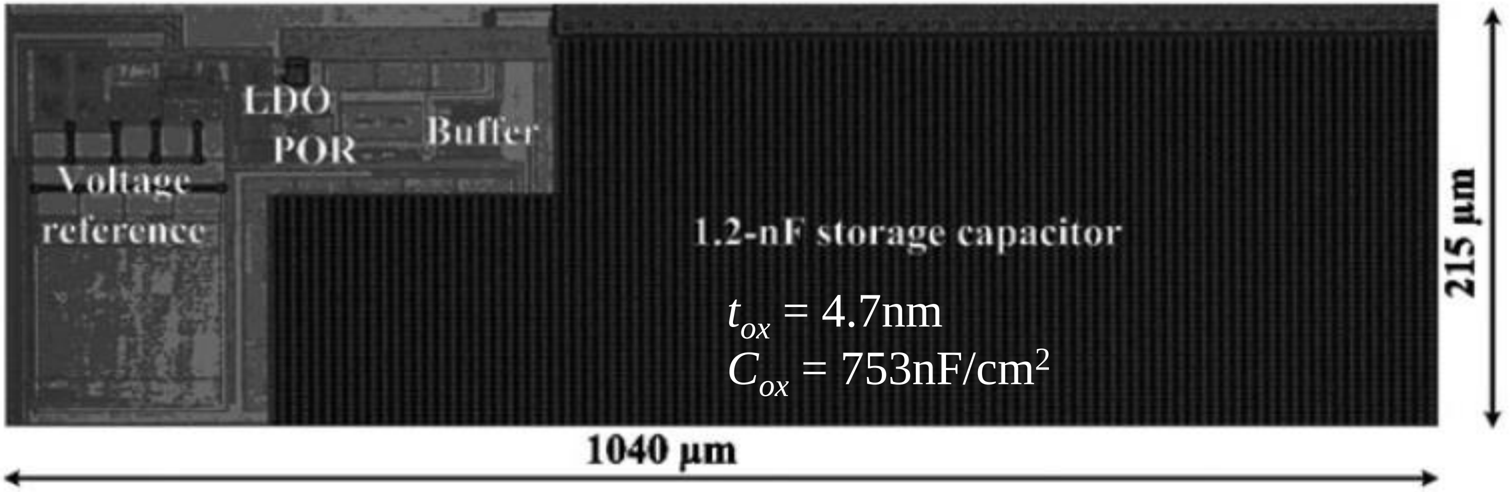
# Regulator Temperature Response





- After laser trimming, almost zero temperature coefficients for both $V_{REF}$ and $V_{DD}$.

# Regulator Decoupling Capacitor



$t_{ox}$ = 4.7nm
$C_{ox}$ = 753nF/cm$^2$

- EPC requires T = 12.5µs of operation after RF power is cut
- Excessive $C_{on\text{-}chip} = I_{load}T/\Delta V_{DD}$ sometime is required.
  - $I_{load}$ = 3µA; $V_{DD}$ = 1.45V; $\Delta V_{DD}$ = 20%
  - $C_{on\text{-}chip}$ = 1.2 nF, which needs 400µm × 400µm area of $C_{ox}$
  - Special trench or backend capacitors in the DRAM process will help significantly

# Outline

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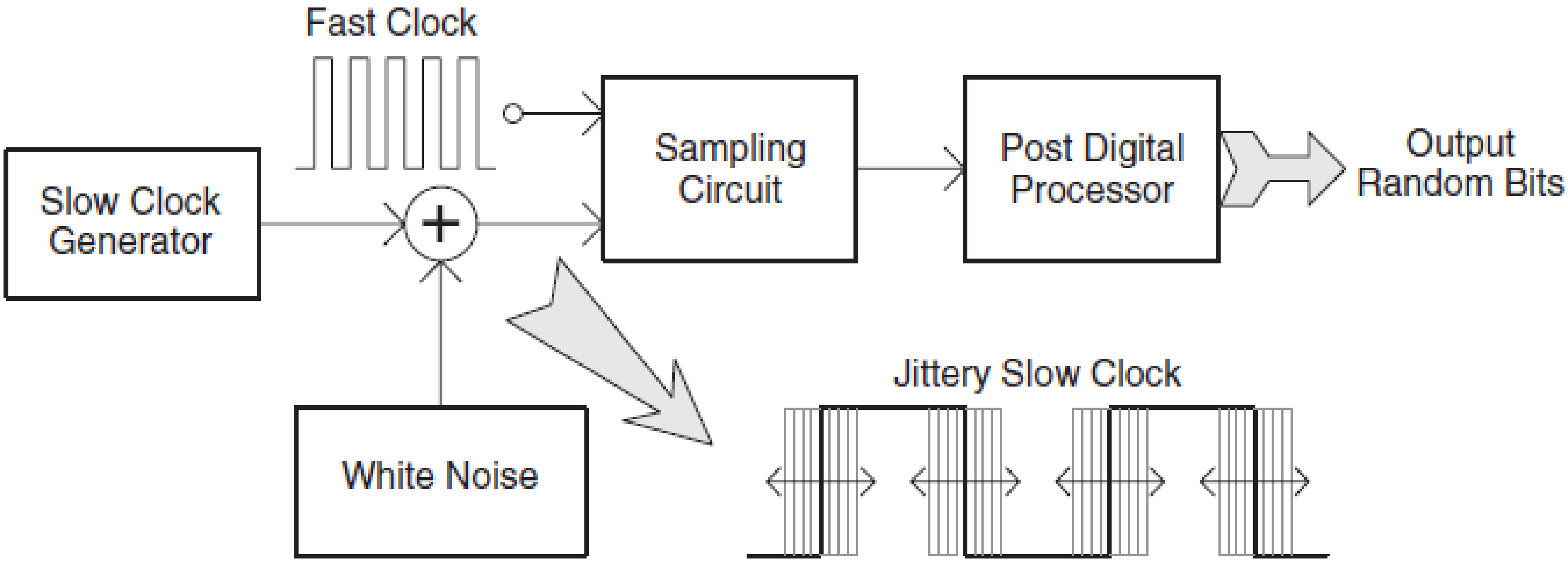
# Random Number Generators

- Pseudo random number generator (PRNG): Use digital state machines with large cycles of repetition
- True random number generator (TRNG): Use unpredictable noise/physical quantities directly or as seed for PRNG (to increase output bandwidth)
- Random numbers are needed in:
  - Seed for security algorithms: TRNG needed
  - Ordering for resolving tag collision: PRNG sufficient
- Diehard and NIST tests of randomness
  - Unpredictable sequence
  - Uniform distribution for a large collection
  - Output bit rate (or called output data bandwidth)

# True Random Number Generator

- Direct amplification of noise using a broadband high-gain amplifier
  - Simple circuit topology, but the amplifier consumes much power; noise may be “colored” which fails uniform distribution
- High frequency oscillator to sample a low-frequency oscillator with larger jitter noises
  - Isolation from other parts; jitter can be colored
- Discrete time chaos systems using analog signal processing
  - Complicated circuit topology and large power consumption
- Release of meta-stable operating points.
  - Often SRAM is used with an equilization transistor

# Oscillator-Based TRNG



- Reasonable tradeoffs between chip area and power consumption; Very good output bit rates
- Can avoid colored noise by raising the frequency of the slow clock
- Insensitive to process variations

# Oscillator-Based TRNG

| Approach | Power Consumption | Bit rate (kb/s) | Chip Size ($mm^2$) | Random nature |
|---|---|---|---|---|
| Oscillator 3-bit random + 16 deterministic | **0.528 μW** | **320** | **0.0056** | Low |
| Oscillator 16-bit random | **1.04 μW** | 40 | 0.05 | **Medium** |
| Oscillator 16-bit random | 2.3 mW | **10,000** | **0.0016** | **High** |
| Latch-metastability Scalable Software-enhanced if power available | 180 μW | 50 | 1.49 | **High** |
|  | **2.92 μW** | 0.5 | 0.031 | **High** |

- The RNG bit rate needs to give at least ≅ N bits ($2^{N-1}$ is the maximum tags allowed within the read range) within several clock cycles of 640 kHz – 1.92 MHz.
- Active tags can pre-compute a set of RN and store them.

# Group Exercise: Why Random?

- Practice counting 1, 2, 3, 4, etc.
- Write down a series of "random number" between 0 and 9 (at least 8 of them).
- After you count to the random number you have, say your name.
- If you are the ONLY person who talks and can be heard clearly, stop saying your name. If more than one persons say their names and interfered each other, after counting to 10, wait for my signal "Say your name", and use your next random number.

- What happened if your number is not truly random (say, you always do $n_i = (n_i + 2) \bmod 10$
- What happened if I tell you to choose a number between 0 and 99?

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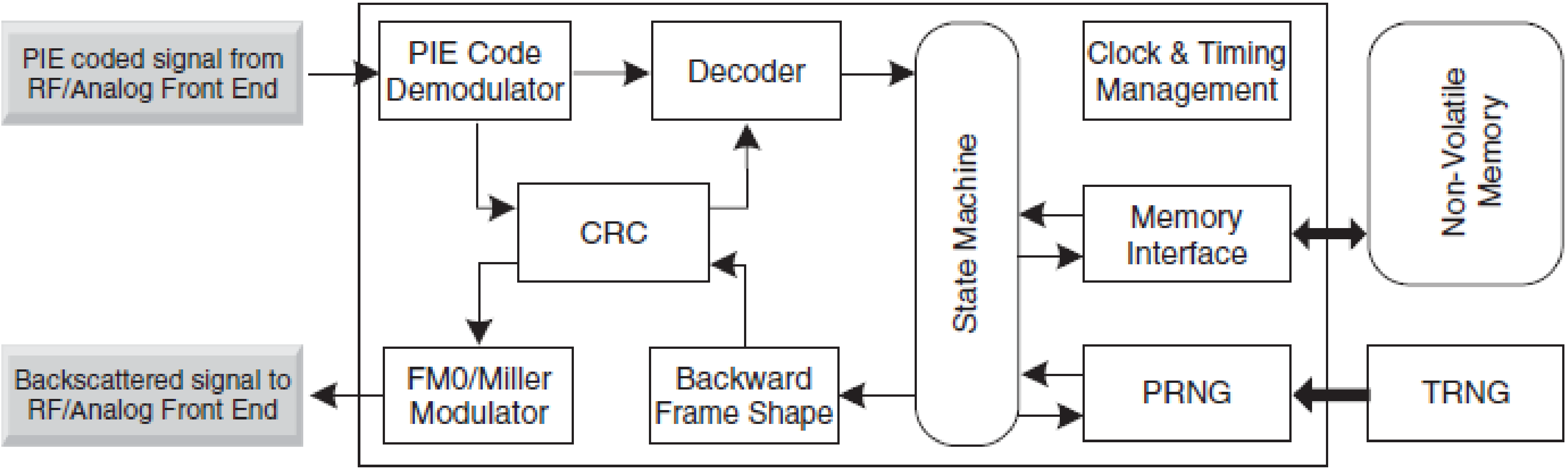
# Digital Baseband Circuits

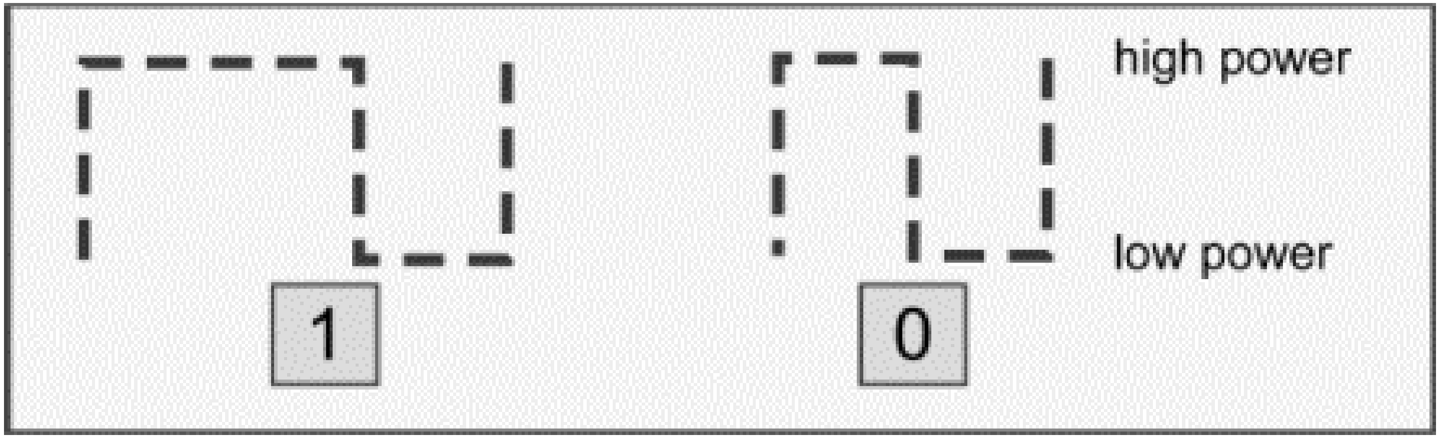


- Need to minimize
  - Dynamic switching power: $CV_{DD}{}^2f$, by reducing $C$, $V_{DD}$ and $f$
  - Signal glitches: by using dynamic logic and clock gating
  - The short-circuit current $I_{SC}$, by reducing rise time, or using dynamic or adiabatic switching with non-overlapping clocks
  - Static leakage: Reasonably high $V_{th}$ and subthreshold slope $S$.

# Baseband Clock Rate

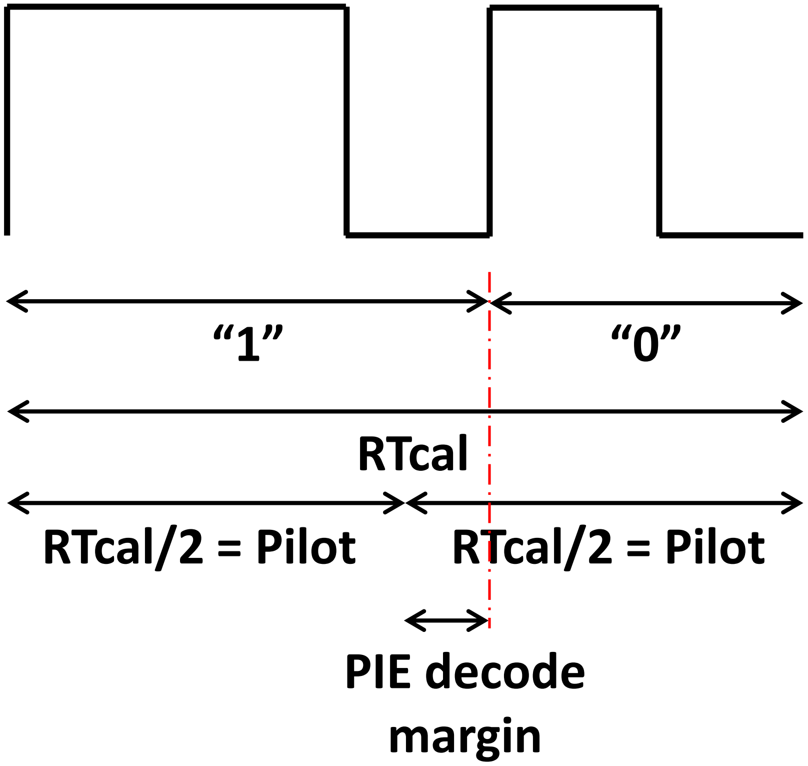
The baseband clock rate is set by:

- Time resolution during non-coherent (no phase info) demodulation of Pulse interval encoding (PIE) codes
  - Ambiguity between “0” and “1”,
  - backscatter link frequency (BLF): 640kHz for EPC Gen 2
- Power requirements: clock generation oscillator and dynamic switching power



# PIE Decode Margin

- RTcal: reader to tag communication unit: the sum of “1” and “0” duration = $T_{"0"} + T_{"1"}$
- Pilot = RTcal/2
- Decode margin = worse case of ($T_{"1"}$ – Pilot) or (Pilot – $T_{"0"}$)



# Decode Margin and Baseband Clock Jitter

- The baseband clock is a multiple rate of backscatter link frequency (BLF), and it needs to sample the PIE code after demodulation.
- Sampling or quantization error (caused by clock jitters) will need to be larger than the decode margin, or else the code will have an error/ambiguity.
- Quantization error and jitter noise is proportional to the baseband clock period.
- This sets a lower bound of the baseband clock.

# BLF and Divide Ratio

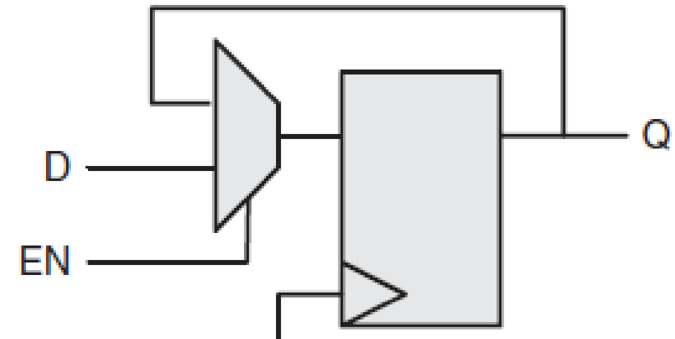
- EPC C1G2 specifies a number DR (divide ratio) to set the BLF and the data rate of TRcal (tag to reader communication unit)

$$BLF = \frac{DR}{TRcal}$$

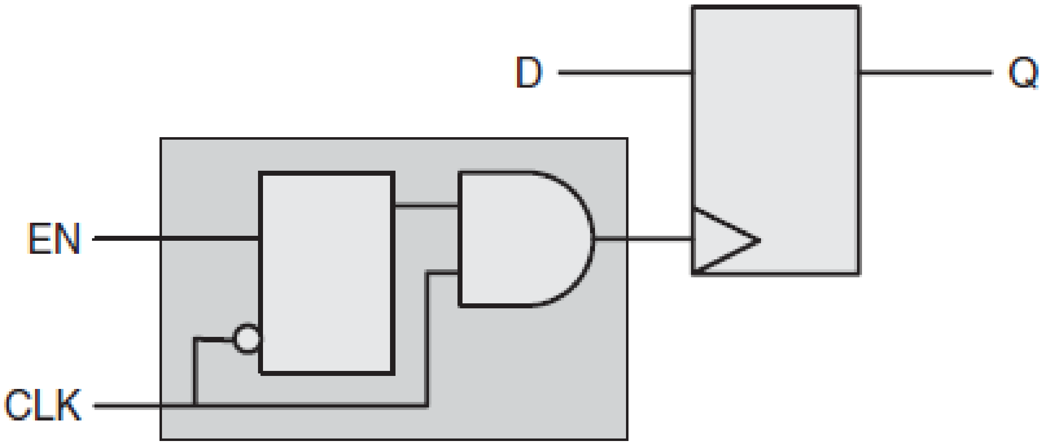
$$TRcal_{measure} = nT_{clk} = TRcal + error$$

- If $f_{clk} = 1/T_{clk}$ is not high enough, the quantization error may be too large to be acceptable.

# Clock Gating in Baseband Logic



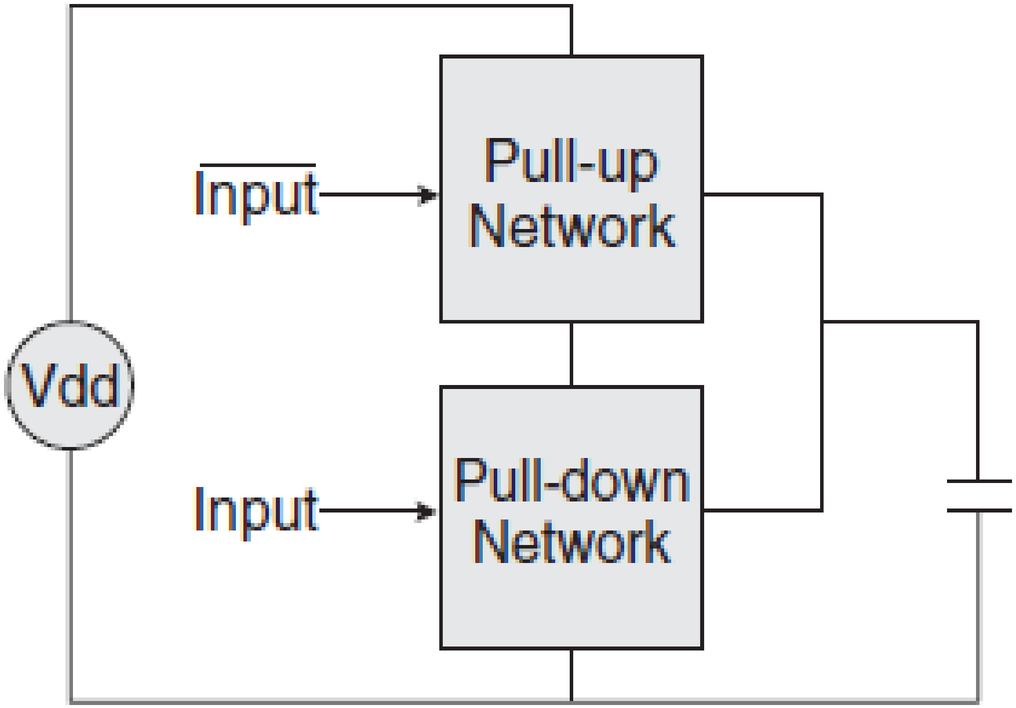
DFF with MUX



DFF with clock gating

- Minimizing the switching in the registers by applying logic to the clock signal
- No race condition for DFF

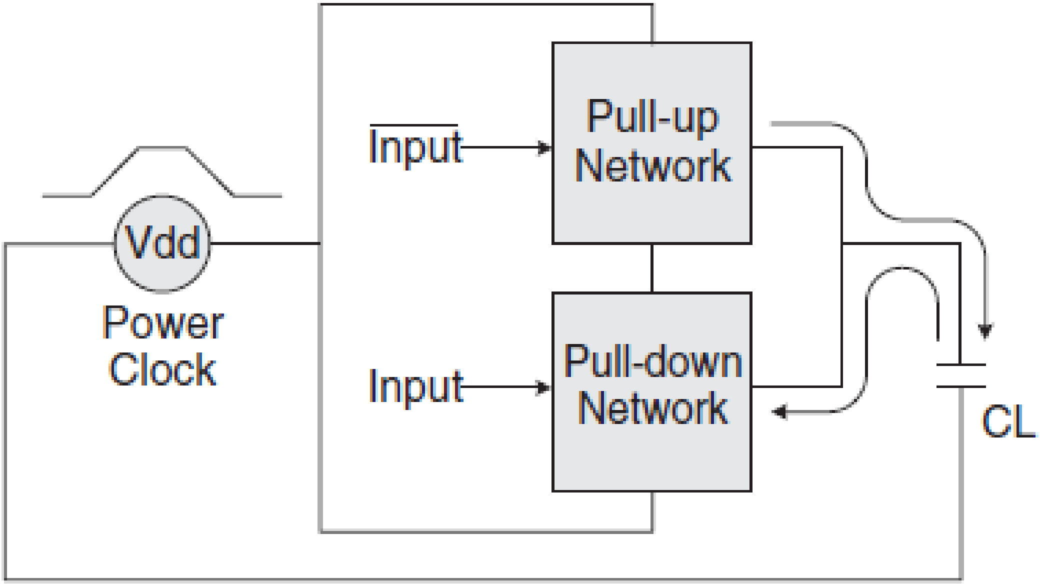
# Short-Circuit Current and Glitches



Standard CMOS Logic

- If PUN and PDN are never simultaneously ON, no short-circuit current.
- If PUN and PDN are ON only once during the clock cycle: no glitch

# Adiabatic Logic in Baseband



Adiabatic CMOS Logic

- $V_{GS}$ can only turn device ON when $V_{DS}$ = 0
- $V_{DS}$ can be changed only when $V_{GS}$ turn the device OFF.
- Any voltage can only change slowly

$$E_{total} = E_{switching} + E_{data} = 2\frac{RC}{T}CV^2 + \frac{1}{2}CV^2$$

# Outline

- Tag architecture
- Analog, RF and digital circuit components
- RF-to-DC converter and voltage regulator
- Random number generator
- Baseband circuits and considerations
- Frequency strategy in mod/demod

# Carrier and Baseband Frequency Strategy

- To shift frequency from one band to the other, we will need either a **nonlinear** or **time-variant** system, as linear time-invariant (LTI) can have superposition in the frequency domain.

LTI:

$$y(t)=\int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau = x(t)*h(t)$$

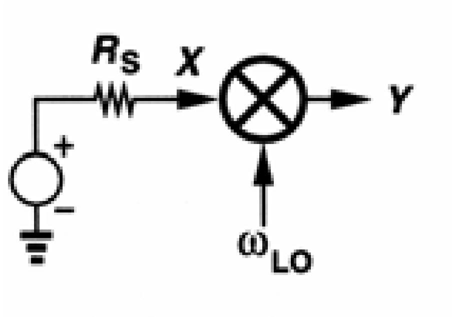
$$Y(\omega)=X(\omega)H(\omega)$$

- To shift frequency to high-frequency carrier (up conversion):
  - High frequency has smaller antennas
  - More effective use of bands and bandwidth
  - Different channels can share a narrow-band power amplifier
- To shift frequency to low-frequency baseband (down conversion):
  - Easier manipulation (filtering, A/D, etc.) of a fixed bandwidth (which is proportional is data rate)
  - Lower power consumption

# CMOS Mixers and Switch Loading

## Mixer by multiplication (Superheterodyne)

$V_{RF}(\omega_{RF})$
or $V_{base}(\omega_{Base})$

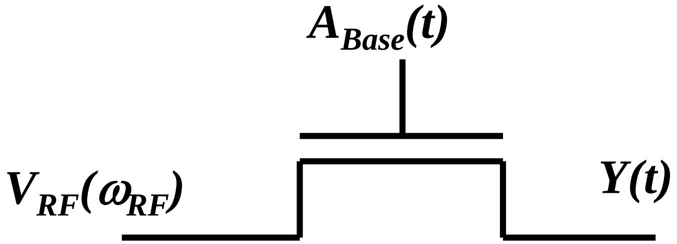


$$\left(A_{RF}\cos(\omega_{RF}t)\right)\left(A_{LO}\cos(\omega_{LO}t)\right)=$$

$$\frac{A_{RF}A_{LO}}{2}\left[\cos(\omega_{RF}-\omega_{LO})t+\cos(\omega_{RF}+\omega_{LO})t\right]$$

Share the same multiplier for modulator and demodulator

## Switch loading by direct envelope functions



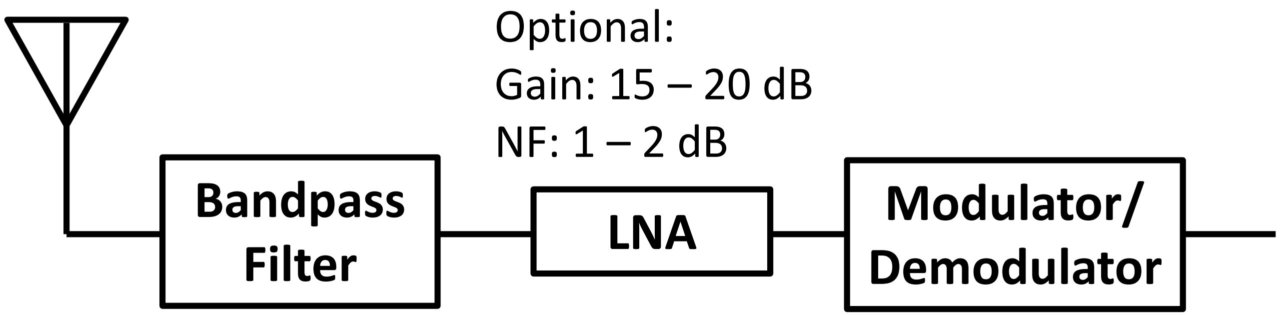
$$A_{Base}(t)\cdot A_{RF}\cos(\omega_{RF}t)$$

Pass transistors for modulation and envelope detector for demodulation

# UHF Tag Mixer Requirements

- Low power consumption
- Acceptable linearity (1dB compression point, $IIP_3$, ...)
- Acceptable noise (noise figure)
- Acceptable gain (voltage gain; input/output impedance for power gain)
- Good isolation between ports

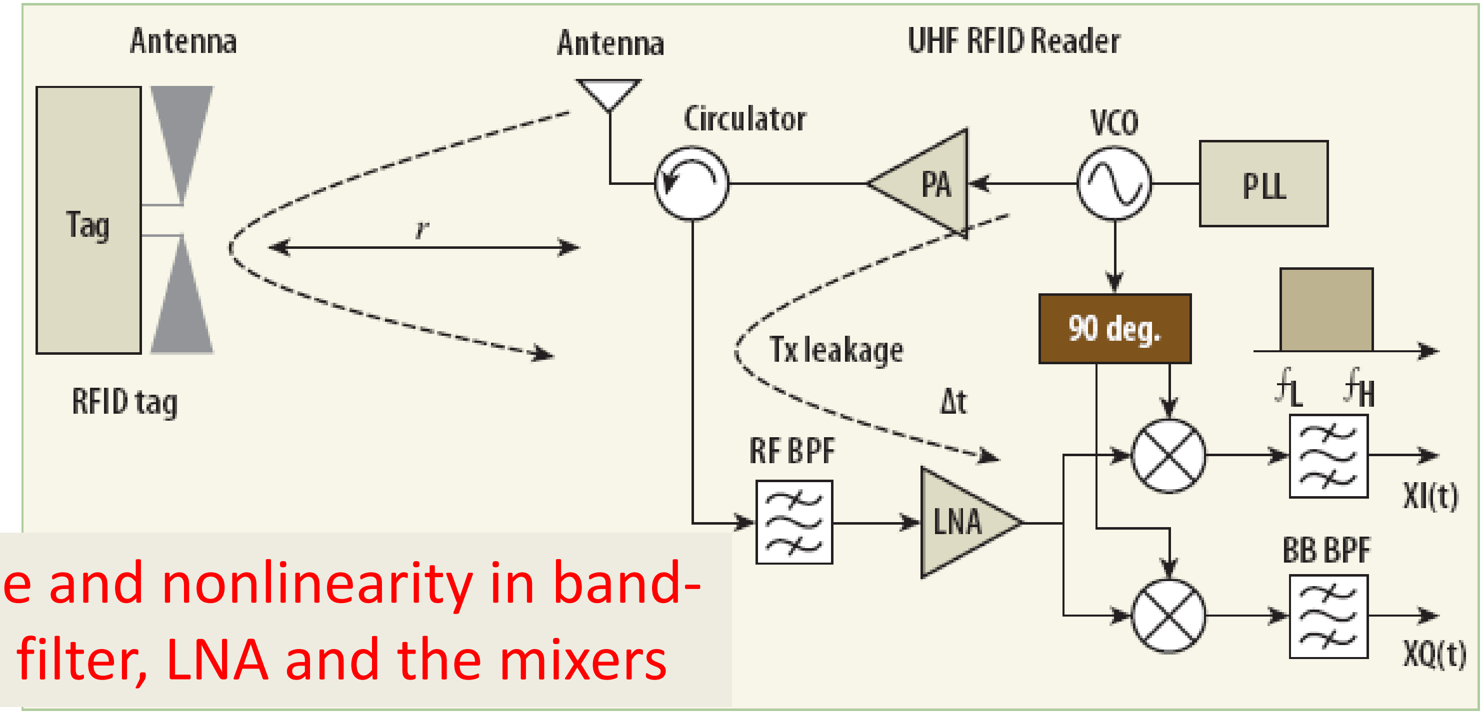
Note: mixer noise will be attenuated by LNA gain, but the nonlinearity will be amplified by the LNA gain.



Optional:
Gain: 15 – 20 dB
NF: 1 – 2 dB

# Fundamental Limits of Receivers

- Dynamic range (dB): The range of signal power when a receiver can decode the intended signal correctly.
- The lowest signal power that can be decoded is limited by **NOISE** (SNR).
- The highest signal power that can be decoded is limited by receiver **NONLINEARITY** (jamming)



Noise and nonlinearity in band-pass filter, LNA and the mixers

# Nonlinearity and Jamming

- A dynamic range of 100dB of a receiver means: if the sensitivity is –90 dBm (1pW, 7μV), then when the input power is higher than 10dBm (10mW, 0.7V), it would cause jamming.
- Signal itself can be distorted after amplifier
- Signal can be buried with a strong in-band jamming

- BUT, the dynamic range required for the tag receiver is relatively **SMALL**!!! (Highest impinging signal from reader: 36 dBm; Lowest impinging signal to understand: –20 dBm. DR = –56dB)

**Notice DR in dB, not dBm!!!**

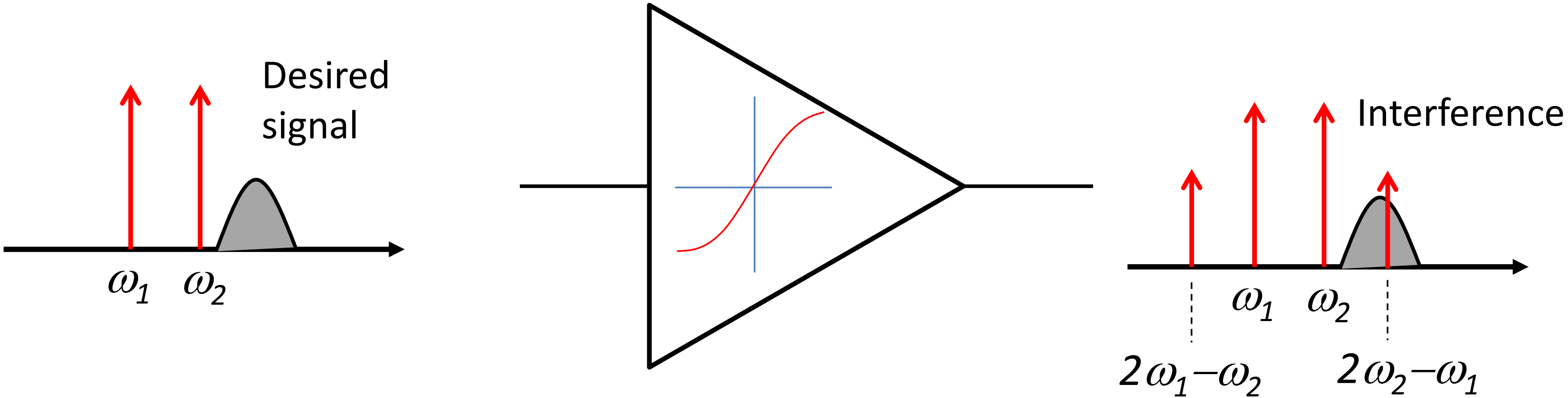
# Weakly Nonlinear Receivers

- Practical amplifiers ALWAYS have nonlinearity when the input signal is sufficiently large.
- In a transfer function point of view:

$$P_{out} = \alpha_1 P_{in} + \alpha_2 P_{in}^2 + \alpha_3 P_{in}^3 + \ldots$$

- Harmonics from single-tone input
- Intermodulation products from two-tone input ($f_1$ and $f_2$ are fairly close): $A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)$
- Rule-of-thumb use for “$\mathrm{IIP}_3$” (input interception point 3)
  - IIP3 = 10 dBm; at Pin = -5dBm, the nonlinear product will be: $(3 - 1)\times(10 - (-5)) = 30$ dB below test signal

# Third-Order Nonlinearity Effect



Nonlinear amplifier:

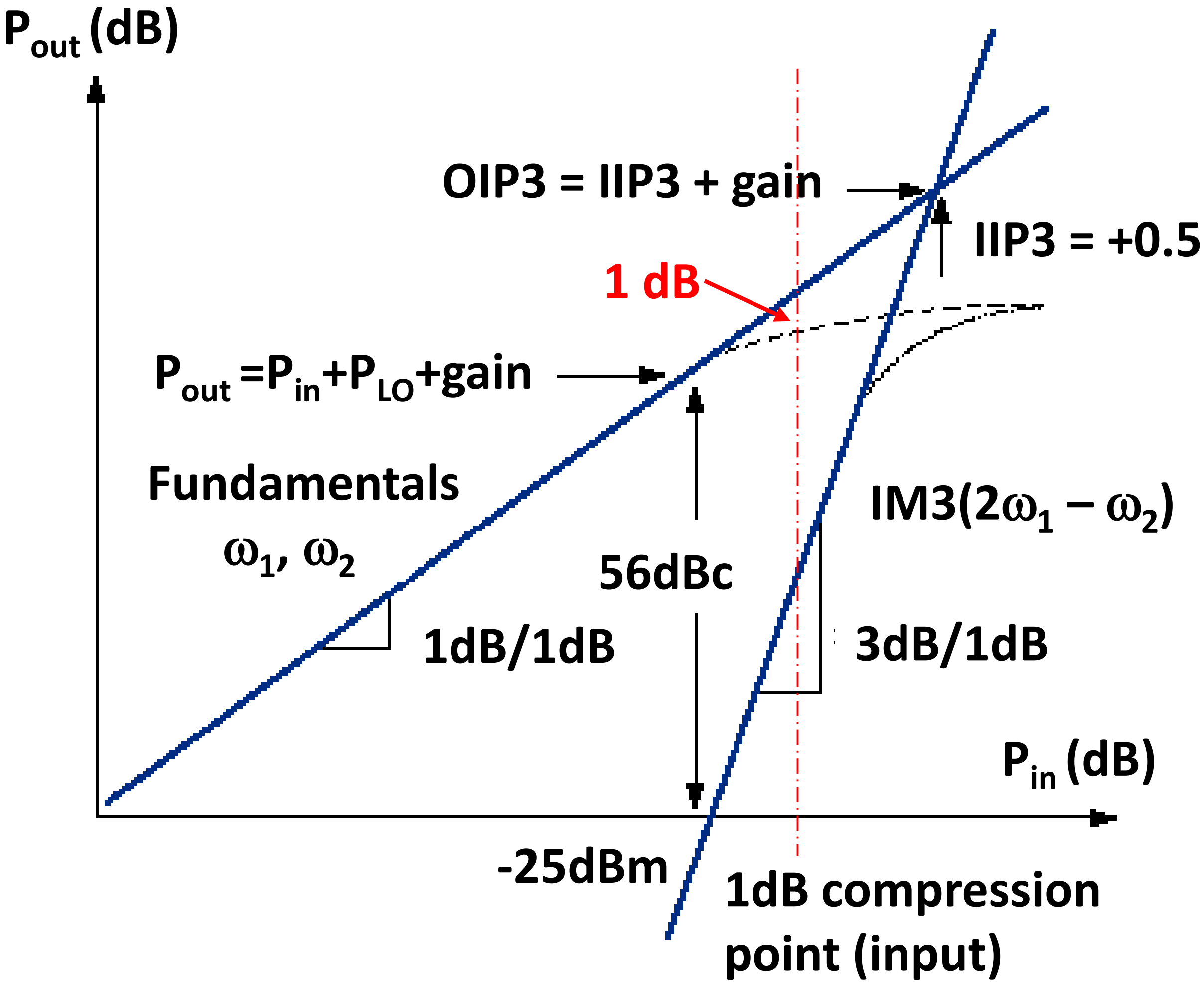
$$V_{out} = GV_{in} - D_3 V_{in}^3 + \ldots$$

$$\cos^3(x) = \frac{3}{4}\cos(x) + \frac{1}{4}\cos(3x)$$

“1dB compression point” is about **10dB** lower than IIP$_3$

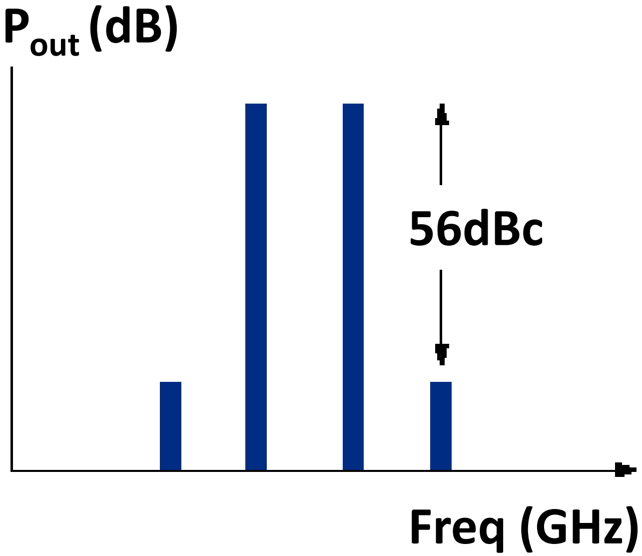
Proof: http://en.wikipedia.org/wiki/Third-order_intercept_point

# Mixer Linearity for Intermodulation



IIP3: Input third-order intermodulation point

OIP3: Output third-order intermodulation point

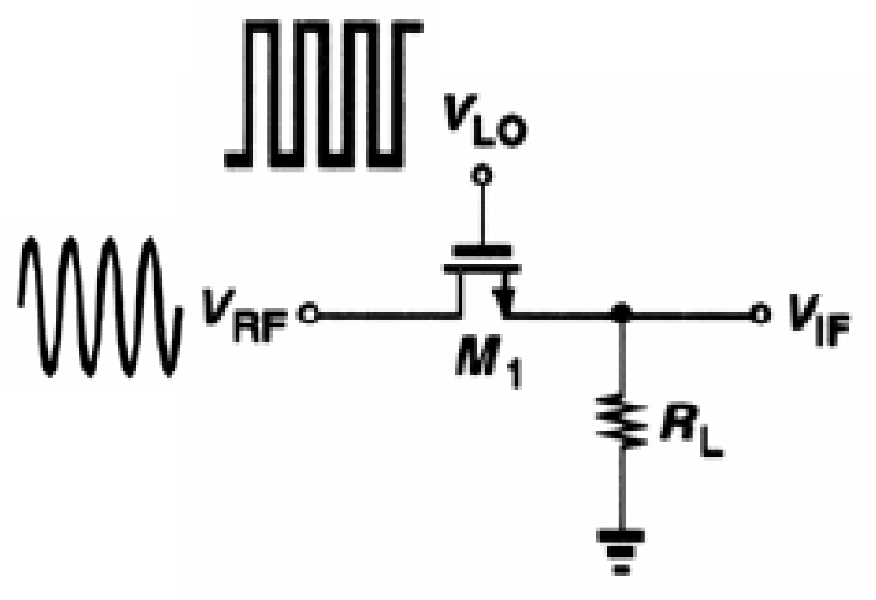


Maxim SiGe BJT Mixer

# Group Exercise: Dynamic Range?

- Give real-world, non-electronic examples on system behavior when sensitivity and range are fundamental trade-offs. Give also the fundamental constraint (finite resources).

# Passive Mixer Based on Linear Time Varying (LTV) System with Direct Multiplication



Assume

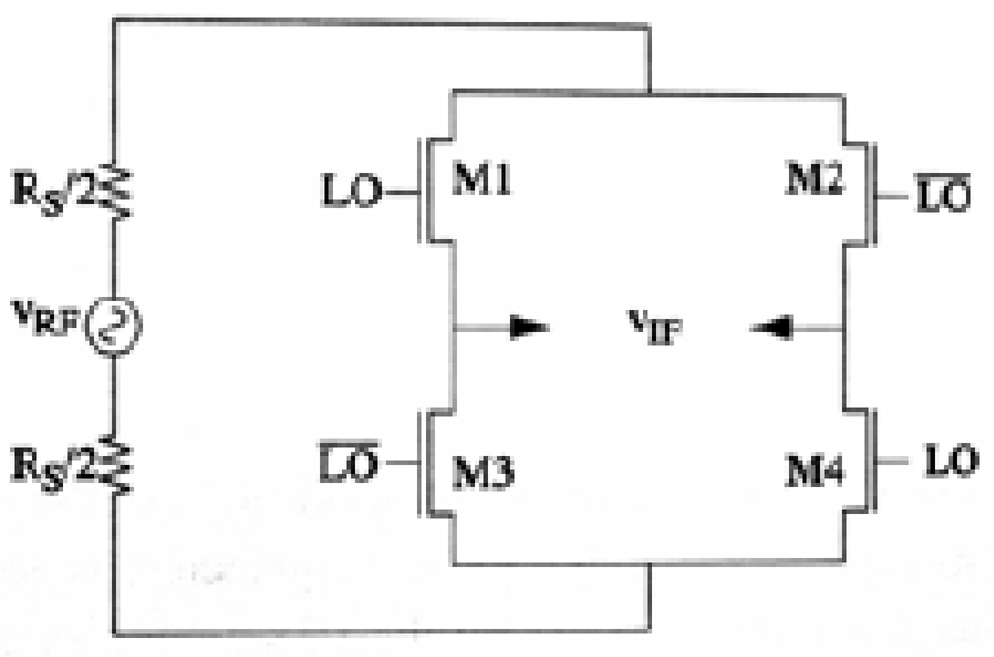
- 50% duty cycle of $v_{LO}$
- $R_L >> R_{M1(Ohmic)}$

$$\omega_{IF} = \omega_{RF} \pm \omega_{LO}$$

$$G_C \cong \frac{1}{\pi}$$

- $v_{LO}$ switches $M_1$ ON and OFF ($M_1$ works between OFF and deep Ohmic region, i.e., $v_{DS} \cong 0$ and $v_{IF} \cong v_{RF}$ when $v_{LO}$ = high)
- No power consumption and high linearity (with $V_{th} \cong 0$)
- No bias current: No Flicker noise (good for direct conversion)
- Poor channel isolation by $C_{gd}$ and $C_{ds}$

# Passive Double-Balanced Mixer



Assume

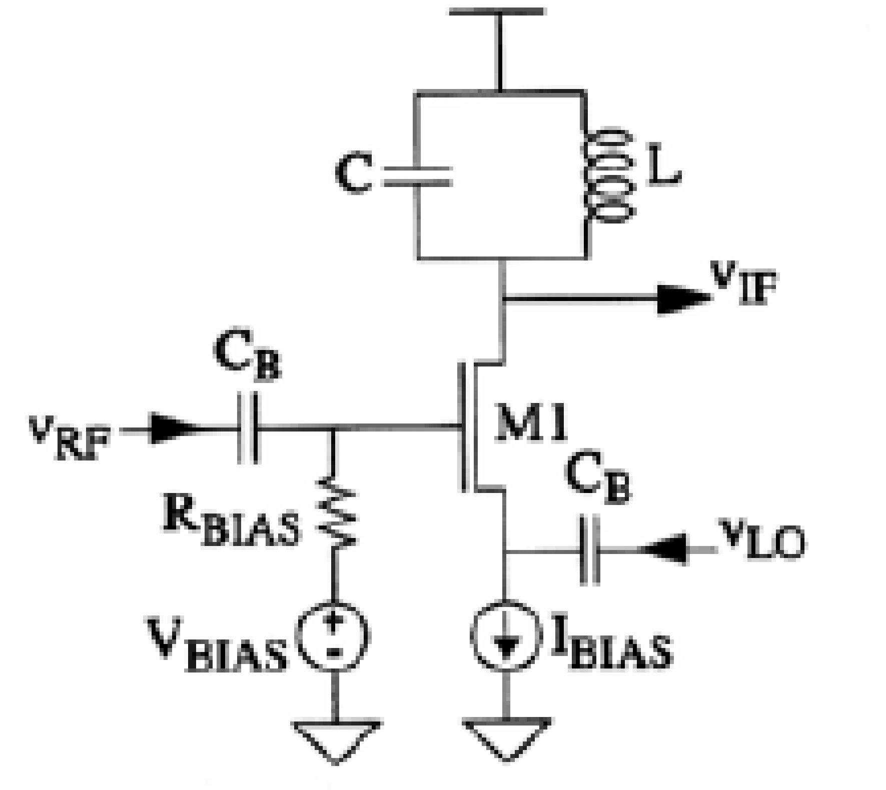
- $R_L >> R_{M(Ohmic)}$

$$\omega_{IF} = \omega_{RF} \pm \omega_{LO}$$

$$G_C \cong \frac{2}{\pi}$$

- Differential setup (3dB higher gain)
- Better RF and IF isolation

# Active Mixer Based on Nonlinearity



$$i_D = \frac{k'}{2}\left(\frac{W}{L}\right)\left(v_{GS} - V_{th}\right)^2$$

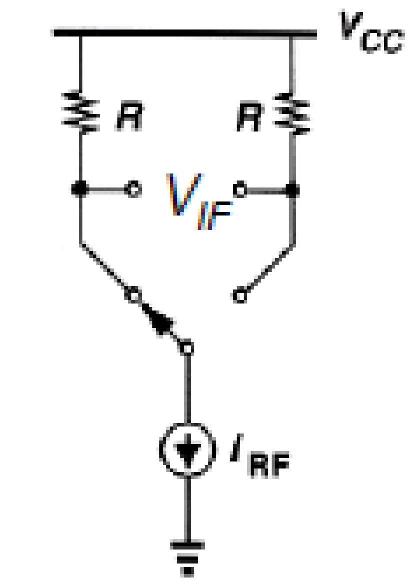
$$v_{RF}(t) = V_{RF}\cos(\omega_{RF} t)$$

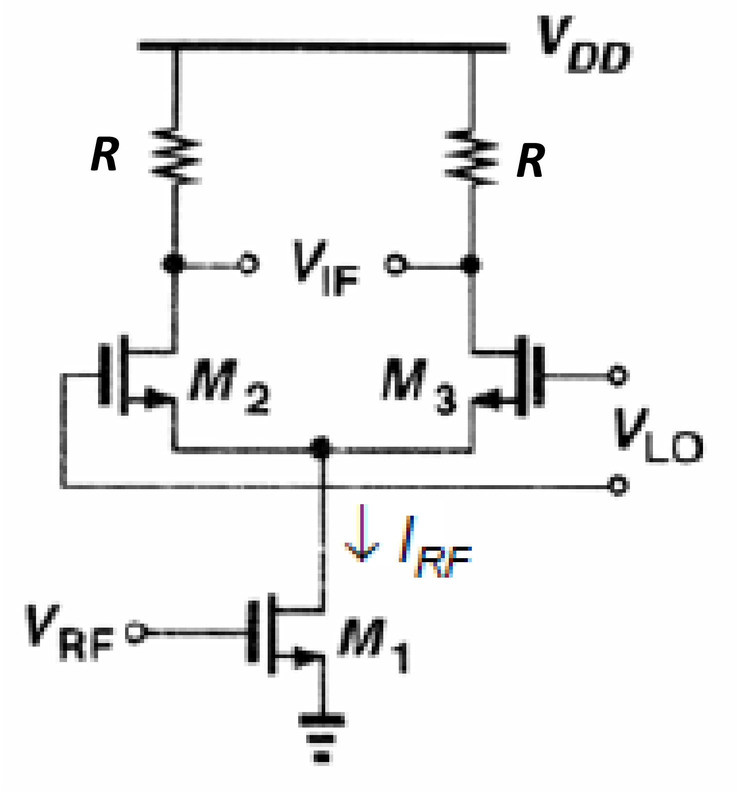
$$v_{LO}(t) = V_{LO}\cos(\omega_{LO} t)$$

$$v_{GS} = \left(v_{RF} - v_{LO}\right)$$

- Very large coupling capacitors for correct blocking
- $v_{RF}$ and $v_{LO}$ can see very different impedance

# Active Mixer Based on Multipliers



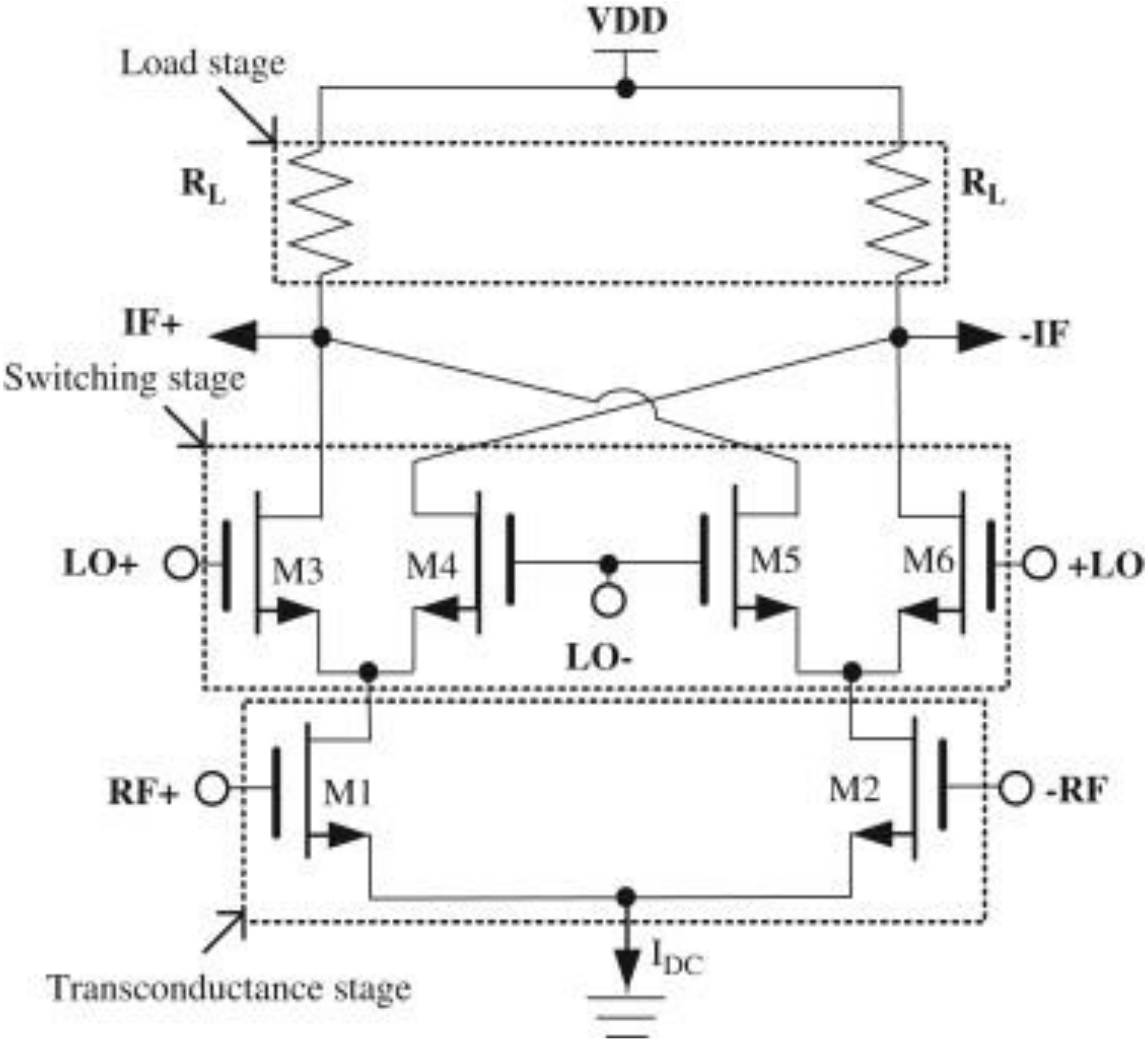


$$\omega_{IF} = \omega_{RF} \pm \omega_{LO}$$

$$G_C \cong \frac{2}{\pi} g_m R$$

- Common-source differential amplifier ($M_{1\text{-}3}$ in saturation)
- Differential output has theoretical infinite RF to IF isolation
- Body-effect distortion

# Active Mixer Based on Gilbert Multipliers



- Double Balanced
- Fully Differential
- Most popular mixer for the active RF transmitter and reader
- Power consumption prohibitive for most passive RFID tags.

# What Do You Learn

- The overall tag architecture
- Analog, RF and digital circuit functions on tags
- Dickson’s RF-to-DC converter
- Compensation in voltage regulator
- Baseband digital circuit implementations
- Passive and active mixers

- Low power, ultra low power in tag circuits!!!