Department of Electrical and Computer Engineering, Cornell University

ECE 3150: Microelectronics

Spring 2016

Lab 3 **Due one week after your lab day in the course "Lab Dropbox"**

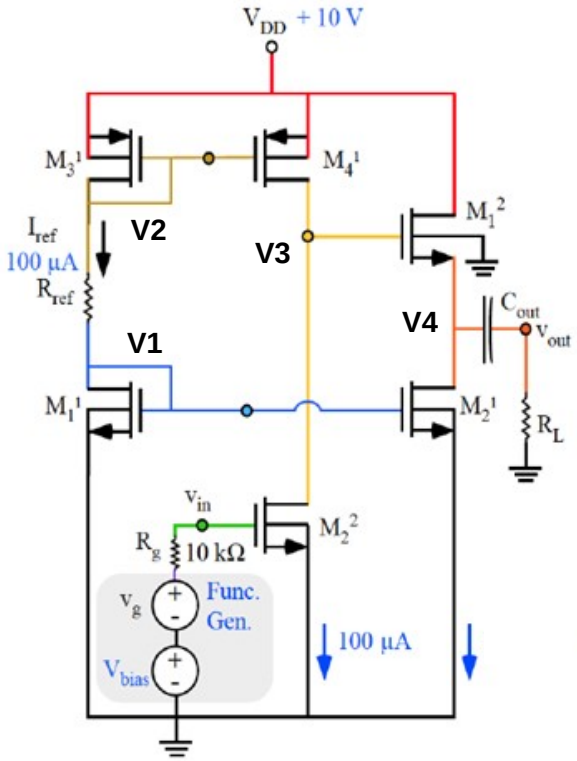
Lab Goals

1) Examine the properties of a common source/common drain cascaded FET amplifier.
2) Characterize the output resistance of current mirrors.
3) Test a cascode amplifier with a cascode current mirror load.
4) Learn measurement techniques to determine the amplifier performance metrics like voltage gain and input/output resistances.

Pre-Lab Work

4.1 A FET Common Source and Common Drain Cascade Amplifier

Consider the following FET amplifier along with its biasing circuit:



Assume (see appendix for PFET and NFET measured data):

$V_{TN} = 0.65\,V$

$V_{TP} = -0.70\,V$ $\qquad \lambda_n = .018\,1/V$

$k_n = 0.622\,mA/V^2$ $\qquad \lambda_p = .026\,1/V$

$k_p = 0.270\,mA/V^2$

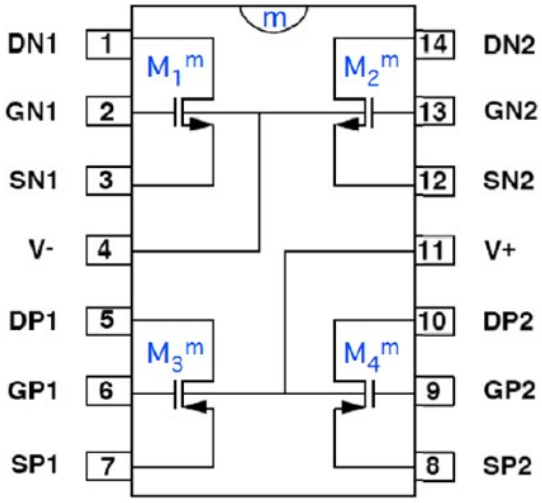
a) What ought to be the value of the resistor R_{ref} such that I_{ref} is ~100 μA?

b) Using your results from part (a), find the DC bias voltages V_1, V_3, V_3. In finding V_3 assume that the current in the middle leg of the circuit is also ~100 μA (provided V_{bias} is appropriately adjusted). Now estimate V_4. Note that the current in the last leg will also be close to 100 μA.

c) Find an expression for and then calculate the small signal open circuit voltage gain of the amplifier (i.e. assuming $R_L = \infty$).

Lab Preparation

1) Carefully review this document. You need to know all that you will be doing in the lab and all the data that you will need later (after the lab) for the post-lab work.
2) You can use a USB memory stick to get data out of the lab computer (recommended). Or you might also be able to email the data files to yourself (not recommended).
3) Be sure to understand the analysis of the circuit(s) to be built (pre-lab work).
4) Look over the data sheet of the chip ADL1105, shown below. You will need two of these.
4) Do the pre-lab before coming to the lab.

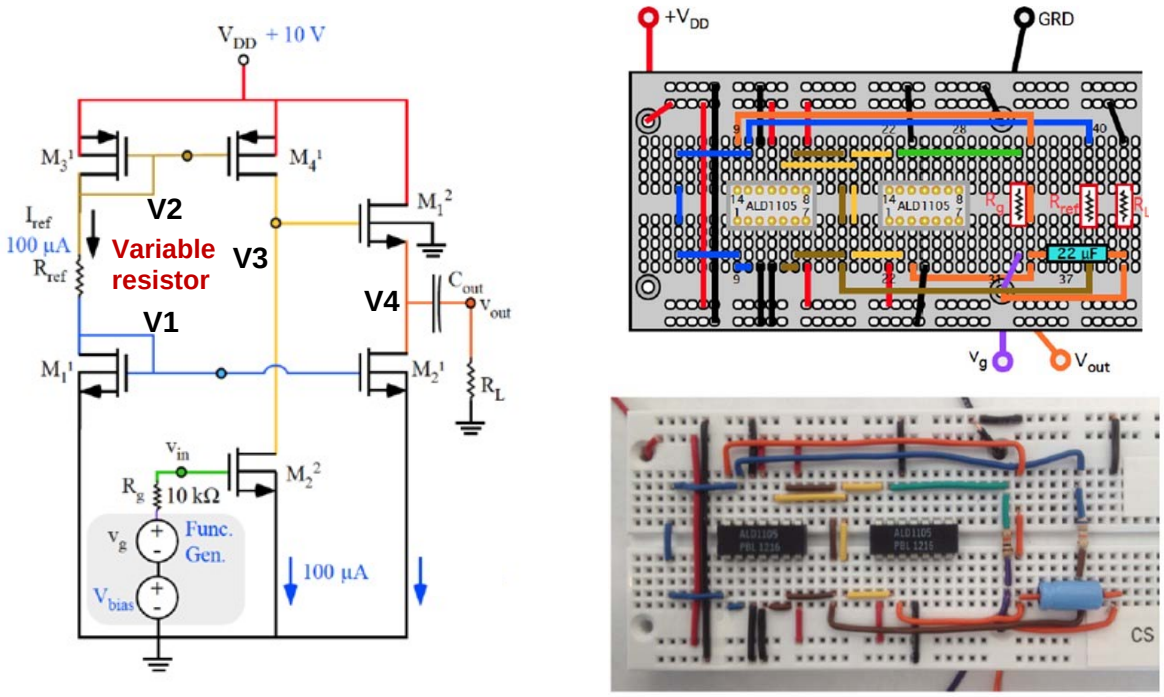


Lab Work

4.2 Common Source and Common Drain Cascade Amplifier

a) Build a common source/common drain amplifier circuit whose schematic diagram appears below along with a photograph of a circuit build on the board (to help you with the layout). In addition to the FETs

used for amplification, this circuit requires 2 PFETs for the bias current source on the common source input stage, and two NFETs to form the bias current source on the common drain stage. Two ALD1105 chips are therefore required. Note that the output is AC coupled through a 22 μF capacitor. In the diagram below, the transistor are labelled as M_n^m where m is the ALD1105 package (chip) number (left = 1, right = 2) and n is the transistor number in the package. Matched FETs must belong to the same package (chip). The resistor R_{ref} is selected to adjust the DC current flowing through the bias circuit (left hand branch) which is mirrored on the common source stage and the common drain stage. Given actual the characteristics of NFETs and PFETs we are using R_{ref} should be around ~72 kΩ to get a current I_{ref} of around ~100 μA and V_{bias} needs to be around ~1.25 V. Values can vary from chip to chip. **Use a variable resistor as R_{ref}.** <u>One you have connected the circuit make sure the DC current passing through the resistor R_{ref} is ~100 μA.</u> The DC output voltage will be VERY sensitive to the exact value of V_{bias}. <u>To understand (or rather remind yourself of) the origin of this sensitivity refer to pages 5 and 6 of lecture handout 15.</u>



b) Select a 1 kHz sine wave on the function generator. Set the DC voltage offset on the function generator to the chosen value for V_{bias}. Set the function generator to a 5 mV peak-to-peak AC amplitude (really small). Remember to Recall ECE2100Setup and enable external trigger on the scope. Both scope channels should be AC coupled. Connect everything (except the load resistor).

c) Measure the DC voltage of each node (V_1,V_3,V_3,V_4) of each stage with the DMM and record it. Make sure they are close to what you expect and <u>that no FET is outside the saturation region of operation</u>. Average and measure input and output AC voltage amplitudes (peak-to-peak) and record them.

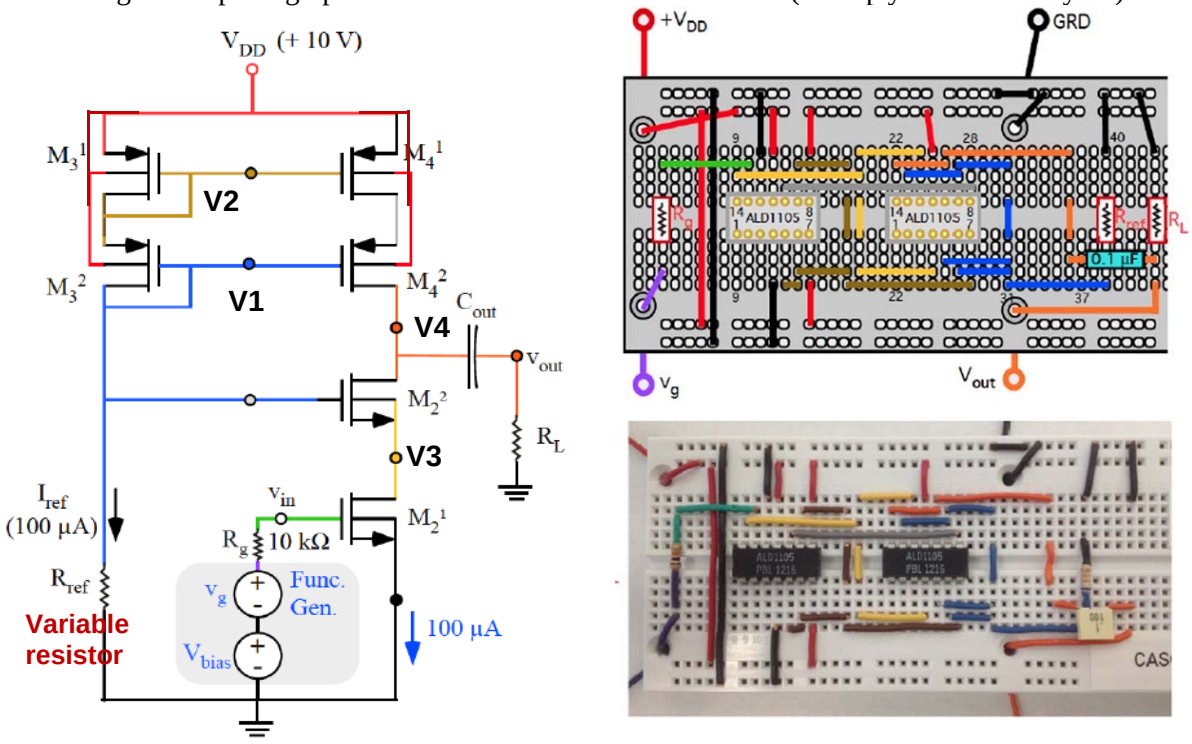
d) The circuit would be a bit sensitive to the exact value of the DC bias voltage V_{bias}. Adjust the function generator's offset voltage (V_{bias}) in a few mV or a few tens of mV increments/decrements and repeat input and output AC voltage measurements. Optimize the DC offset (V_{bias}) voltage for the best voltage gain (largest output signal). Make sure no clipping is happening. If you see clipping, this could indicate some FET operating out of the saturation region. Record the best value of the voltage gain and the corresponding values of V_{bias} and all other DC node voltages V_1,V_3,V_3,V_4 . <u>Make sure no FET is outside</u>

the saturation region of operation. Once you have figured out the optimum V_{bias} this way, proceed to the next part. If you see some FET operating outside the saturation region adjust V_{bias} to correct.

e) Up until now the circuit is unloaded ($R_L = \infty$). Using your optimized value of V_{bias}, connect ~10 different load resistors R_L, with values ranging from 100 Ω to 100 kΩ, and for each load resistor value, measure the voltage gain. You will be predicting these loaded voltage gains in the analysis. And you will plotting the voltage gain vs. the log of load resistance so spread your resistor values out evenly (on a log scale).

4.3 Cascode Amplifier with a Cascode Current Source

a) Build a cascode amplifier circuit with a cascode current bias source whose schematic diagram appears below along with a photograph of the of a circuit build on the board (to help you with the layout).



Note that the output is AC coupled through a 0.1 μF capacitor. Verify that R_{ref} should be around ~69 kΩ in order to get I_{ref} around ~100 μA. Actual values of R_{ref} can vary from chip to chip. **Use a variable resistor as R_{ref}.** After you have connected the circuit verify that I_{ref} is indeed ~100 μA. Select V_{bias} to be close to ~1.25 V.

b) Select a 1 kHz sine wave on the function generator. Set the DC voltage offset on the function generator to the chosen value for V_{bias}. Set the function generator to a 5 mV peak-to-peak AC amplitude (really small). Remember to Recall ECE2100Setup and enable external trigger on the scope. Both scope channels should be AC coupled. Connect everything (except the load resistor).

c) Measure the DC voltage of each node (V_1, V_3, V_3, V_4) of each stage with the DMM and record it. Make sure they are close to what you expect and that no FET is outside the saturation region of operation. Average and measure input and output AC voltage amplitudes (peak-to-peak) and record them.

d) The circuit would be a bit sensitive to the exact value of the DC bias voltage V_{bias}. Adjust the function generator's offset voltage (V_{bias}) in a few mV or a few tens of mV increments/decrements and repeat input and output AC voltage measurements. Optimize the DC offset (V_{bias}) voltage for the best voltage gain (largest output signal). Make sure no clipping is happening. Record the best value of the voltage gain and the corresponding values of V_{bias} and all other DC node voltages V_1, V_3, V_3, V_4 . Make sure no FET is outside the saturation region of operation. Once you have figured out the optimum V_{bias} this way, proceed to the next part. If you see some FET operating outside the saturation region adjust V_{bias} to correct.

e) Up until now the circuit is unloaded ($R_L = \infty$). Using your optimized value of V_{bias}, connect ~10 different load resistors R_L , with values ranging from 10 kΩ to 1 MΩ, and for each load resistor value, measure the voltage gain. You will be predicting these loaded voltage gains in the analysis. And you will plotting the voltage gain vs. the log of load resistance so spread your resistor values out evenly (on a log scale).

f) **Wind down:** Dismantle your circuit(s) and place your bread-board and the devices you tested in the bins that the TAs provided. Transfer all generated files for access outside the lab. Alternatively, if you brought portable media (USB memory stick) then gather up all the files onto your media.

Post-Lab Work

4.4 CS/CD Amplifier

a) Compare the predicted (from 4.1(b)) and measured DC values of V_1, V_3, V_3, V_4 from 4.2(d).

b) Compare the best measured voltage gain from 4.2(d) and the predicted value using 4.1(e).

c) Prepare a plot of voltage gain (in dBs) versus log of load resistance both measured (from 4.2(e)) and predicted. Carefully explain which device parameters influence the loaded voltage gain. Indicate the unloaded gain (when $R_L = \infty$) both predicted and measured on the plot.

4.5 Cascode Amplifier

a) Using the given FET parameters, and the biasing current value I_{ref}, find the DC bias voltages V_1, V_3, V_3, V_4 using theory.

b) Find an expression for and then calculate the small signal open circuit voltage gain of the amplifier (i.e. assuming $R_L = \infty$) using theory.

c) Compare the predicted (from 4.5(a)) and measured DC values of V_1, V_3, V_3, V_4 from 4.3(d).

d) Compare the best measured voltage gain from 4.3(d) and the predicted value using 4.5(b).

e) Prepare a plot of voltage gain (in dBs) versus log of load resistance both measured (from 4.3(e)) and predicted. Carefully explain which device parameters influence the loaded voltage gain. Indicate the unloaded gain (when $R_L = \infty$) both predicted and measured on the plot.