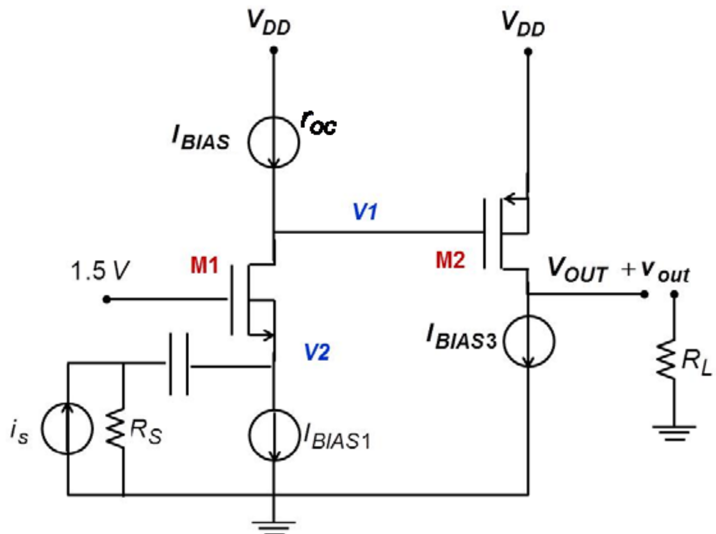
ECE 3150 Homework 9 Solutions

Problem 9.1: (Designing a cascade transresistance amplifier)



a) This is a common gate stage followed by a common source stage.

b) One can ignore λ_n in the calculation of the FET width:

$$\frac{k_n}{2}(V_{GS1}-V_{TN})^2 = \frac{W_1}{2L}\mu_n C_{ox}(1.5-0.5-0.7)^2 = 200\ \mu A$$
$$\Rightarrow W_1 \approx 356\ \mu\text{m}$$

c) One can again ignore λ_p in the calculation of the FET width:

$$\frac{k_p}{2}(V_{GS2}-V_{TP})^2 = \frac{W_2}{2L}\mu_p C_{ox}(3.0-5.0+1.0)^2 = 500\ \mu A$$
$$\Rightarrow W_2 \approx 160\ \mu\text{m}$$

d) R_{in} would just be the input resistance of the NFET common gate stage (from the lecture handouts) that is connected to an infinite R_L but where the resistance R on the drain side is r_{oc}:

$$\Rightarrow R_{in} = \frac{r_{on}+r_{oc}}{g_{mn}r_{on}+1} \approx \frac{1}{g_{mn}}\left(1+\frac{r_{oc}}{r_{on}}\right)$$

e) R_{out} would just be the output resistance of the PFET common source stage (from the lecture handouts) that has an infinite resistance R on the drain side (because of the ideal current source I_{BIAS3}):

$$\Rightarrow R_{out} = r_{op}$$

f) The problem can be solved in two steps; first we find v_1/i_s and then we find v_{out}/v_1. Since there the input resistance of stage 2 (i.e. the PFET common source stage) is infinite, there will be no inter-stage voltage division and one can write,

$$R_m = \left(\frac{v_1}{i_s}\right)\left(\frac{v_{out}}{v_1}\right)$$

In the small signal model, the current i_s must entirely flow through the resistance r_{oc} (there is no other place for it to go) so:

$$v_1 = i_s r_{oc}$$

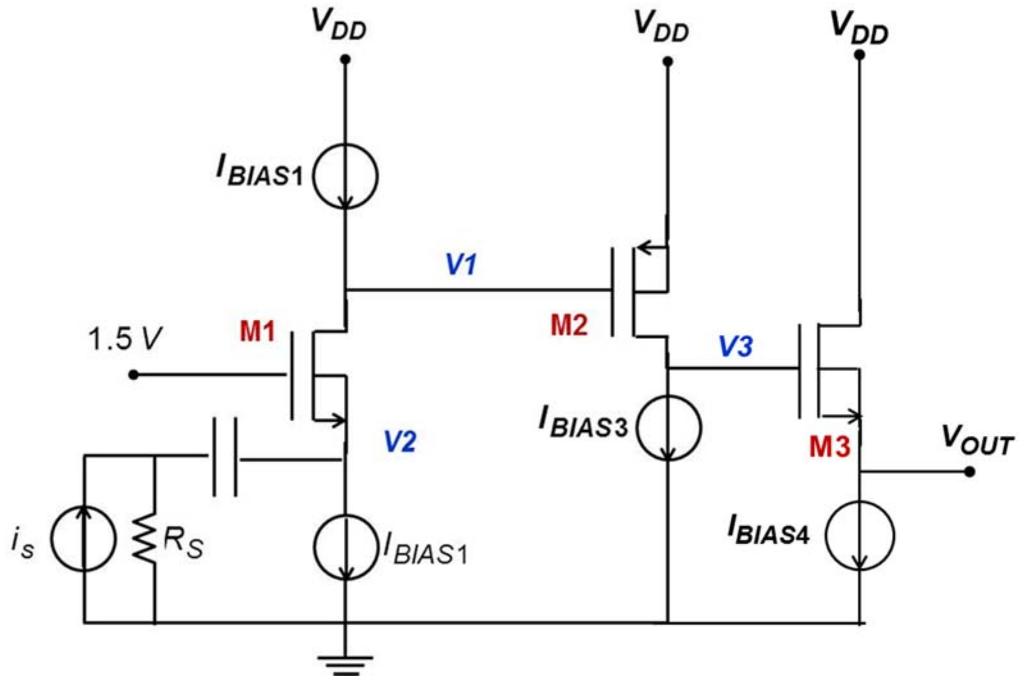
For the second common source stage,

$$\frac{v_{out}}{v_1} = -g_{mp} r_{op}$$

Therefore,

$$R_m = \left(\frac{v_1}{i_s}\right)\left(\frac{v_{out}}{v_1}\right) = -g_{mp} r_{op} r_{oc}$$

g)



Assuming the current source I_{BIAS4} is ideal, the output resistance of the amplifier will be the output resistance of the common drain stage (with $R = 0$) and equals:

$$\Rightarrow \frac{1}{R_{out}} = \frac{1}{r_{oc4}} + \frac{g_{mn} r_{on} + 1}{r_{on}} \approx g_{mn}$$

I choose $R_{out} = 1\text{k}\Omega$ then $g_{mn} = 1\text{mS}$. I choose I_{BIAS4} to equal 200 µA. Other values will work too. Since,

$$g_{mn} \approx \sqrt{2 k_n I_D}$$

$$\Rightarrow \frac{W_3}{L} = 50$$

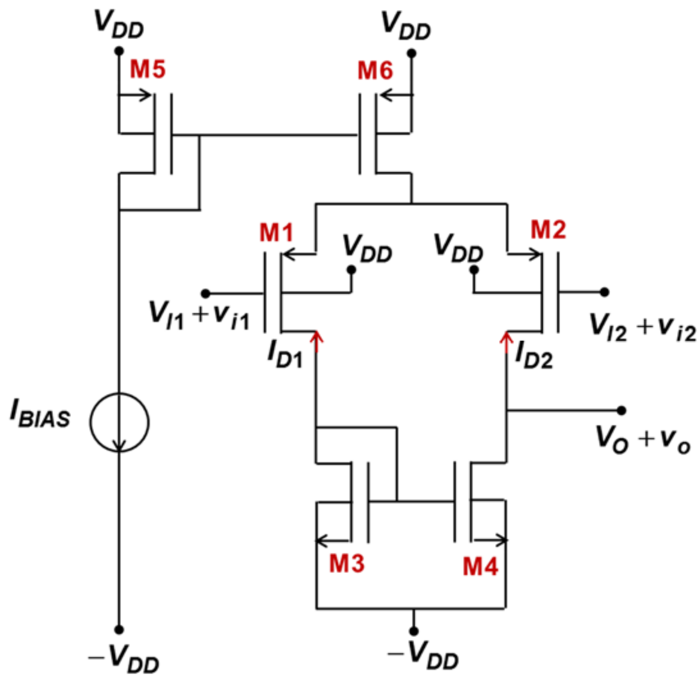
$$\Rightarrow W_3 \approx 200\ \mu\text{m}$$

I choose, $V_{OUT} = 1.8\text{ V}$,

$$\frac{k_n}{2}(V_{GS3} - V_{TN})^2 = \frac{W_3}{2L}\mu_n C_{ox}(V3 - 1.8 - 0.7)^2 = 200\ \mu A$$
$$\Rightarrow V3 = 2.9\ \text{V}$$

M2 will be safely operating in the saturation region (to keep M2 in saturation, $V3$ needs to be less than 4 V). The voltage gain of the last stage is approximately unity, so all specs are met.

Problem 9.2: (A Differential Amplifier)



The amplifier is DC biased such that $V_{I1} = V_{I2}$. M3 and M4 are matched. M1 and M2 are matched. And M5 and M6 are matched.

a) M6 and M5 provide the current biasing needed to bias the amplifier.

b) M3 and M4 serve as the current mirror load.

c) and d) The small signal model of the amplifier will resemble the one in the lecture handouts (except that PFETs will replace NFETs and vice versa and M6 will replace the current biasing source). See the Figure. So the answers for parts (c) and (d) can be pretty much copied from the lecture handouts. Assuming,

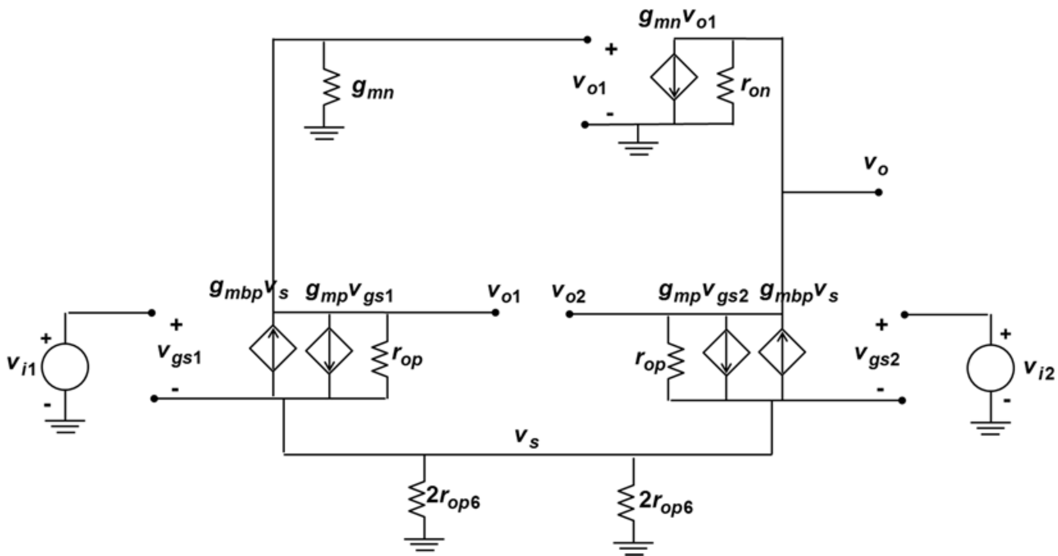
$$v_{i1} = -v_{i2} = v_{id}/2$$

Then,

$$A_{vd} = \frac{v_o}{v_{id}} \approx g_{mp}\left(r_{on} \,||\, r_{op}\right)$$

And,

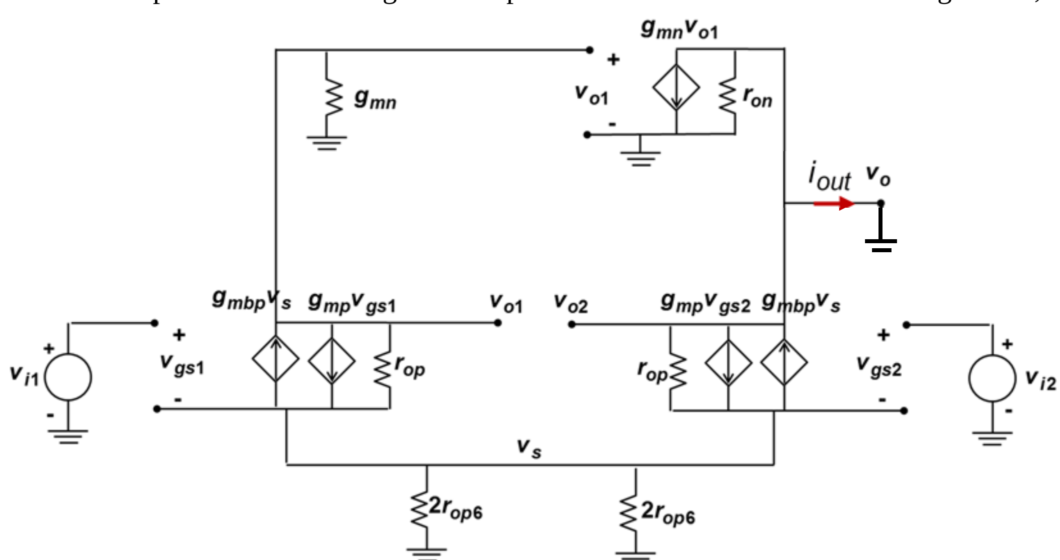
$$A_{vc} = \frac{v_o}{v_{ic}} \approx -\frac{\frac{g_{mp}}{g_{mn}} r_{op}}{r_{op} + \frac{1}{g_{mn}} + 2r_{op6} + (g_{mp} + g_{mbp}) r_{op} (2r_{op6})} \approx -\frac{1}{g_{mn}(2r_{op6})}$$



e) Easiest way to find the output resistance is to short the output and measure the short circuit output current in the differential mode. We already know the open circuit voltage in the differential mode,

$$v_o \approx g_{mp}(r_{on} \,||\, r_{op}) v_{id}$$

So if we find the short circuit output current as well, and take the ratio of the open circuit voltage and the short circuit output current we will get the output resistance. Consider the following circuit,



Assuming,

$$v_{i1} = -v_{i2} = v_{id}/2$$

And $v_s \approx 0$, we get, $v_{o1} \approx -\frac{g_{mp}}{g_{mn}}\frac{v_{id}}{2}$. Doing KCL at the output node we get,

$$g_{mn}v_{o1} + i_{out} + g_{mp}v_{gs2} = 0$$

$$\Rightarrow -g_{mp}\frac{v_{id}}{2} + i_{out} - -g_{mp}\frac{v_{id}}{2} = 0$$

$$\Rightarrow i_{out} = g_{mp}v_{id}$$

Finally,

$$R_{out} = \frac{g_{mp}(r_{op} \,||\, r_{on})v_{id}}{g_{mp}v_{id}} = (r_{op} \,||\, r_{on})$$

If you don't assume that $v_s \approx 0$, which is a better and more sensible approach given that the symmetry is not there at all, the same answer for the short circuit current can still be obtained. Doing KCL at the drain end of M1 gives,

$$-v_{o1}g_{mn} \approx g_{mp}\left(\frac{v_{id}}{2} - v_s\right) - g_{mbp}v_s + g_{op}(v_{o1} - v_s)$$

$$\Rightarrow v_{o1} \approx -\frac{g_{mp}}{g_{mn}}\left(\frac{v_{id}}{2} - v_s\right) + \frac{(g_{mbp} + g_{op})}{g_{mn}}v_s$$

Again doing KCL at the output node we get,

$$[g_{mn}v_{o1}] + i_{out} + \left[g_{mp}\left(-\frac{v_{id}}{2} - v_s\right) - g_{mbp}v_s - g_{op}v_s\right] = 0$$

$$\Rightarrow -g_{mp}\frac{v_{id}}{2} + i_{out} - g_{mp}\frac{v_{id}}{2} = 0$$

$$\Rightarrow i_{out} = g_{mp}v_{id}$$

Note that all factors containing v_s cancel out.

f) It is easiest to calculate the work done by the voltage sources. This equals 4 I_{BIAS} V_{DD}, which is 5 mW.