ECE 3150: Microelectronics

Spring 2016

Homework 8 **Due on April 07, 2016 at 7:00 PM**

Suggested Readings:

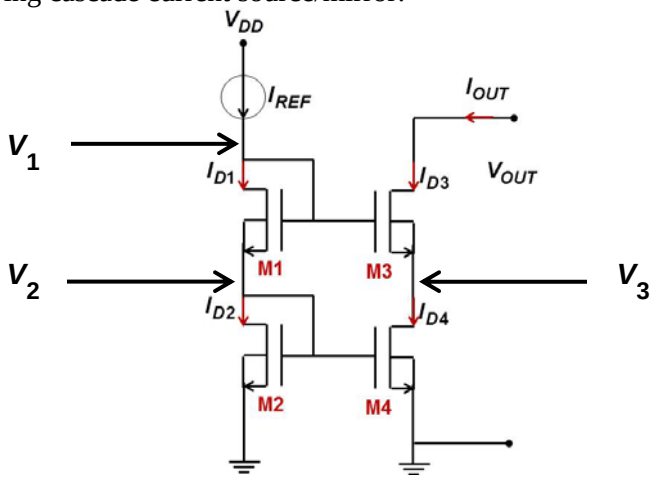
a) Lecture notes

Important Notes:

1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Unless noted otherwise, always assume room temperature.

Problem 8.1: (A cascode current source/mirror)

Consider the following cascade current source/mirror:



Assume that all NFETs are identical and their characteristics are given by:

$W = 10\ \mu\text{m}$
$L = 1\ \mu\text{m}$
$\mu_n C_{ox} = 200\ \mu A/V^2$
$\lambda_n = 0.1\,1/V$
$V_{DD} = 5.0\,V$
$V_{TN} = 0.5\,V$
$I_{REF} = 1\,mA$

a) Find the voltages V_1 and V_2.

b) What is the relationship between voltages V_3 and V_{OUT} ?

It might be obvious that if $V_{OUT} = V_1$ then $I_{OUT} = I_{REF}$. However, when $V_{OUT} \neq V_1$ then $I_{OUT} \neq I_{REF}$.

c) Supposed V_{OUT} is reduced. What is the value of V_{OUT} at which at least one NFET goes into the linear region? Which NFET?

d) Using the values of voltages V_1 and V_2 found in part (a), calculate and plot (not sketch) I_{OUT} vs V_{OUT} with V_{OUT} in the range 0 and 5 Volts.

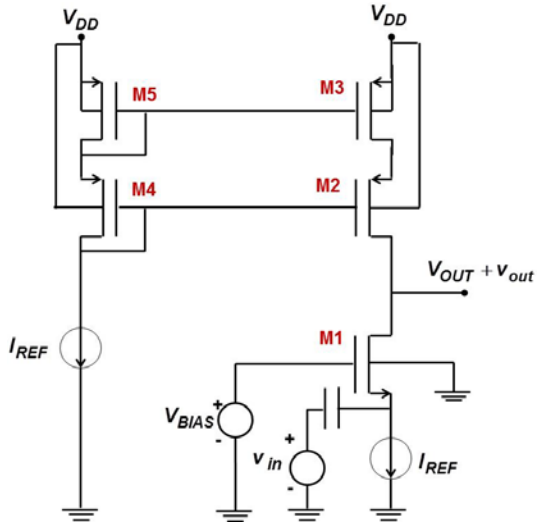
e) Draw a small signal circuit of the current source suitable for when looking in from the output terminals.

f) Use the small signal circuit of part (e) to find and expression for the output resistance r_{oc} of the current source.

g) Assuming $V_{OUT} = V_1$, find the actual numerical value of the output resistance r_{oc} using the expression found in part (f).

Problem 8.2: (A common gate amplifier)

Consider the following FET common gate amplifier. The two current sources shown have output resistances equal to r_{oc} .



a) Find the open circuit voltage gain $A_v = v_{out}/v_{in}$.

b) Find the input resistance R_{in} assuming a load resistor R_L is connected at the output.

c) Find the output resistance R_{out} assuming that the input voltage source v_{in} is replaced by a voltage source v_s is in series with a resistor R_s .

Problem 8.3: (Designing a cascode transconductance amplifier)

A transconductance (voltage to current) amplifier requires a large input resistance, a large output resistance and a large transcoductance gain. Suppose we require an output resistance greater than 10MΩ, a transconductance gain of at least 1 mS, and an infinite input resistance. The 2 μm FET technology available to us has the following specifications. We also have a single stable current source available on a chip.

$L = 2\ \mu\text{m}$

$\mu_n C_{ox} = 50\ \mu A/V^2$

$\mu_p C_{ox} = 25\ \mu A/V^2$

$\lambda_n = 0.05\ 1/V$

$\lambda_p = 0.02\ 1/V$

$V_{DD} = 5.0\ V$

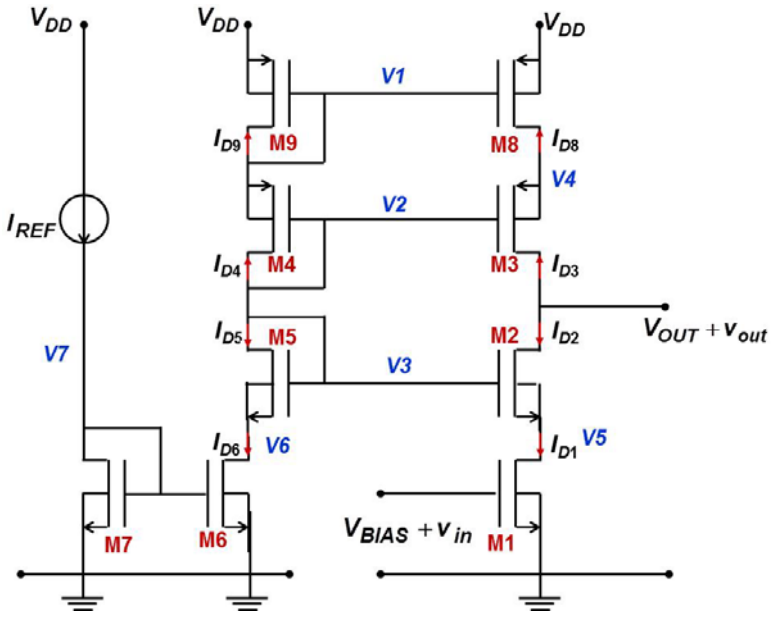
$V_{TN} = 1.0\ V$

$V_{TP} = -1.0\ V$

$I_{REF} = 100\ \mu A$

How do we choose a good design? The simplest idea would be to try a single or multistage cascade of CS stages. It will not be difficult to get a transconductance gain of 1 mS using CS stages. However, getting a large output resistance of 10 MΩ will not be easy. For example, suppose the final stage is a CS stage with a 100 μA current going through a NFET. The output resistance of the NFET, which will set the upper limit for the output resistance of the amplifier, will be $\sim (\lambda_n I_D)^{-1}$ which equals 200 kΩ. Therefore, using single or cascaded CS stages one can never hope to meet the design specs. A different design is required. A cascode design can work. The design of a cascode transconductance amplifier is shown below.

Suppose we choose the current I_{D1} to equal 100 μA. Rest of the design process follows step by step after making this choice.



a) Assuming that the resistance looking into the PFET biasing source on top of the cascode is very large, what value should one choose for the width W_1 of M1 such that the transconductance of the cascode amplifier is around 1 mS?

b) What are the output resistances of M1 and M2 at the chosen bias point? What are the output resistances of M3 and M8 at the chosen bias point?

c) Assuming that the resistance looking into the PFET biasing source on top of the cascode is very large, what value should one have for the transconductance g_{m2} of M2 such that the output resistance of the cascode amplifier is around 20 MΩ?

d) Assuming for a moment that:

$$I_{D2} \approx \frac{k_n}{2}(V_{GS2} - V_{TN})^2$$

what value should one choose for the width W_2 of M2 such that the transconductance g_{m2} of M2 has the value found in part (c)?

e) Suppose we want the resistance looking into the PFET biasing source on top of the cascode to be 100 MΩ (i.e. very large). What value should one have for the transconductance g_{m3} of M3?

f) Assuming for a moment that:

$$I_{D3} \approx -\frac{k_p}{2}(V_{GS3} - V_{TP})^2$$

what value should one choose for the width W_3 of M3 such that the transconductance g_{m3} of M3 has the value found in part (e)?

Now we choose $W_3 = W_8$

g) To bias the circuit properly, what should be the widths of M5, M4, and M9?

Next, we choose $W_6 = W_1$.

h) Now what should be W_7 ?

i) Find the voltages V1, V2, and V3.

j) Find the voltages V4, V5, V6 and V7.

k) What should be V_{BIAS} ?

l) Suppose the on chip current source I_{REF} is no longer available. But you are allowed to choose a resistor in its place. What value resistor would you use to keep the rest of the circuit functioning as before?