ECE 3150: Microelectronics

Spring 2016

Homework 7 **Due on March. 17, 2016 at 7:00 PM**

Suggested Readings:

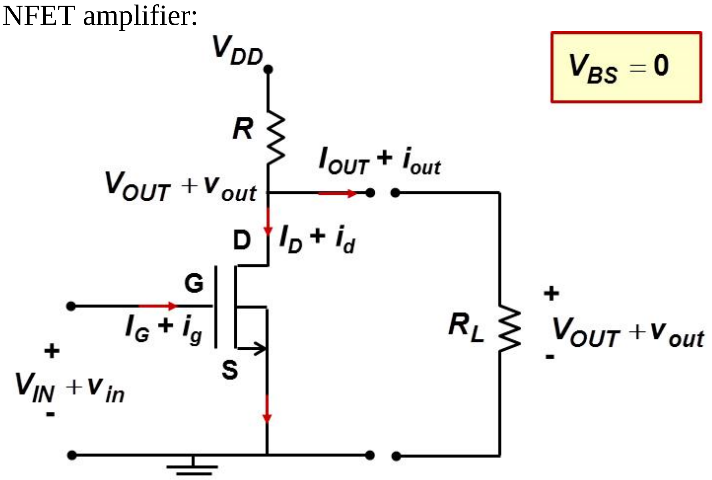
a) Lecture notes

Important Notes:

1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Unless noted otherwise, always assume room temperature.
3) Midterm on March 24, 7:30-10:00 PM in KMBB11.

Problem 7.1: (A Simple NFET Amplifier)

Consider the following NFET amplifier:



For the NFET assume:

$W = 10\ \mu\text{m}$

$L = 1\ \mu\text{m}$

$\mu_n C_{ox} = 200\ \mu A/V^2$

$\lambda_n = 0.1 1/V$

$V_{DD} = 2.5\ V$

$R_L = 10\ \text{k}\Omega$

$V_{TN} = 0.5\ V$

$N_a = 10^{17}\ \text{cm}^{-3}$

In the following parts, assume that the load resistor R_L is NOT connected to the output.

a) Generally one would like to keep the resistor R large. But if it is too large, the FET could go into the linear region for a given desired value of the DC drain current I_D. Suppose you are at liberty to choose any value of the DC input bias voltage V_{IN}. For every value of V_{IN} above V_{TN} the value of the resistor R has to be within a range in order to keep the FET in the saturation region of operation. For values of V_{IN} between 0.5 and 2.5 Volts, find the maximum (R_{max}) and the minimum (R_{min}) values of the resistance R needed to keep the FET working the saturation region. Plot R_{max} and R_{min} on the same plot as a function of V_{IN}.

b) Suppose you need to the keep the DC voltage at the output V_{OUT} equal to $1.5\,V$. And you also need to keep the small signal gain, and therefore g_m, reasonably high, so you choose $I_D = 200\ \mu A$. What should be the values of the resistor R and the input bias voltage V_{IN} needed to meet these objectives? Or can these objectives even be met while keeping the FET in the saturation region?

c) With the numerical value of the resistor as in part (b), and a varying input voltage V_{IN}, what are the maximum and the minimum values of the ouput voltage V_{OUT} such that the FET remains in the saturation region?

d) With the value of the resistor as in part (b), what are the maximum and the minimum values of the input voltage V_{IN} such that the FET remains in the saturation region?

e) With the value of the resistor as in part (b), compute and plot (sketches not acceptable) the transfer curve $V_{OUT} - vs - V_{IN}$ and indicate regions in which the FET is in the cut off, linear, and saturation regions.

f) With the value of the resistor and the biasing scheme as in part (b), what is the open circuit small signal voltage gain $A_v = v_{out}/v_{in}$ (i.e. the voltage gain with the load resistor disconnected)? Need a numerical number as an answer and not just a formula.

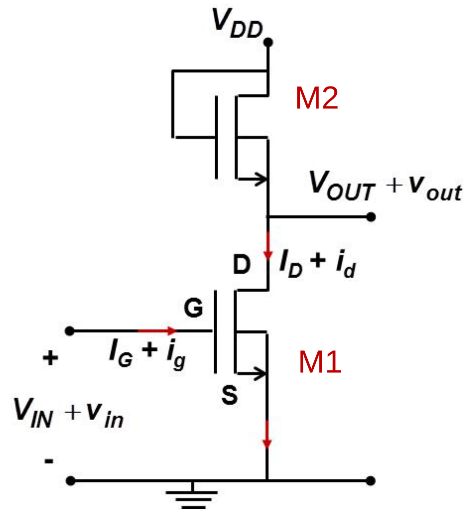
Now suppose the load resistor R_L is connected to the output of the amplifier. Its presence will change things significantly.

g) Suppose your biasing scheme, including values of V_{IN} and R are as in part (b) above. With the load resistor now connected, what is the new output voltage V_{OUT}? Hint: it is not going to be 1.5 Volts anymore. And what is I_{OUT}?
Lesson: loading can affect the DC biasing of an amplifier!

h) Suppose your biasing scheme, including values of V_{IN} and R are as in part (b) above. With the load resistor now connected, what is the small signal voltage gain $A_v = v_{out}/v_{in}$? Need a numerical number as an answer and not just a formula. Has it decreased or increased compared to the case when the load resistor was not connected?
Lesson: loading can affect the small signal performance of an amplifier!

Problem 7.2: (NFET Loaded NFET Amplifier)

Consider the following circuit:



Assume that for both NFETs:

$W = 10\ \mu\text{m}$

$L = 1\ \mu\text{m}$

$\mu_n C_{ox} = 200\ \mu A/V^2$

$\lambda_n = 0.1 1/V$

$V_{DD} = 2.5\,V$

$V_{TN} = 0.5\,V$

$N_a = 10^{17}\,\text{cm}^{-3}$

a) If $V_{IN} = 1.25\text{ V}$, find V_{OUT} ? Is the bottom NFET in linear or saturation region?

b) If $V_{IN} = 2.0\text{ V}$, find V_{OUT} ? Is the bottom NFET in linear or saturation region?

c) What is the highest voltage V_{OUT} can take if both the FETs are to remain in saturation? What is the corresponding input voltage V_{IN} ?

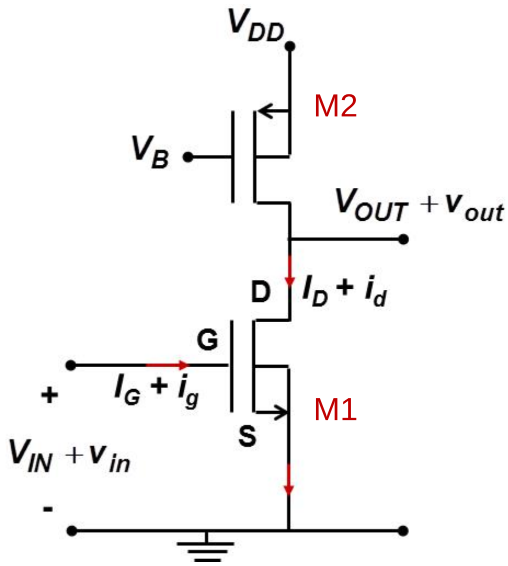
d) What is the lowest voltage V_{OUT} can take if both the FETs are to remain in saturation? What is the corresponding input voltage V_{IN} ?

e) Draw a small signal circuit for the amplifier and find an expression for the open circuit voltage gain $A_v = v_{out}/v_{in}$.

f) Suppose $V_{IN} = 1.25\text{ V}$. Find the values of g_{m1}, g_{m2}, r_{o1}, r_{o2} for the two NFETs and then find the value of the voltage gain $A_v = v_{out}/v_{in}$ at this bias point.

Problem 7.3: (PFET Loaded NFET Amplifier)

Consider the following circuit:



Assume that for the NFET:

$W = 10\ \mu\text{m}$

$L = 1\ \mu\text{m}$

$\mu_n C_{ox} = 200\ \mu A/V^2$

$\lambda_n = 0.1\ 1/V$

$V_{TN} = 0.5\ V$

$N_a = 10^{17}\ \text{cm}^{-3}$

And assume that for the PFET:

$W = 20\ \mu\text{m}$

$L = 1\ \mu\text{m}$

$\mu_p C_{ox} = 100\ \mu A/V^2$

$\lambda_p = 0.1\ 1/V$

$V_{TP} = -0.5\ V$

$N_d = 10^{17}\ \text{cm}^{-3}$

And:

$V_{DD} = 2.5\ V$

a) If $V_B = 1.25$ V, and $V_{IN} = 1.25$ V, what is V_{OUT} ?

b) If $V_B = 1.25$ V, what is the highest voltage V_{OUT} can take if both the FETs are to remain in saturation? What is the corresponding input voltage V_{IN} ?

c) If $V_B = 1.25$ V, what is the lowest voltage V_{OUT} can take if both the FETs are to remain in saturation? What is the corresponding input voltage V_{IN} ?

d) Draw a small signal circuit for the amplifier and find an expression for the open circuit voltage gain $A_v = v_{out}/v_{in}$.

e) If $V_B = 1.25$ V, and $V_{IN} = 1.25$ V, find the values of g_{m1} , g_{m2} , r_{o1} , r_{o2} for the two FETs and then find the value of the voltage gain $A_v = v_{out}/v_{in}$ at this bias point.

f) Based on what you have found, would you use the amplifier of problem 7.1(f), problem 7.2(f) or the amplifier of this problem 7.3(e) for high gain applications?