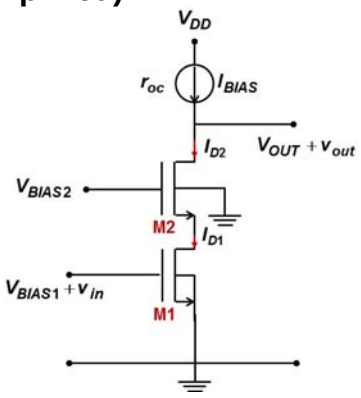
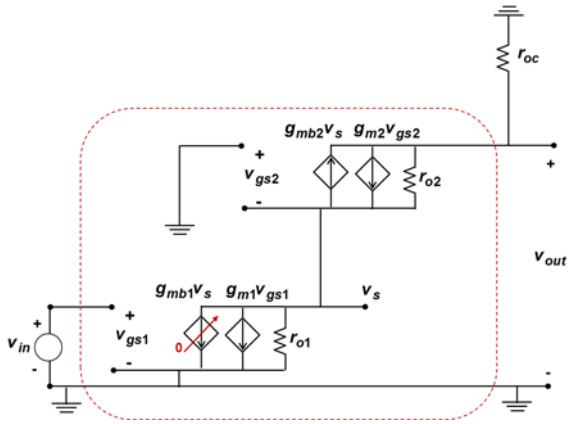
ECE Homework 12 Solutions

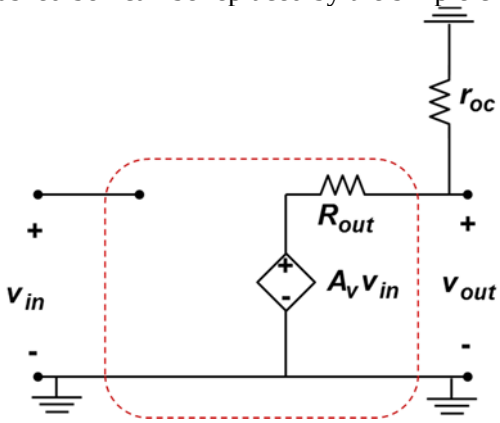
Problem 12.1: (Cascode simplified)



The small signal model is:



Everything inside the dashed box can be replaced by the simple circuit shown below:



a) What is the value of the voltage gain A_V?

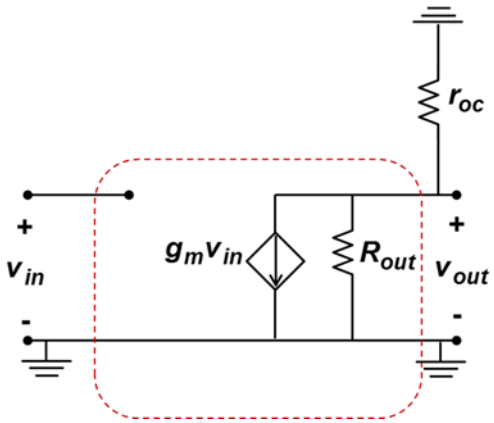
The voltage gain is just what the open circuit voltage gain of a cascode would be if $r_{oc} = \infty$.

$$A_V \approx [-g_{m1}r_{o1}][(g_{m2} + g_{m2b})r_{o2}]$$

b) What is the value of the output resistance R_{out}?

Again, the output resistance is just what the output resistance of a cascode would be if $r_{oc} = \infty$.

$$R_{out} = [r_{o2} + R_{out1} + r_{o1}r_{o2}(g_{m2} + g_{mb2})]$$



c) One can even make the cascode appear like a single transistor in the small signal model, as shown above. What is the value of g_m ?

Note that if $r_{oc} = \infty$ then the output voltage given by both the models should be the same. Therefore,

$$v_{out} = -g_m R_{out} v_{in} = A_V v_{in}$$

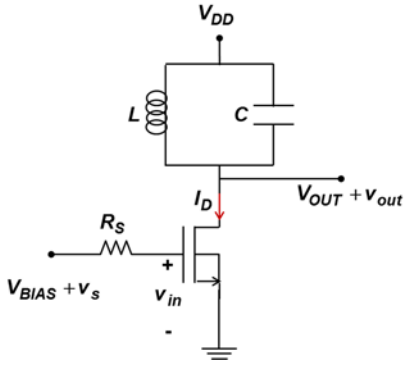
$$\Rightarrow g_m R_{out} = -A_V$$

$$\Rightarrow g_m = \frac{g_{m1} r_{o1} r_{o2} (g_{m2} + g_{mb2})}{[r_{o2} + R_{out1} + r_{o1} r_{o2} (g_{m2} + g_{mb2})]} \approx g_{m1}$$

d) See if now you can more easily understand the analysis of the folded cascode differential amplifier of the last homework set.

See the solutions for homework 11.

Problem 12.2: (RF Amplifier/Filter in one)



Suppose:

$W/L = 8$ $\quad C_{gs} = 0.5$ fF $\quad C_{gd} = 0.1$ fF

$\mu_n C_{ox} = 200\ \mu A/V^2$ $\quad R_S = 10$ kΩ

$\lambda_n = .04\ 1/V$ $\quad L = 25$ nH $\quad C = ?$ pF

$V_{DD} = 3.5$ $\quad V_{BIAS} = 2.5$ $\quad V_{TN} = 0.5$ V

a) What ought to be the value of the capacitor C so that the maximum gain occurs at ~1 GHz?

Impedance of the LC circuit on top is:

$$Z(\omega) = \frac{j\omega L}{(j\omega)^2 LC + 1}$$

Impedance is maximum when:

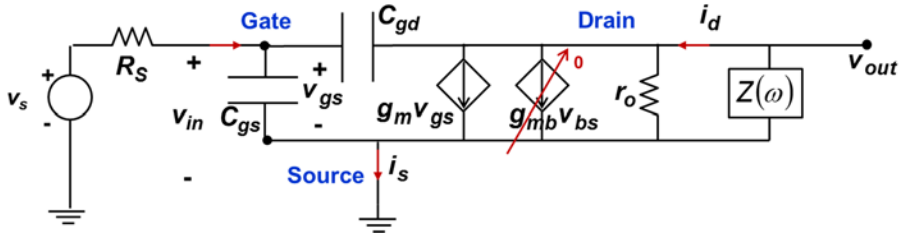
$$\omega = \frac{1}{\sqrt{LC}}$$

If one wants $\frac{1}{\sqrt{LC}} = 1\,\text{GHz}$, then $C \approx 1\,\text{pF}$.

b) What is the impedance $Z(\omega)$ of the load sitting on top of the FET?

$$Z(\omega) = \frac{j\omega L}{(j\omega)^2 LC + 1}$$

c) Draw a small signal model of the circuit. Use the high frequency small signal model for the FET. Represent the LC load by its impedance $Z(\omega)$.



d) Find the small signal voltage gain of the amplifier:

$$A_V(\omega) = \frac{v_{out}(\omega)}{v_s(\omega)}$$

Proceed as follows:

i) Do a KVL at the output node to get:

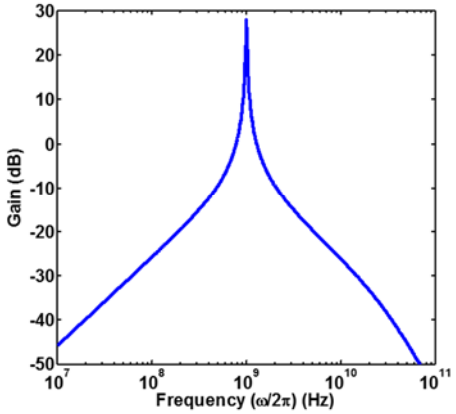
$$\frac{v_{out}(\omega)}{v_{in}(\omega)} = -\frac{g_m Z - j\omega Z C_{gd}}{1 + g_o Z + j\omega Z C_{gd}} = -g_m (Z \,||\, r_o) \frac{1 - j\omega \frac{C_{gd}}{g_m}}{1 + j\omega C_{gd} (Z \,||\, r_o)} = -h_1(\omega)$$

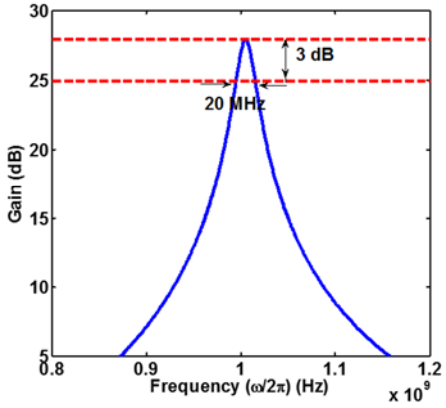
ii) Then do a KCL at the input node to get:

$$\frac{v_{in}(\omega)}{v_s(\omega)} \approx \frac{1}{1 + j\omega \left[C_{gs} + C_{gd} (1 + h_1(\omega)) \right] R_S}$$

$$A_V(\omega) = \frac{v_{out}(\omega)}{v_s(\omega)} = \frac{v_{out}(\omega)}{v_{in}(\omega)} \frac{v_{in}(\omega)}{v_s(\omega)}$$

e) Plot the gain (in dB units: i.e. $20 \log_{10}|Av|$) as a function of frequency from 10 MHz to 100 GHz. Use matlab or your favorite plotting program.





f) What is the maximum gain (in dB units) you see in your plot in part (e)?
Around 27.9 dB.

g) What is the full width half max (FWHM) gain bandwidth you see in your plot in part (e)?
Around 20 MHz.

h) Derive an analytic expression for the FWHM gain bandwidth and show that it matches what you see in your plot.

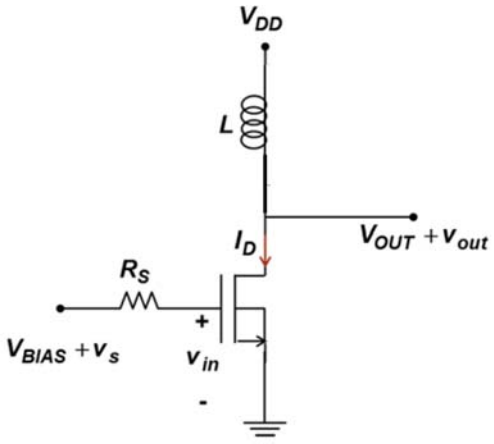
Looking at the small signal model one can see that low frequencies when both C_{gd} and C_{gs} are open, the effective resistance that appears in parallel with the L and C is the output resistance r_o of the FET. Therefore, the amplifier gain is essentially (at these low frequencies),

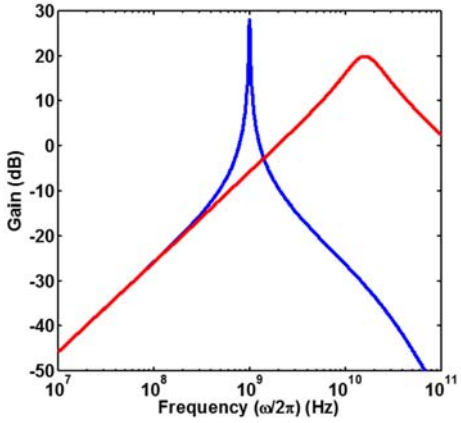
$$-g_m(Z \,||\, r_o) = -g_m \frac{\frac{j\omega}{C}}{\frac{1}{LC} + j\omega\frac{1}{r_o C} + (j\omega)^2}$$

The above looks like the expression for the response of a damped simple harmonic oscillator. The FWHM frequency bandwidth is $\frac{1}{2\pi\, r_o C}$ (in Hz) and comes out to be very close to ~20 MHz.

i) A simple inductor loaded CS stage can also perform well at high frequencies compared to a resistively loaded CS stage in terms of gain and output voltage swing. Suppose in the problem, the LC circuit is replaced by just an inductor of inductance 25 nH. Plot the gain (in dB units: i.e. $20\log_{10}|Av|$) as a function of frequency from 10 MHz to 100 GHz.

Now $Z(\omega) = j\omega L$. The plot is shown below.





12.3)

a) As long as $V_{DS} > V_{GS} - V_{TN}$ for the NFET, or $V_{OUT} > V_{DD} - V_{TN}$, the NFET will be in Saturation. In Saturation,

$$C_L \frac{dV_{OUT}}{dt} = -I_D = -\frac{k_n}{2}(V_{DD} - V_{TN})^2$$

$$\Rightarrow V_{OUT}(t) = V_{OUT}(t=0) - \frac{k_n}{2C_L}(V_{DD} - V_{TN})^2 t$$

$$= V_{DD} - \frac{k_n}{2C_L}(V_{DD} - V_{TN})^2 t$$

The time it takes for the output to reach $V_{DD} - V_{TN}$ is

$$t_1 = \frac{2C_L}{k_n} \frac{V_{TN}}{(V_{DD} - V_{TN})^2}$$

For $t > t_1$, NFET will be in the Linear region, where,

$$C_L \frac{dV_{OUT}}{dt} = I_D = -k_n \left(V_{DD} - V_{TN} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

{ boundary condition $V_{OUT}(t=0) = V_{DD} - V_{TN}$.

$$\int_{V_{DD}-V_{TN}}^{0.1V_{DD}} \frac{dV_{OUT}}{\left(2(V_{DD} - V_{TN}) - V_{OUT}\right) V_{OUT}} = -\frac{k_n}{2C_L} t$$

$$\frac{1}{2(V_{DD} - V_{TN})} \log\left[\frac{0.1V_{DD}}{2(V_{DD} - V_{TN}) - 0.1V_{DD}} \right] = -\frac{k_n}{2C_L} t$$

$$t = -\frac{2C_L}{k_n (V_{DD} - V_{TN})} \times \frac{1}{2} \log\left[\frac{0.1V_{DD}}{2(V_{DD} - V_{TN}) - 0.1V_{DD}} \right]$$

$$\text{Total time} = \frac{2C_L}{k_n (V_{DD} - V_{TN})} \left\{ \frac{V_{TN}}{V_{DD} - V_{TN}} - \frac{1}{2} \log\left[\frac{0.1V_{DD}}{2(V_{DD} - V_{TN}) - 0.1V_{DD}} \right] \right\}$$

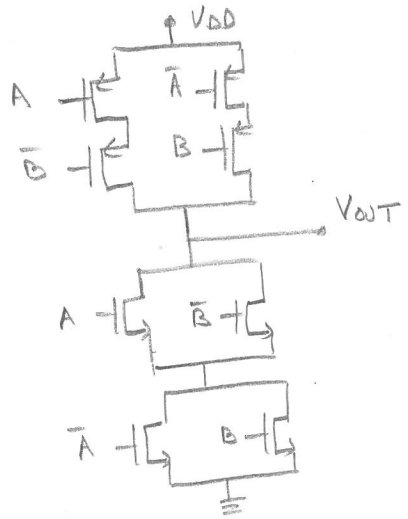
b) The expression for fall time will be the same as in part (a) if we replace k_n in there by $\frac{k_n}{2}$ because two NFETs in series with the same gate voltage is like one longer NFET that is twice as long.

c) If we consider two NFETs as one longe FET then the bottom FET never operates in saturation. It always operates in the linear region.

d) Yes. The top FET goes from saturation into the linear region when $V_{OUT} < V_{DD} - V_{TN}$.

12.4)

$A \oplus B = A\bar{B} + \bar{A}B$. So the pull-up network could be:



The pull-down network is just the dual of it.

We will need to generate $\bar{A}$ and $\bar{B}$ using inverters. So we will need total of 12 FETs.