Department of Electrical and Computer Engineering, Cornell University

ECE 3150: Microelectronics

Spring 2016

Homework 12 **Due on May 05, 2016 at 7:00 PM**

Suggested Readings:

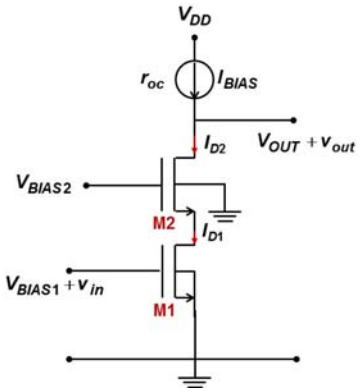
a) Lecture notes

Important Notes:

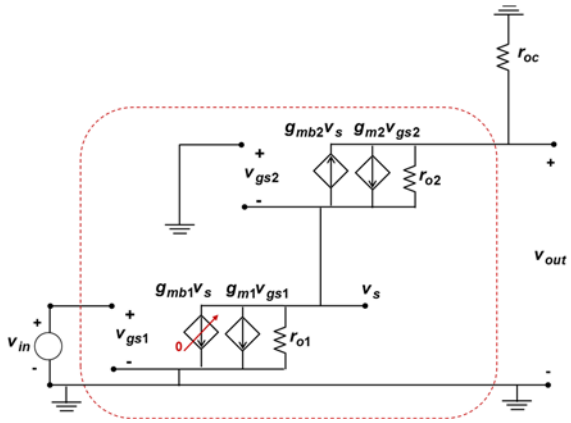
1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Unless noted otherwise, always assume room temperature.

Problem 12.1: (Cascode simplified)

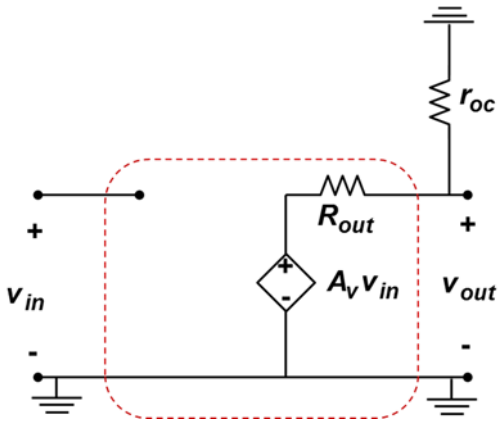
Many of you try to analyze the cascode topology from scratch whenever it appears embedded in a more complex network. One of the basic engineering principles is "abstraction" – the ability to abstract away the details in order to more easily build complex things using abstract building blocks. The cascode can be dealt in the same way. Consider the cascode circuit from the lecture handouts:



The small signal model is:

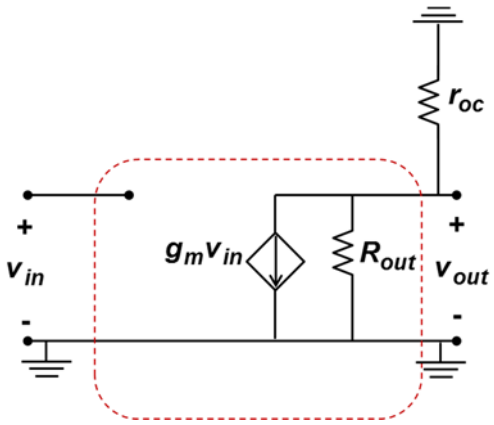


Everything inside the dashed box can be replaced by the simple circuit shown below:



a) What is the value of the voltage gain A_V ? Do not blindly copy from the lecture notes – we often include r_{OC} as a part of the abstraction but here we have placed r_{OC} outside the abstraction box. Do not make approximations.

b) What is the value of the output resistance R_{out} ? Do not blindly copy from the lecture notes – we often include r_{OC} as a part of the abstraction but here we have placed r_{OC} outside the abstraction box. Do not make approximations.



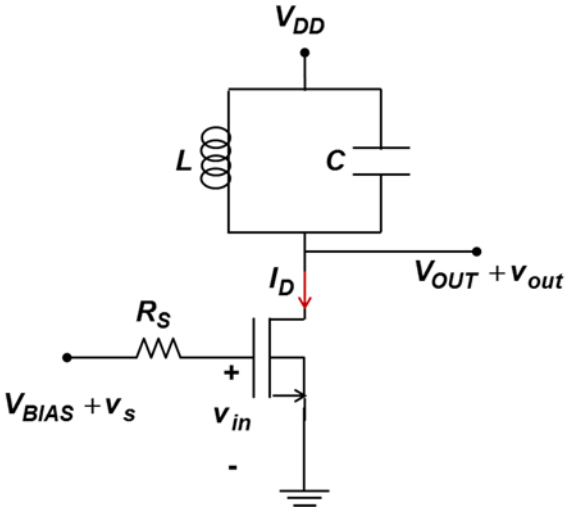
c) One can even make the cascode appear like a single transistor in the small signal model, as shown above. What is the value of g_m ? Do not make approximations.

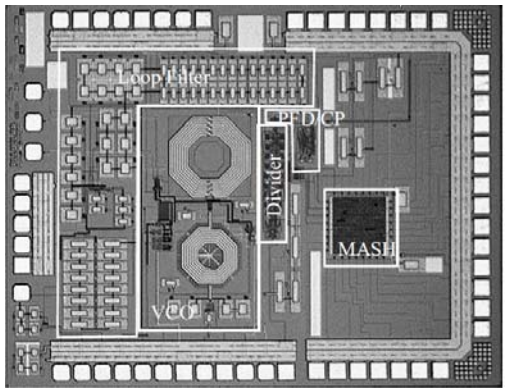
d) See if now you can more easily understand the analysis of the folded cascode differential amplifier of the last homework set.

Problem 12.2: (RF Amplifier/Filter in one)

Many CMOS RF receiving modules in wireless systems use a RF band-pass filter and an amplifier combination before demodulating or mixing down the RF signal. Often the filtration and amplification processes can be combined in a single stage. One such CMOS stage is shown in the figure below and has been implemented in the 100 nm CMOS technology. The “100 nm” refers to the FET channel length. The CS stage is loaded with a LC circuit. Placing an inductor in a CMOS chip is not an easy task but can be done. The figure below also shows the micrograph of a CMOS GSM receiver chip with two integrated spiral inductors.

You will need to figure out the frequency response of the circuit. The operation of the circuit is as follows: We know that the resistance of the load sitting on top of the FET determines the gain of a CS stage. If a simple resistor is replaced by an LC circuit then the impedance of the LC circuit will be frequency dependent and therefore the CS stage gain can also be made frequency dependent. At low frequencies we expect the inductor to act like a short and therefore the amplifier gain will be very small. At high frequencies we expect the capacitor to act like a short and therefore the gain will again be very small. At some intermediate frequency the gain will be maximum and this maximum gain will occur in a very narrow band of frequencies. One can choose values for L and C so that the maximum gain occurs at around ~1 GHz (which is close to the carrier frequency used by mobile systems, e.g. GSM).





Suppose:

$W/L = 8$ $C_{gs} = 0.5\,\text{fF}$ $C_{gd} = 0.1\,\text{fF}$

$\mu_n C_{ox} = 200\ \mu A/V^2$ $R_S = 10\,\text{k}\Omega$

$\lambda_n = .04\ 1/V$ $L = 25\,\text{nH}$ $C = ?\ \text{pF}$

$V_{DD} = 3.5$ $V_{BIAS} = 2.5$ $V_{TN} = 0.5\ \text{V}$

a) What ought to be the value of the capacitor C so that the maximum gain occurs at ~1 GHz?

b) What is the impedance $Z(\omega)$ of the load sitting on top of the FET?

c) Draw a small signal model of the circuit. Use the high frequency small signal model for the FET. Represent the LC load by its impedance $Z(\omega)$.

d) Find the small signal voltage gain of the amplifier:

$$A_V(\omega) = \frac{v_{out}(\omega)}{v_S(\omega)}$$

The best way to do it is to first find:

$$v_{out}/v_{in}$$

and then find:

$$v_{in}/v_S$$

and then multiply the two.

e) Plot the gain (in dB units: i.e. $20\log_{10}|Av|$) as a function of frequency from 10 MHz to 100 GHz. Use matlab or your favorite plotting program.

f) What is the maximum gain (in dB units) you see in your plot in part (e)?

g) What is the full width half max (FWHM) gain bandwidth you see in your plot in part (e)? FWHM gain bandwidth is the range of frequencies (in Hz) over which the gain (in dB) is larger than the peak gain value (in dB) minus 3 dB. In other words, FWHM gain bandwidth is the range of frequencies over which the square magnitude of the gain is more than one-half of the peak gain value.

h) Derive an analytic expression for the FWHM gain bandwidth and show that it matches what you see in your plot.
Hint: using open circuit time constant technique determine the effective resistance associated with the LC circuit.

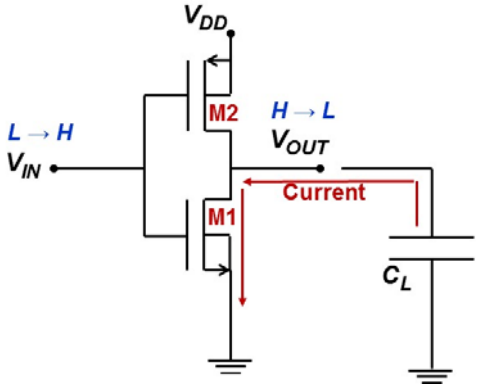
i) A simple inductor loaded CS stage can also perform well at high frequencies compared to a resistively loaded CS stage in terms of gain and output voltage swing. Suppose in the problem, the LC circuit is replaced by just an inductor of inductance 25 nH. Find the small signal voltage gain of the amplifier:

$$A_V(\omega) = \frac{v_{out}(\omega)}{v_s(\omega)}$$

Plot the gain (in dB units: i.e. $20\log_{10}|Av|$) as a function of frequency from 10 MHz to 100 GHz. Use matlab or your favorite plotting program. You will note that there is no bandpass filtering but the gain still peaks around 15-16 GHz and is pretty large. You could not have obtained such a large gain at such high frequencies using a standard resistive load.

Problem 12.3: (CMOS Logic: Fall times)

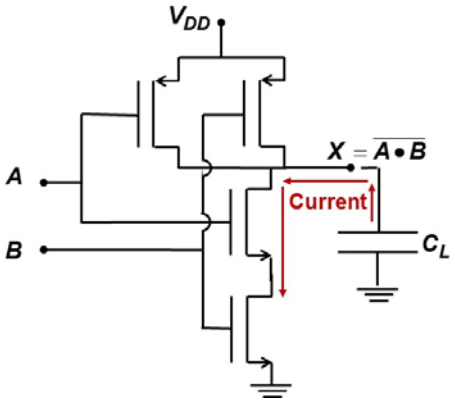
a) Consider the following inverter from the lecture handouts:



Suppose the output capacitor was charged HIGH ($\sim V_{DD}$) at time zero. The input transitioned from LOW to HIGH. The output capacitor will discharge through the FET M1. For simplicity we will define the fall time t_f to be the time in which the output goes from V_{DD} to $0.1V_{DD}$. Show that the fall time is:

$$t_f \approx \frac{2C_L}{k_n(V_{DD}-V_{TN})}\left\{\frac{V_{TN}}{V_{DD}-V_{TN}} - \frac{1}{2}\ln\left[\frac{0.1V_{DD}}{2(V_{DD}-V_{TN})-0.1V_{DD}}\right]\right\}$$

b) Now consider the following NAND gate:



Suppose the output capacitor was charged HIGH (~V_{DD}) at time zero. Both the inputs transitioned from LOW to HIGH. The output capacitor will discharge through the NFETs. For simplicity we will define the fall time t_f to be the time in which the output goes from V_{DD} to $0.1V_{DD}$. Find an expression for the fall time.

c) In part (b), does the bottom NFET ever go into the linear region during the discharge process? Explain?

d) In part (b), does the top NFET ever go into the linear region during the discharge process? Explain?

Problem 12.4: (CMOS Logic: The XOR gate)

a) Design a CMOS XOR gate using the minimum number of PFETs and NFETs (do not Google the answer). The truth table for the XOR gate is:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0