Department of Electrical and Computer Engineering, Cornell University

ECE 3150: Microelectronics

Spring 2016

Homework 10 **Due on April 21, 2016 at 7:00 PM**

Suggested Readings:

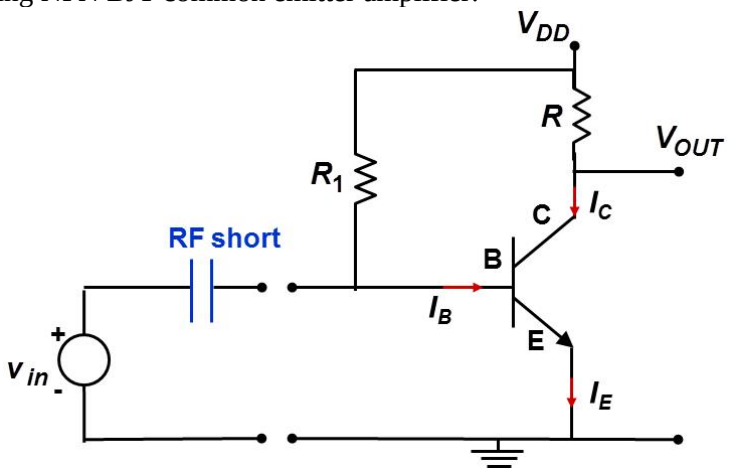
a) Lecture notes

Important Notes:

1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Unless noted otherwise, always assume room temperature.

Problem 10.1: (A NPN Common Emitter Amplifier)

Consider the following NPN BJT common emitter amplifier:



For the BJT assume:

$\beta_{FO} = 100$
$V_{BE-ON} = 0.6\,V$
$V_{CE-SAT} = 0.2\,V$
$V_{DD} = 5.0\,V$
$V_A = 50\,V$

For BJTs, the collector current in the forward active region is,

$I_C = \beta_F I_B$

The current gain factor β_F depends on the width of the base region, which in turn depends on the collector voltage because of base-width modulation as discussed in the lecture handouts (the depletion region of the reversed biased base-collector junction expands into the base region when the collector

voltage is increased thereby reducing the width of the base region). Therefore, the current gain factor β_F depends on the collector voltage as well. One can model this dependence using a convenient analytical expression,

$$\beta_F = \beta_{FO} e^{\frac{V_{CE}}{V_A}} \approx \beta_F \left(1 + \frac{V_{CE}}{V_A}\right) \qquad \{ I_B > 0, V_{CE} > V_{CE-SAT}$$

This implies that,

$$g_o = \frac{\partial I_C}{\partial V_{CE}} = \frac{\partial \beta_F}{\partial V_{CE}} I_B = \frac{\beta_F}{V_A} I_B = \frac{I_C}{V_A}$$

which is the expression given in the lecture handout for the output conductance of BJTs. **Whenever the early voltage is specified, as in this problem, you should use the V_{CE} -dependent expression for the current gain β_F .**

Compare the above to what we did for FETs. In a FET in saturation,

$$I_D = \frac{k_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda_n V_{DS})$$

And,

$$g_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{k_n}{2}(V_{GS} - V_{TN})^2 \lambda_n \approx \lambda_n I_D$$

The problem below is very similar to problem 7.1 for the NFET. It will be helpful if you compare parts of this problem with what you did in the same part in problem 7.1.

In the following parts, the small signal source at the input is not connected.

a) Generally one would like to keep the resistor R large in order to get a large voltage gain. But if it is too large, the BJT could go into the saturation region. Suppose you are at liberty to choose any value of the DC base current I_B. For every value of $I_B > 0$ the value of the resistor R has to be within a range in order to keep the BJT in the forward active region of operation. For values of I_B between 5 and 50 μA, find the maximum ($R_{\max}$) and the minimum ($R_{\min}$) values of the resistance R needed to keep the BJT operating in the forward active region. Plot $R_{\max}$ and $R_{\min}$ on the same plot as a function of I_B.

b) Suppose you need to the keep the DC voltage at the output V_{OUT} equal to $2.5\,V$. And you also need to keep the small signal gain, and therefore g_m, reasonably high, so you choose $I_C = 1\,mA$. What should be the values of the resistor R and the base current I_B needed to meet these objectives?

c) With the numerical value of the resistor as in part (b), and a varying base current I_B, what are the maximum and the minimum values of the ouput voltage V_{OUT} such that the BJT remains in the forward active region?

d) With the value of the resistor as in part (b), what are the maximum and the minimum values of the base current I_B such that the BJT remains in the forward active region?

e) The DC biasing of a BJT requires some care. In the circuit shown, the base-emitter junction of the BJT is effectively current biased using the resistor R_1. And R_1 should be much larger than the small signal resistance r_π of the base-emitter junction otherwise the small signal gain gets spoiled, as you will see below. For the value of the base current I_B found in part (b), what should be the value of the biasing resistor R_1?

In the following parts, the small signal source at the input is connected via a DC-blocking capacitor that is effectively a short at the RF frequencies of interest.

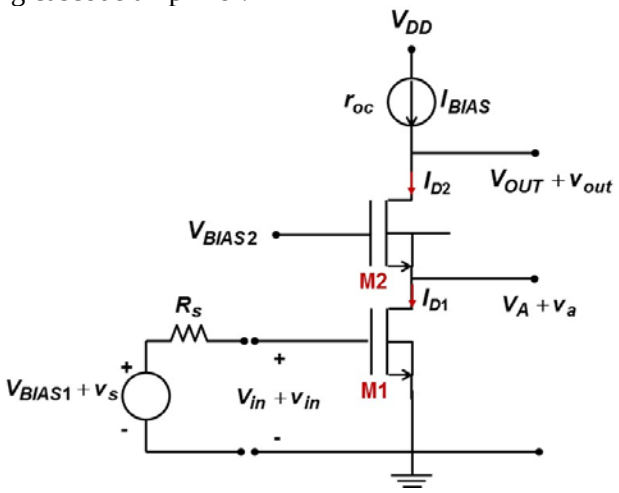
f) Draw a small signal model of the circuit, and find an expression for the open circuit small signal voltage gain $A_V = v_{out}/v_{in}$. Now explain what will happen if $R_1 << r_\pi$.

g) With the values of the resistors, R and R_1, as in part (b) and part (e), what is the open circuit small signal voltage gain $A_V = v_{out}/v_{in}$. Need a numerical number as an answer.

h) Under the constrain that the DC output voltage V_{OUT} must equal $2.5\,V$, you perhaps wonder if the voltage gain A_V could have been made significantly larger by choosing a different DC value of I_C than the 1 mA value picked in part (b). Of course, then the resistors R and R_1 would also need to change accordingly. Can you pick values for I_C, R and R_1 that let you obtain a much larger value for the voltage gain A_V than that obtained in part (g)?

Problem 10.2: (Frequency performance of a cascode amplifier vs a common source amplifier)

Consider the following cascode amplifier:



$W = 10\ \mu\text{m}$
$L = 0.5\ \mu\text{m}$
$\mu_n C_{ox} = 200\ \mu A/V^2$
$\lambda_n = 0.02\ 1/V$
$V_{DD} = 3.0\ V$
$V_{TN} = 0.5\ V$

$I_{BIAS} = 4\ mA$
$C_{gd} = 10\ fF$
$C_{gs} = \frac{2}{3} C_{ox} WL = 30\ fF$
$r_{oc} \approx r_{o2} = r_{o1}$

Assume that V_{BIAS1} and V_{BIAS2} have been adjusted such that the drain current of the both the FETs is 4 mA. Suppose $R_S = 2\text{k}\Omega$.

Synopsis: A good voltage amplifiers needs to have a large input resistance, a small output resistance, a large gain, and a large gain bandwidth (i.e. the bandwidth over which the gain is flat and at the DC value is large). A common source amplifier has a large gain and a large input resistance, but suffers from the Miller effect which compromises the gain bandwidth. A common gate amplifier has a large gain, and a large gain bandwidth, but has a small input resistance. A casacade of the two, i.e. a cascode, has a large input resistance, a large gain, and a large gain bandwidth. These characteristics make the cascode an attractive stage for circuit designers. In this problem you will explore this in detail.

a) Draw the small signal model of the cascode shown above.

b) At the bias point, find the (numerical) values of g_m and g_o for both the FETs (these should be identical for the two FETs since they are both biased with the same DC current). How big is g_m compared to g_o?

c) Using KCL at the drain end of M2 in the small signal model, show that:

$$\frac{v_{out}}{v_a} \approx \frac{g_{m2}(r_{oc} \,||\, r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \,||\, r_{o2})}$$

The above expression is the open circuit voltage gain of the second common gate stage. At low frequencies (~DC), the above expression gives the familiar near-DC open circuit voltage gain of a common gate amplifier: $g_{m2}(r_{oc} \,||\, r_{o2})$.

d) Plot $10\log_{10}\left|\frac{v_{out}}{v_a}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency in Hz (not rad/s). The matlab function "logspace" will be useful when making the frequency array for plotting.

e) Using KCL at the drain end of M1 in the small signal model, show that:

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + g_{o2} + g_{m2} + j\omega(C_{gd1} + C_{gs2}) - g_{o2}\left[\frac{g_{m2}(r_{oc} \,||\, r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \,||\, r_{o2})}\right]}$$

If the input impedance looking into M2 from the source end were assumed to be infinite, the above expression would reduce to,

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + j\omega(C_{gd1})}$$

which is the just the open circuit voltage gain of a common source amplifier with a low frequency value equal to $-g_{m1}r_{o1}$. However, the input impedance of the common gate amplifier is not infinite and is in fact very small. After making suitable approximations, the above expression simplifies to,

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{m2} + j\omega(C_{gd1} + C_{gs2}) - g_{o2}\left[\dfrac{g_{m2}(r_{oc} \,||\, r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \,||\, r_{o2})}\right]}$$

The near-DC value of the above expression is,

$$\frac{v_a}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}}\left(1 + \frac{r_{oc}}{r_{o2}}\right) = A_{v1}\frac{R_{in2}}{R_{out1} + R_{in2}}$$

$$\left\{ A_{v1} = -g_{m1}r_{o1} \quad R_{out1} = r_{o1} \quad R_{in2} \approx \frac{1}{g_{m2}}\left(1 + \frac{r_{oc}}{r_{o2}}\right)\right.$$

v_a/v_{in} at near-DC is of the order of unity. What the above analysis shows is that the first stage, the common source stage, does not really provide much gain at all. All the gain comes from the second stage, the common gate stage. The first stage does not provide much gain because it is loaded with the small input resistance of the second stage. And so the loaded voltage gain of the first stage (not the open circuit voltage gain) is pretty small, near unity! Now here comes the punch line: *since the first common source stage does not really provide much gain, the Miller effect does not make the gate-to-drain capacitance of the first stage look terribly big and therefore the Miller effect does not destroy the high frequency performance of the first common source stage!*

f) Plot $10\log_{10}\left|\frac{v_a}{v_{in}}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

g) Do a KCL at the gate of M1, used previously obtained results, and show that,

$$\frac{v_{in}}{v_s} \approx \frac{1}{1 + j\omega(C_{gs1} + C_{gd1})R_s - j\omega C_{gd1}R_s\left[\dfrac{-g_{m1} + j\omega C_{gd1}}{g_{m2} + j\omega(C_{gd1} + C_{gs2}) - g_{o2}\left[\dfrac{g_{m2}(r_{oc} \,||\, r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \,||\, r_{o2})}\right]}\right]}$$

h) Plot $10\log_{10}\left|\frac{v_{in}}{v_s}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

i) Based on the results in part (d) and (f) and (h), which stage, first or second or the input part, limits the overall frequency bandwidth of the amplifier?

j) Now using your results from parts (c), (e), amd (g), Plot $10\log_{10}\left|\frac{v_{out}}{v_s}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

k) If you now just consider a simple common source amplifier (assume that the FET M2 is replaced by a wire) then from the lecture notes (without making approximations):

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + g_{oc} + j\omega(C_{gd1})}$$

$$\frac{v_{in}}{v_s} \approx \frac{1}{1 + j\omega(C_{gs1} + C_{gd1})R_s - j\omega C_{gd1}R_s\left[\frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + g_{oc} + j\omega(C_{gd1})}\right]}$$

Plot $10\log_{10}\left|\frac{v_a}{v_s}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency. Compare the plot to your answer in part (j) for the cascode amplifier. You should see that the cascode does better in terms of the frequency bandwidth while providing at the same time few dB larger near-DC gain.

l) There is still a problem with using the cascode as a voltage amplifier; it has a large output resistance. This can be fixed by using a common drain stage as the final output stage. Do you think that adding a common drain stage would significantly spoil the frequency performance of the overall amplifier? Why or why not? Does a common drain stage suffer from the Miller effect?