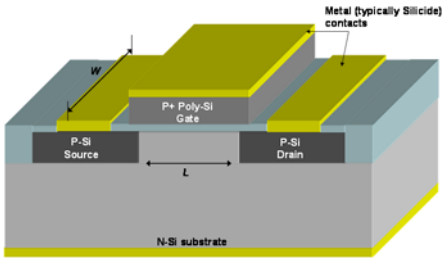
Lecture 9

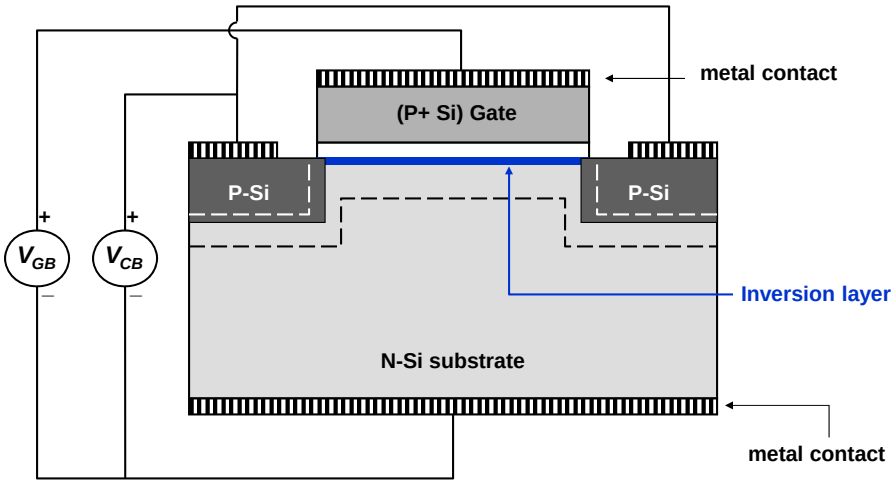
PMOS Field Effect Transistor (PMOSFET or PFET)

In this lecture you will learn:

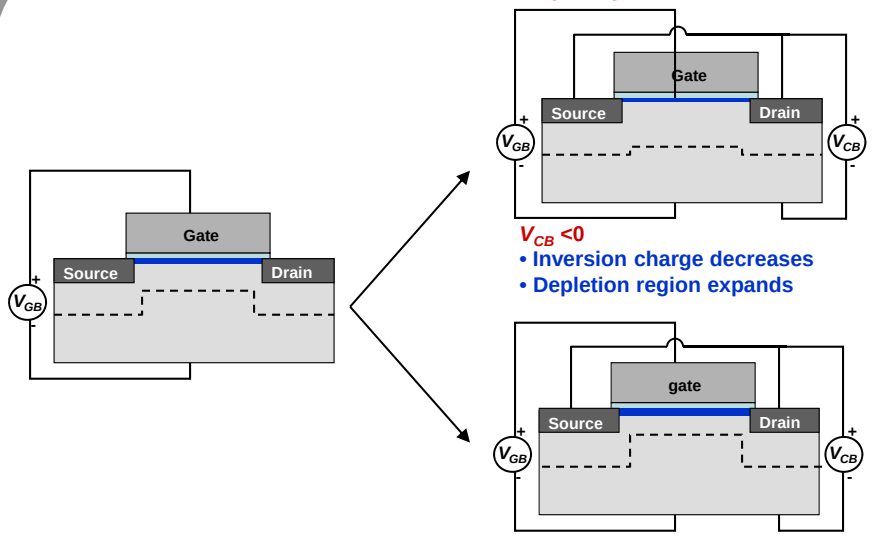
- **The operation and working of the PMOS transistor**



A PMOS Capacitor with a Channel Contact



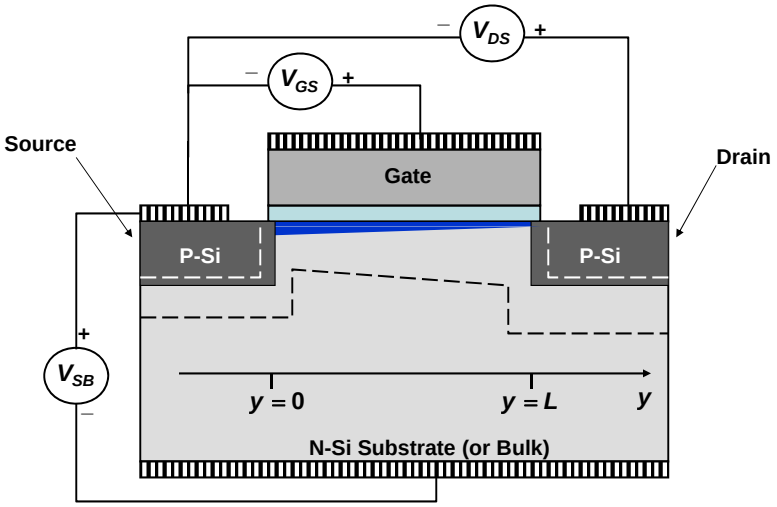
PMOS Capacitor: Effect of V_{CB} ($V_{GB} < V_{TP}$)



V_{CB} <0
- Inversion charge decreases
- Depletion region expands

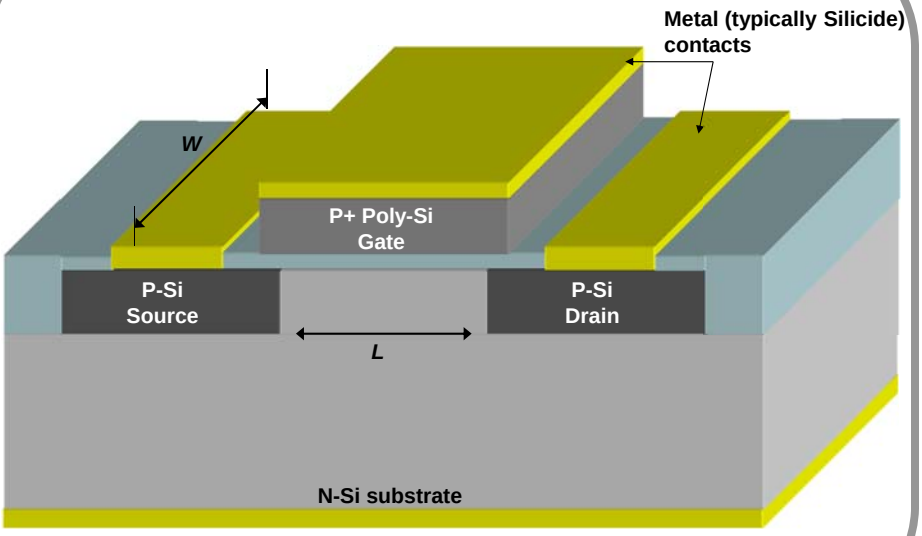
V_{CB} >0
- Inversion charge increases
- Depletion region shrinks

A PMOS Transistor

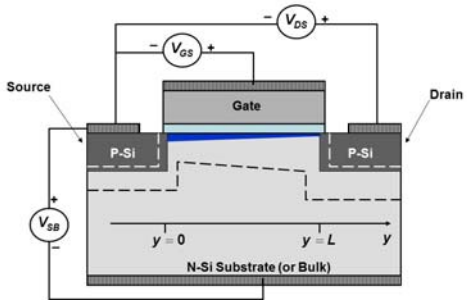


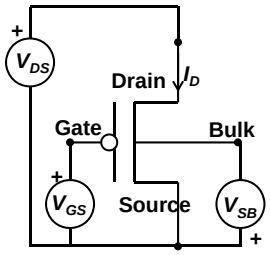
Basic Idea: Current can be made to flow in the inversion layer by applying a voltage across it in the horizontal direction

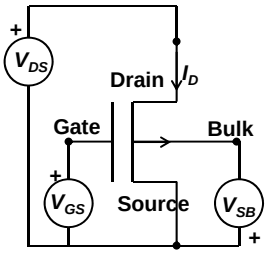
A PMOS Transistor in 3D

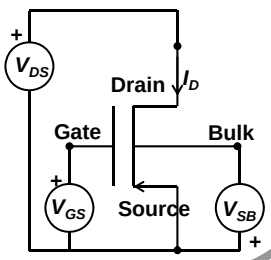


A PMOS Transistor: Circuit Symbols









MOS Transistor: The Gradual Channel Approximation

• The operation of the MOS transistor is best understood under the "gradual channel approximation" which assumes that:

"Electrostatics of the MOS transistor in the horizontal direction have nothing to do with the electrostatics in the vertical direction"

• This assumption decouples the 2-dimensional complicated problem into two 1-dimensional simpler problems – one for the vertical direction and one for the horizontal direction.

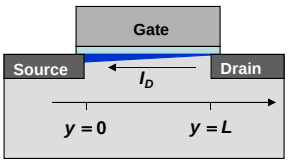
• The electrostatics in the vertical direction have already been worked out by us in the context of the MOS capacitor

• In this lecture we will work out the electrostatics in the horizontal direction and calculate the current flow

PMOS Transistor: Current Flow

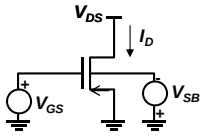
Current in the inversion channel at the location *y* is:

$$I_D = -W\,Q_P(y)\,v_y(y)$$



$Q_P(y)$ = Inversion layer charge (C/cm²)

$v_y(y)$ = Drift velocity of inversion layer charge (cm/s)



Drift velocity of holes is:

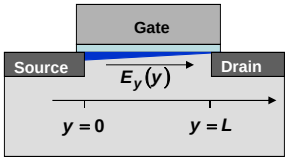
$$v_y(y) = \mu_p E_y(y)$$

$E_y(y)$ = Horizontal component of the electric field (V/cm)

Note: positive direction of current is when the current flows from the drain to the source

Therefore:

$$I_D = -W\,Q_P(y)\,\mu_p E_y(y)$$



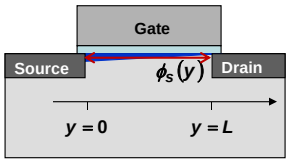
PMOS Transistor: Current Flow

Let the potential in the channel from the source to the drain end be written as:

$$\phi_s(y) = -\phi_n + V_{CB}(y)$$

At the source end: $V_{CB}(y=0) = V_{SB}$

At the drain end: $V_{CB}(y=L) = V_{DB} = V_{DS} + V_{SB}$

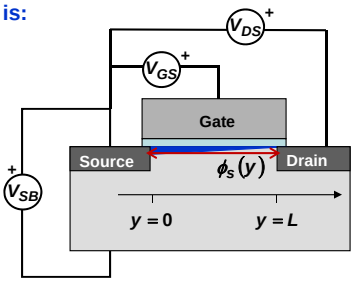


Then the horizontal electric field in the channel is:

$$E_y(y) = -\frac{d\phi_s(y)}{dy} = -\frac{dV_{CB}(y)}{dy}$$

Therefore:

$$I_D = W\, Q_P(y)\, \mu_p \frac{dV_{CB}(y)}{dy}$$



PMOS Transistor: Inversion Charge

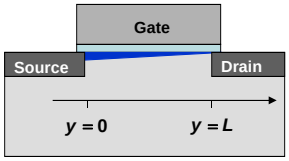
The inversion charge in the channel is:

$$Q_P(y) = \begin{cases} 0 & \text{For } V_{GB} > V_{TP}(y) \\ -C_{ox}\left(V_{GB} - V_{TP}(y)\right) & \text{For } V_{GB} \le V_{TP}(y) \end{cases}$$

Where the position dependent threshold voltage is:

$$V_{TP}(y) = V_{FB} - 2\phi_n + V_{CB}(y) - \frac{\sqrt{2\,\varepsilon_s q N_d \left(2\phi_n - V_{CB}(y)\right)}}{C_{ox}}$$

The channel potential is "*y*" dependent, and therefore the threshold voltage is also "*y*" dependent. Consequently, the inversion charge is also "*y*" dependent



PMOS Transistor: Inversion Charge and FET Threshold Voltage

So:

$$Q_P(y) = -C_{ox}\left(V_{GB} - V_{TP}(y)\right)$$

$$= -C_{ox}\left(V_{GB} - V_{FB} + 2\phi_n - V_{CB}(y) + \frac{\sqrt{2\varepsilon_s q N_d\left(2\phi_n - V_{CB}(y)\right)}}{C_{ox}}\right)$$

use: $V_{GB} = V_{GS} + V_{SB}$ and: $V_{CB}(y) = V_{CS}(y) + V_{SB}$

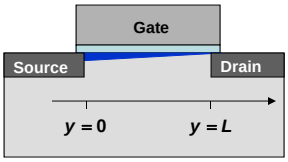
$$= -C_{ox}\left(V_{GS} - V_{FB} + 2\phi_n - V_{CS}(y) + \frac{\sqrt{2\varepsilon_s q N_d\left(2\phi_n - V_{CS}(y) - V_{SB}\right)}}{C_{ox}}\right)$$

$$Q_P(y) \approx -C_{ox}\left(V_{GS} - V_{FB} + 2\phi_n - V_{CS}(y) + \frac{\sqrt{2\varepsilon_s q N_d\left(2\phi_n - V_{SB}\right)}}{C_{ox}}\right)$$

$$Q_P(y) = -C_{ox}\left(V_{GS} - V_{TP} - V_{CS}(y)\right)$$

The PMOS transistor threshold voltage is defined as:

$$V_{TP} = V_{FB} - 2\phi_n - \frac{\sqrt{2\,\varepsilon_s q N_d\left(2\phi_n - V_{SB}\right)}}{C_{ox}}$$



PMOS Transistor: Inversion Charge

The inversion charge in the channel is:

$$Q_P(y) = -C_{ox}\left(V_{GS} - V_{TP} - V_{CS}(y)\right)$$

Near the source end:

$$V_{CS}(y = 0) = 0$$

and

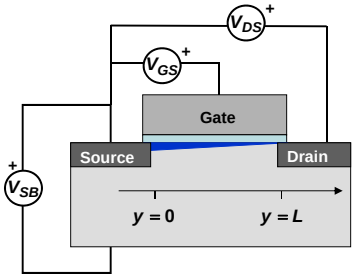
$$Q_P(y = 0) = -C_{ox}\left(V_{GS} - V_{TP}\right)$$

Near the drain end:

$$V_{CS}(y = L) = V_{DS}$$

and

$$Q_P(y = 0) = -C_{ox}\left(V_{GS} - V_{TP} - V_{DS}\right)$$



Conclusion:

Inversion layer charge is maximum near the source end and minimum near the drain end (as shown graphically in the figure)

PMOS Transistor: Current Flow

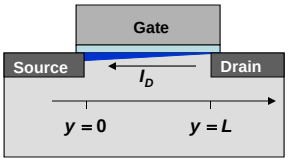
Current in the inversion channel at the location y is:

$$I_D = -W\, Q_P(y)\, \mu_p\, E(y)$$

$$= W\, Q_P(y)\, \mu_p\, \frac{dV_{CS}(y)}{dy}$$

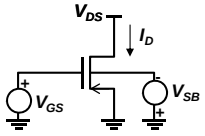
$$I_D = -W\, \mu_p\, C_{ox}\left(V_{GS} - V_{TP} - V_{CS}(y)\right)\frac{dV_{CS}(y)}{dy}$$

$$E(y) = -\frac{dV_{CB}(y)}{dy} = -\frac{dV_{CS}(y)}{dy}$$



Integrate the above equation from y=0 to y=L:

$$\int_0^L I_D\, dy = -\int_0^{V_{DS}} W\, \mu_p\, C_{ox}\left(V_{GS} - V_{TP} - V_{CS}\right) dV_{CS}$$



And the result is:

$$I_D = -\frac{W}{L}\mu_p\, C_{ox}\left[V_{GS} - V_{TP} - \frac{V_{DS}}{2}\right]V_{DS}$$

Some interpretation is required to understand the range of validity of the above equation. This we do next ……..

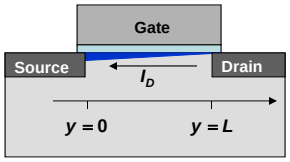
PMOS Transistor: Current Flow

First note that:

when $V_{DS} = 0$

then $I_D = 0$

There can be no current when there is no bias and no electric field in the channel to drive the current

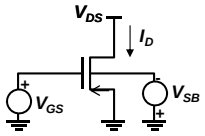


Also note that:

The inversion layer charge is maximum at the source end and is given by:

$$Q_P(y = 0) = -C_{ox}\left(V_{GS} - V_{TP} - V_{CS}(y = 0)\right)$$

$$= -C_{ox}\left(V_{GS} - V_{TP}\right)$$



When $V_{GS} \geq V_{TP}$ there is no inversion charge anywhere in the channel and therefore $I_D = 0$

Conclusion:

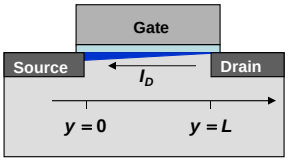
$I_D \neq 0$ only when:

$V_{GS} < V_{TP}$ AND $V_{DS} \neq 0$

PMOS Transistor: Current Flow

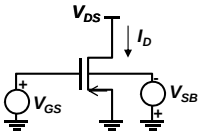
Suppose now:

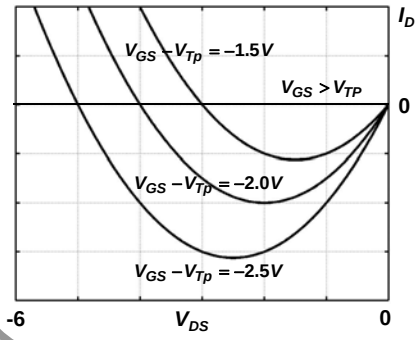
$$V_{GS} < V_{TP} \quad \text{and} \quad V_{DS} < 0$$



First plot the I_D-V_{DS} curve from the result:

$$I_D = -\frac{W}{L}\mu_p C_{ox}\left[V_{GS} - V_{TP} - \frac{V_{DS}}{2}\right]V_{DS}$$





As V_{DS} is decreased the current magnitude increases
…… but then it decreases !?

This decrease is unphysical !
A mathematical artifact !

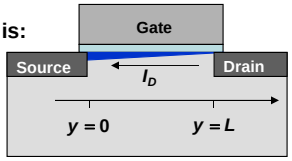
Note that current magnitude is maximum when:

$$V_{DS} = V_{GS} - V_{TP}$$

PMOS Transistor: Pinch-Off

The inversion charge in the channel near the drain end is:

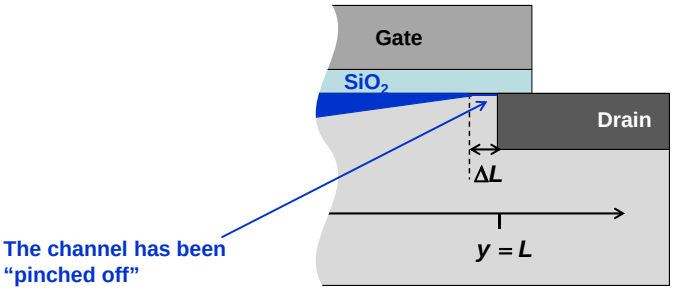
$$Q_P(y = L) = -C_{ox}(V_{GS} - V_{TP} - V_{CS}(y = L))$$
$$= -C_{ox}(V_{GS} - V_{TP} - V_{DS})$$



When V_{DS} approaches V_{GS} - V_{TP} the inversion layer charge just near the drain end approaches zero

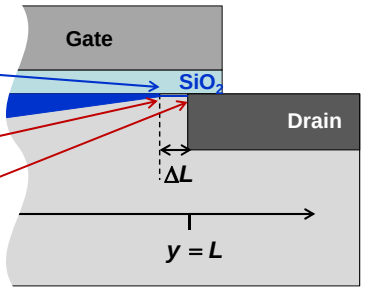
This condition is called "pinch-off"

For $V_{DS} < V_{GS}$ - V_{TP} there is a small section of channel just near the drain end that is almost devoid of mobile carriers (i.e. holes). This is a highly resistive section.



PMOS Transistor: Pinch-Off and Current Saturation

The channel has been "pinched off"



For $V_{DS} \le V_{GS} - V_{TP}$:

Channel potential: $V_{CS}(y) = V_{GS} - V_{TP}$

Channel potential: $V_{CS}(y) = V_{DS}$

Any decrease in V_{DS} below V_{GS} - V_{TP} completely falls across this small resistive section

For $V_{DS} < V_{GS} - V_{TP}$, integrate the current equation from y=0 to y=L-ΔL:

$$\int_0^{L-\Delta L} I_D \, dy = -\int_0^{V_{GS}-V_{TP}} W \mu_p C_{ox} (V_{GS} - V_{TP} - V_{CS}) \, dV_{CS}$$

$$\Rightarrow I_D = -\frac{W}{2(L-\Delta L)} \mu_p C_{ox} (V_{GS} - V_{TP})^2 \approx -\frac{W}{2L} \mu_p C_{ox} (V_{GS} - V_{TP})^2$$

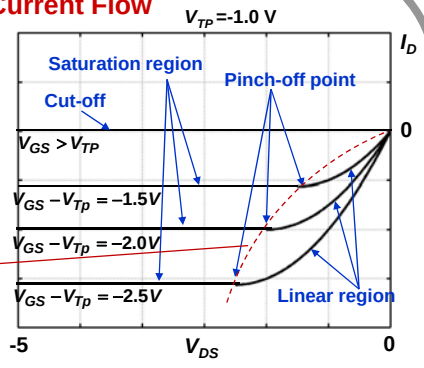
So for $V_{DS} < V_{GS} - V_{TP}$ the current is what it was when V_{DS} was equal to $V_{GS} - V_{TP}$

Thus for large negative values of V_{DS} ($< V_{GS} - V_{TN}$) the current saturates!

PMOS Transistor: Current Flow

The I_D - V_{DS} curves for an PMOS looks like as shown in the figure

The three curves are for different values of V_{GS} - V_{TP}

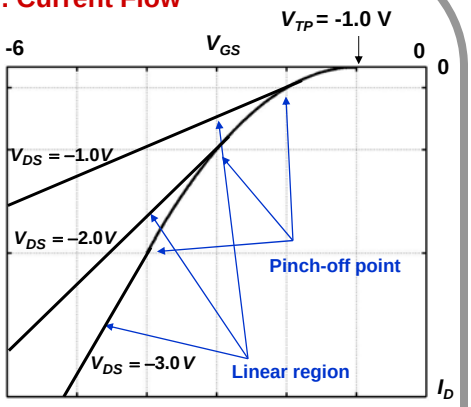


$$I_D = \begin{cases} 0 & \text{For } V_{GS} > V_{TP} \quad \text{(Cut-off region)} \\ -\frac{W}{L} \mu_p C_{ox} \left[V_{GS} - V_{TP} - \frac{V_{DS}}{2} \right] V_{DS} & \text{For } 0 \ge V_{DS} \ge V_{GS} - V_{TP} \quad \text{(Linear region)} \\ -\frac{W}{2L} \mu_p C_{ox} (V_{GS} - V_{TP})^2 & \text{For } 0 \ge V_{GS} - V_{TP} \ge V_{DS} \quad \text{(Saturation region)} \end{cases}$$

PMOS Transistor: Current Flow

I_D - V_{GS} curves for an PMOS are shown in the figure →

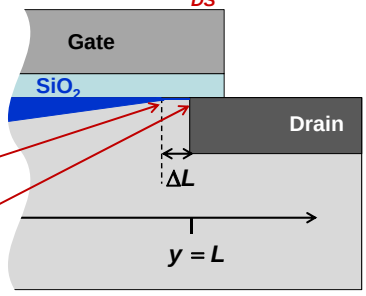
The three curves are for different values of V_{DS}



$$I_D = \begin{cases} 0 & \text{For } V_{GS} > V_{TP} \quad \text{(Cut-off region)} \\ -\frac{W}{L}\mu_p C_{ox}\left[V_{GS} - V_{TP} - \frac{V_{DS}}{2}\right]V_{DS} & \text{For } 0 \geq V_{DS} \geq V_{GS} - V_{TP} \quad \text{(Linear region)} \\ -\frac{W}{2L}\mu_p C_{ox}\left(V_{GS} - V_{TP}\right)^2 & \text{For } 0 \geq V_{GS} - V_{TP} \geq V_{DS} \quad \text{(Saturation region)} \end{cases}$$

PMOS Transistor: Saturation Current vs V_{DS}

For $V_{DS} < V_{GS} - V_{TP}$ (in the saturation region) there is a small section of the channel just near the drain end that is almost devoid of mobile carriers (i.e. holes).



Channel potential: $V_{CS}(y) = V_{GS} - V_{TP}$

Channel potential: $V_{CS}(y) = V_{DS}$

In saturation, for $V_{DS} < V_{GS} - V_{TP}$, integrate the current equation from y=0 to y=L-ΔL:

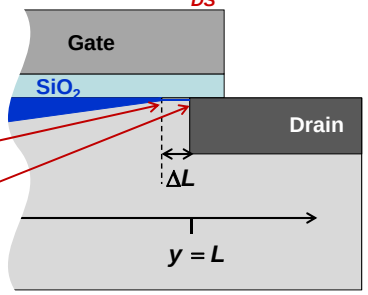
$$\int_0^{L-\Delta L} I_D\, dy = -\int_0^{V_{GS}-V_{TP}} W\,\mu_p C_{ox}\left(V_{GS} - V_{TP} - V_{CS}\right) dV_{CS}$$

$$\Rightarrow I_D = -\frac{W}{2(L-\Delta L)}\mu_p C_{ox}\left(V_{GS} - V_{TP}\right)^2 \approx -\frac{W}{2L\left(1-\frac{\Delta L}{L}\right)}\mu_p C_{ox}\left(V_{GS} - V_{TP}\right)^2$$

$$\approx -\frac{W}{2L}\mu_p C_{ox}\left(V_{GS} - V_{TP}\right)^2\left(1+\frac{\Delta L}{L}\right)$$

PMOS Transistor: Saturation Current vs V_{DS}

For $V_{DS} < V_{GS} - V_{TP}$ (in the saturation region) there is a small section of the channel just near the drain end that is almost devoid of mobile carriers (i.e. electrons).



Channel potential: $V_{CS}(y) = V_{GS} - V_{TP}$

Channel potential: $V_{CS}(y) = V_{DS}$

To a very good approximation:

$$\frac{\Delta L}{L} \propto -V_{DS}$$

$$\Rightarrow \frac{\Delta L}{L} \approx -\lambda_p V_{DS}$$

Channel length modulation

$$\lambda_p \approx \frac{10^{-7}}{L(\text{in meters})}\ 1/V \approx \frac{0.1}{L(\text{in } \mu\text{m})}\ 1/V$$

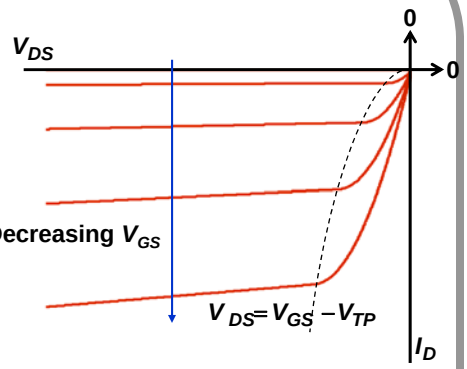
So for $0 \geq V_{GS} - V_{TP} \geq V_{DS}$ (saturation region):

$$I_D \approx -\frac{W}{2L}\mu_p C_{ox}(V_{GS} - V_{TP})^2(1 - \lambda_p V_{DS})$$

PMOS Transistor: Saturation Current vs V_{DS}

For $0 \geq V_{GS} - V_{TP} \geq V_{DS}$
(In saturation region):

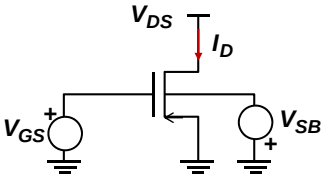
$$I_D \approx -\frac{W}{2L}\mu_p C_{ox}(V_{GS} - V_{TP})^2(1 - \lambda_p V_{DS})$$

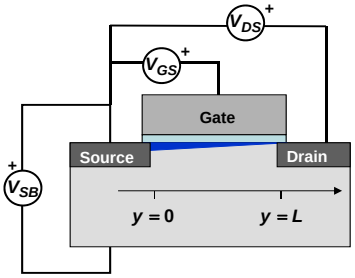


A better PFET current model is:

$$I_D = \begin{cases} 0 & \text{For } V_{GS} > V_{TP} \text{ (Cut-off region)} \\ -\frac{W}{L}\mu_p C_{ox}\left[V_{GS} - V_{TP} - \frac{V_{DS}}{2}\right]V_{DS}(1 - \lambda_p V_{DS}) & \text{For } 0 \geq V_{DS} \geq V_{GS} - V_{TP} \text{ (Linear region)} \\ -\frac{W}{2L}\mu_p C_{ox}(V_{GS} - V_{TP})^2(1 - \lambda_p V_{DS}) & \text{For } 0 \geq V_{GS} - V_{TP} \geq V_{DS} \text{ (Saturation region)} \end{cases}$$

PMOS Transistor: Backgate Effect or the Body Effect





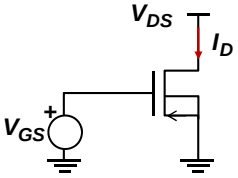
The PMOS transistor threshold voltage depends on the applied source to bulk potential difference:

$$V_{TP} = V_{FB} - 2\phi_n - \frac{\sqrt{2\,\varepsilon_s q N_d (2\phi_n - V_{SB})}}{C_{ox}}$$

$$\Rightarrow V_{TP} = V_{TP}(V_{SB} = 0) - \gamma_p\left(\sqrt{2\phi_n - V_{SB}} - \sqrt{2\phi_n}\right)$$

$$\gamma_p = \frac{\sqrt{2\,\varepsilon_s q N_d}}{C_{ox}}$$ = Backgate effect parameter

PMOS Transistor: Backgate Effect or the Body Effect



To get rid of the body effect, one can short the bulk (or the backgate) to the source such that V_{SB} =0

$$V_{TP} = V_{TP}(V_{SB} = 0) - \gamma_p\left(\sqrt{2\phi_n - V_{SB}} - \sqrt{2\phi_n}\right)$$ (0)

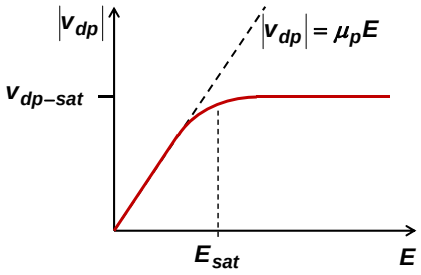
However, depending on the technology used, this may not always be possible……..

PMOS Transistor: Velocity Saturation

The drift velocity vs field curve for almost all materials is not linear and therefore

$$v_{dp} = \mu_p E$$

does not really hold



Drift velocity saturates at high fields!

A better approximation is:

$$v_{dp} = \frac{\mu_p E}{1 + \frac{|E|}{E_{sat}}}$$

In Silicon: $E_{sat} \sim 5 \times 10^4$ V/cm

Current in the inversion channel at the location y is:

$$I_D = -W\, Q_P(y) \frac{\mu_p\, E(y)}{1 + \frac{|E|}{E_{sat}}} = -W\, C_{ox} (V_{GS} - V_{TP} - V_{CS}) \frac{\mu_p \frac{dV_{CS}(y)}{dy}}{1 + \frac{1}{E_{sat}} \left| \frac{dV_{CS}(y)}{dy} \right|}$$

PMOS Transistor: Velocity Saturation

Current in the inversion channel at the location y is:

$$I_D = -W\, Q_P(y) \frac{\mu_p\, E(y)}{1 + \frac{|E|}{E_{sat}}} = -W\, C_{ox} (V_{GS} - V_{TP} - V_{CS}) \frac{\mu_p \frac{dV_{CS}(y)}{dy}}{1 + \frac{1}{E_{sat}} \left| \frac{dV_{CS}(y)}{dy} \right|}$$

Integrate the above equation from $y=0$ to $y=L$:

$$\int_0^L I_D \left(1 + \frac{1}{E_{sat}} \left| \frac{dV_{CS}(y)}{dy} \right|\right) dy = -\int_0^{V_{DS}} W\, \mu_p\, C_{ox} (V_{GS} - V_{TP} - V_{CS})\, dV_{CS}$$

Answer is (in linear region):

$$I_D = -\frac{W}{L} \mu_p\, C_{ox} \left(V_{GS} - V_{TP} - \frac{V_{DS}}{2}\right) \frac{V_{DS}}{\left(1 + \frac{|V_{DS}|}{V_{sat}}\right)}$$

$V_{sat} = E_{sat} L$

Answer is (in saturation region):

$$I_D = -\frac{W}{2L} \frac{\mu_p}{\left(1 + \frac{|V_{GS} - V_{TP}|}{V_{sat}}\right)} C_{ox} (V_{GS} - V_{TP})^2$$

→ Velocity saturation decreases the current

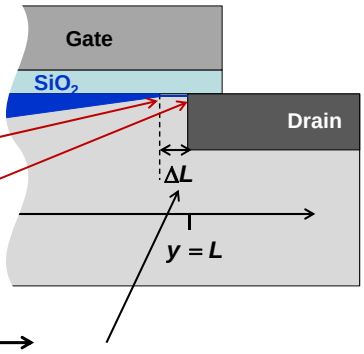
PMOS Transistor: Breakdown

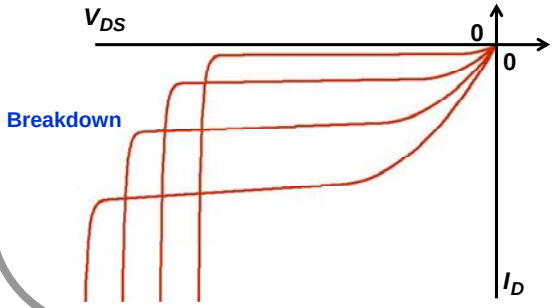
Large fields near the drain end in saturation can lead to breakdown

Breakdown limits the maximum value of V_{DS}

Channel potential: $V_{CS}(y) = V_{GS} - V_{TP}$

Channel potential: $V_{CS}(y) = V_{DS}$





Breakdown

Potential drop in this region:

$$|V_{DS} - (V_{GS} - V_{TN})|$$

Field in this region:

$$\frac{|V_{DS} - (V_{GS} - V_{TN})|}{\Delta L}$$