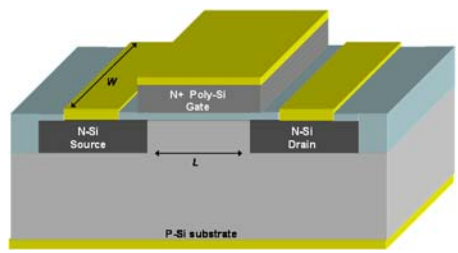
Lecture 9

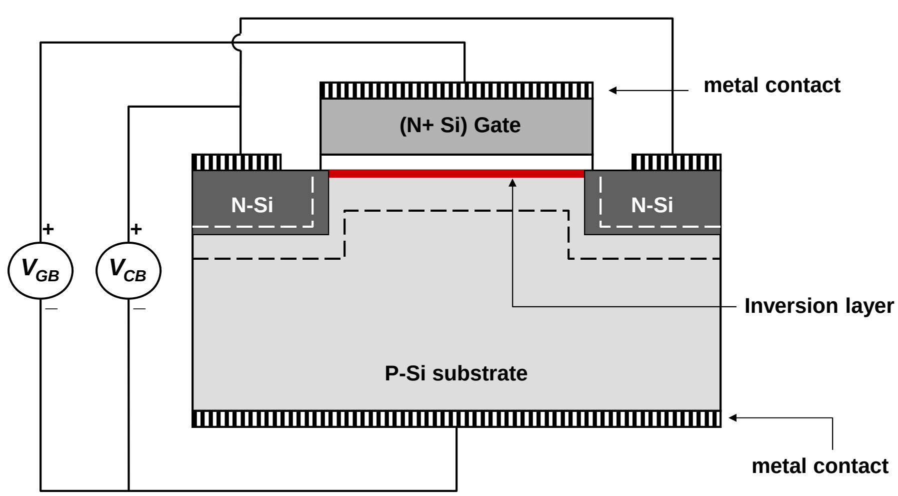
NMOS Field Effect Transistor (NMOSFET or NFET)

In this lecture you will learn:

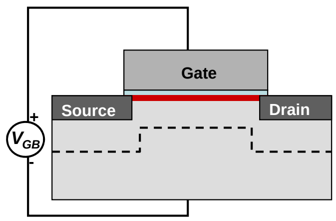
- The operation and working of the NMOS transistor

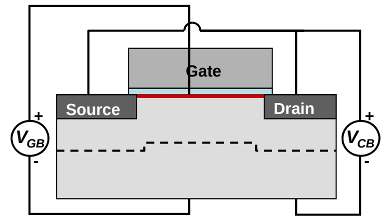


A NMOS Capacitor with a Channel Contact



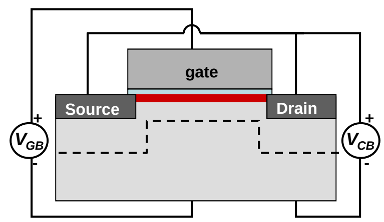
NMOS Capacitor: Effect of V_{CB} ($V_{GB} > V_{TN}$)





$V_{CB} > 0$

- Inversion charge decreases
- Depletion region expands



$V_{CB} < 0$

- Inversion charge increases
- Depletion region shrinks

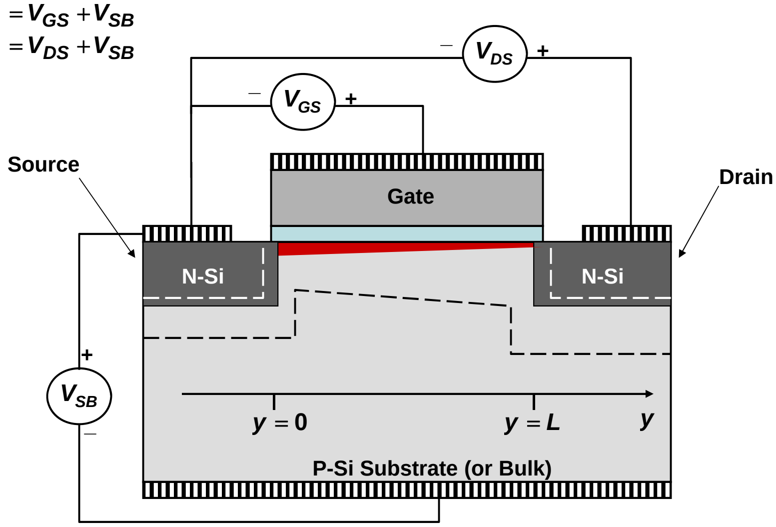
Inversion layer charge:

$$Q_N = -C_{ox}\left(V_{GB} - V_{TN}\right)$$

Depends on V_{CB}

A NMOS Transistor

$$V_{GB} = V_{GS} + V_{SB}$$
$$V_{DB} = V_{DS} + V_{SB}$$



Basic Idea: Current can be made to flow in the inversion layer by applying a voltage across it in the horizontal direction

A Note on Voltage Symbols

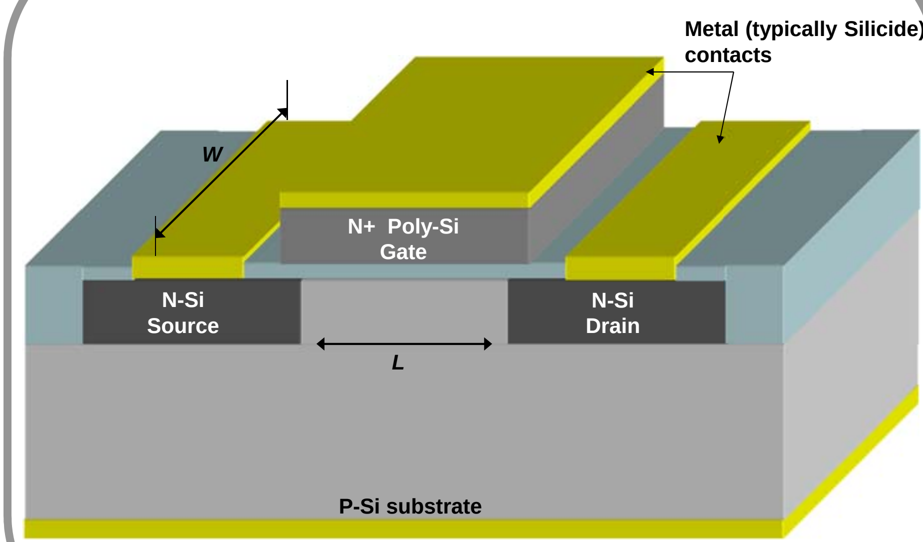
$$V_{CB} = V_C - V_B = -(V_B - V_C) = - V_{BC}$$

$$V_{GS} = V_G - V_S$$

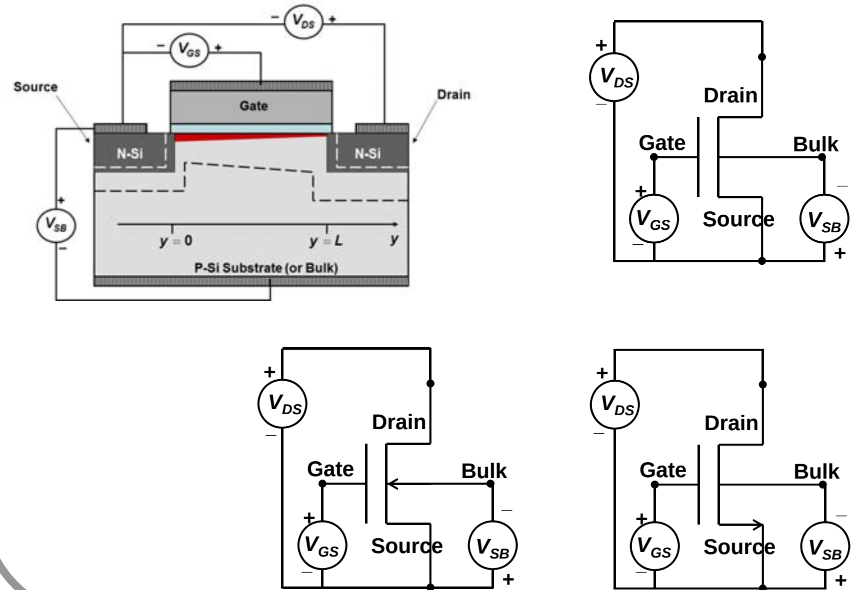
$$= V_G - V_B + V_B - V_S$$

$$= V_{GB} - V_{SB}$$

A NMOS Transistor in 3D



A NMOS Transistor: Circuit Symbols



MOS Transistor: The Gradual Channel Approximation

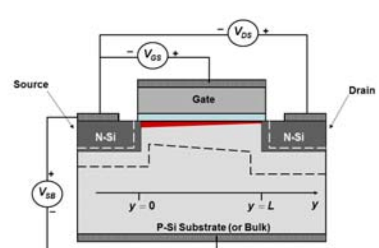
• The operation of the MOS transistor is best understood under the "gradual channel approximation" which assumes that:

"Electrostatics of the MOS transistor in the horizontal direction have nothing to do with the electrostatics in the vertical direction"

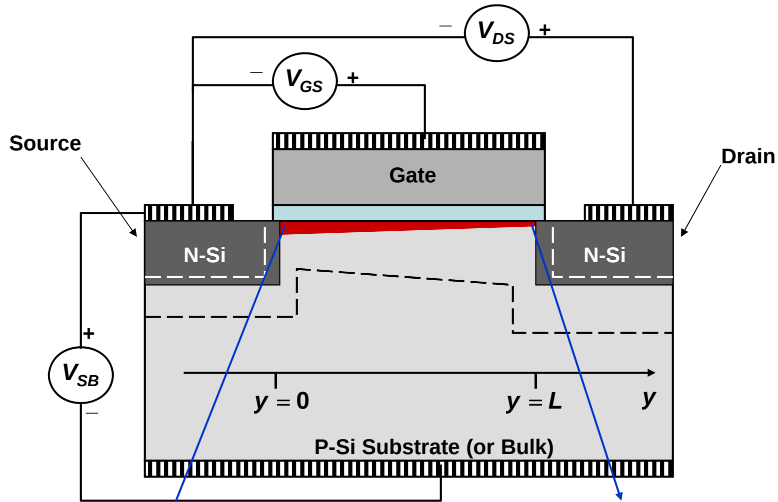
• This assumption decouples the 2-dimensional complicated problem into two 1-dimensional simpler problems – one for the vertical direction and one for the horizontal direction.

• The electrostatics in the vertical direction have already been worked out by us in the context of the MOS capacitor

• In this lecture we will work out the electrostatics in the horizontal direction and calculate the current flow



A NMOS Transistor: Channel Potentials

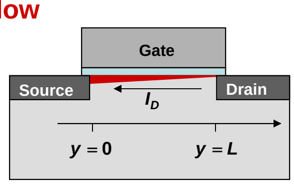


$$\phi_s(y=0) = -\phi_p + V_{CB}(y=0)$$
$$= -\phi_p + V_{SB}$$

$$\phi_s(y=L) = -\phi_p + V_{CB}(y=L)$$
$$= -\phi_p + V_{DB} = -\phi_p + V_{DS} + V_{SB}$$

Potential drop in the channel: $\phi_s(y=L) - \phi_s(y=0) = V_{DS}$

NMOS Transistor: Current Flow

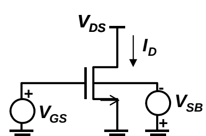


Current in the inversion channel at the location y is:

$$I_D = -W\,Q_N(y)\,v_y(y)$$

$Q_N(y) =$ **Inversion layer charge (C/cm²)**

$v_y(y) =$ **Drift velocity of inversion layer charge (cm/s)**



Drift velocity of electrons is:

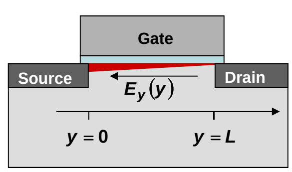
$$v_y(y) = -\mu_n E_y(y)$$

$E_y(y) =$ **Horizontal component of the electric field (V/cm)**

Note: positive direction of current is when the current flows from the drain to the source

Therefore:

$$I_D = W\,Q_N(y)\,\mu_n E_y(y)$$



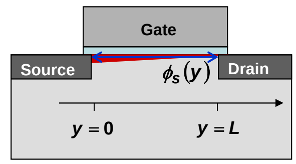
NMOS Transistor: Current Flow

Let the potential in the channel from the source to the drain end be written as:

$$\phi_s(y) = -\phi_p + V_{CB}(y)$$

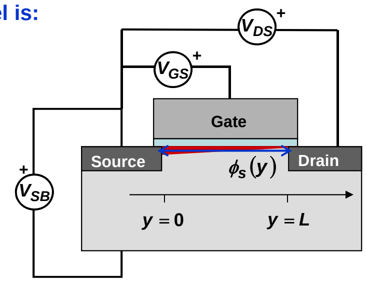
At the source end: $V_{CB}(y = 0) = V_{SB}$

At the drain end: $V_{CB}(y = L) = V_{DB} = V_{DS} + V_{SB}$



Then the horizontal electric field in the channel is:

$$E_y(y) = -\frac{d\phi_s(y)}{dy} = -\frac{d\,V_{CB}(y)}{dy}$$



Therefore:

$$I_D = -W\,Q_N(y)\,\mu_n \frac{dV_{CB}(y)}{dy}$$

NMOS Transistor: Inversion Charge

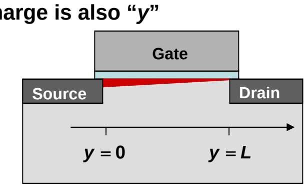
The inversion charge in the channel is:

$$Q_N(y) = \begin{cases} 0 & \text{For } V_{GB} < V_{TN}(y) \\ -C_{ox}\left(V_{GB} - V_{TN}(y)\right) & \text{For } V_{GB} \geq V_{TN}(y) \end{cases}$$

Where the position dependent threshold voltage is:

$$V_{TN}(y) = V_{FB} - 2\phi_p + V_{CB}(y) + \frac{\sqrt{2\,\varepsilon_s q N_a\left(-2\phi_p + V_{CB}(y)\right)}}{C_{ox}}$$

The channel potential is "*y*" dependent, and therefore the threshold voltage is also "*y*" dependent. Consequently, the inversion charge is also "*y*" dependent



NMOS Transistor: Inversion Charge and FET Threshold Voltage

So:

$$Q_N(y) = -C_{ox}\left(V_{GB} - V_{TN}(y)\right)$$

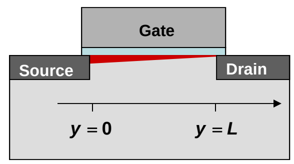
$$= -C_{ox}\left(V_{GB} - V_{FB} + 2\phi_p - V_{CB}(y) - \frac{\sqrt{2\varepsilon_s q N_a\left(-2\phi_p + V_{CB}(y)\right)}}{C_{ox}}\right)$$

use: $V_{GB} = V_{GS} + V_{SB}$ and: $V_{CB}(y) = V_{CS}(y) + V_{SB}$

$$= -C_{ox}\left(V_{GS} - V_{FB} + 2\phi_p - V_{CS}(y) - \frac{\sqrt{2\varepsilon_s q N_a\left(-2\phi_p + V_{CS}(y) + V_{SB}\right)}}{C_{ox}}\right)$$

$$Q_N(y) \approx -C_{ox}\left(V_{GS} - V_{FB} + 2\phi_p - V_{CS}(y) - \frac{\sqrt{2\varepsilon_s q N_a\left(-2\phi_p + V_{SB}\right)}}{C_{ox}}\right)$$

$$Q_N(y) = -C_{ox}\left(V_{GS} - V_{TN} - V_{CS}(y)\right)$$



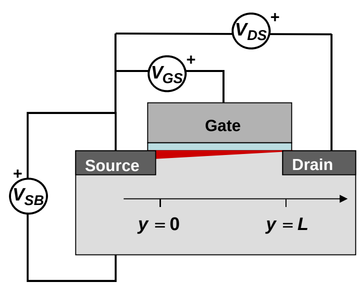
The NMOS transistor threshold voltage is defined as:

$$V_{TN} = V_{FB} - 2\phi_p + \frac{\sqrt{2\,\varepsilon_s q N_a\left(-2\phi_p + V_{SB}\right)}}{C_{ox}}$$

NMOS Transistor: Inversion Charge

The inversion charge in the channel is:

$$Q_N(y) = -C_{ox}\left(V_{GS} - V_{TN} - V_{CS}(y)\right)$$



Near the source end:

$$V_{CS}(y=0) = 0$$

and

$$Q_N(y=0) = -C_{ox}\left(V_{GS} - V_{TN}\right)$$

Near the drain end:

$$V_{CS}(y=L) = V_{DS}$$

and

$$Q_N(y=0) = -C_{ox}\left(V_{GS} - V_{TN} - V_{DS}\right)$$

Conclusion:

Inversion layer charge is maximum near the source end and minimum near the drain end (as shown graphically in the figure)

NMOS Transistor: Current Flow

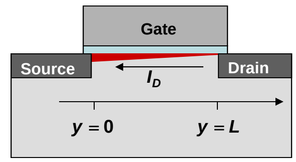
Current in the inversion channel at the location *y* is:

$$I_D = W\, Q_N(y)\, \mu_n\, E(y)$$

$$= -W\, Q_N(y)\, \mu_n \frac{dV_{CS}(y)}{dy}$$

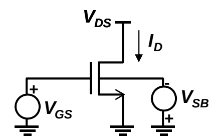
$$E(y) = -\frac{d\,V_{CB}(y)}{dy} = -\frac{d\,V_{CS}(y)}{dy}$$

$$I_D = W\, \mu_n\, C_{ox}\left(V_{GS} - V_{TN} - V_{CS}(y)\right)\frac{dV_{CS}(y)}{dy}$$



Integrate the above equation from *y*=0 to *y*=*L*:

$$\int_0^L I_D\, dy = \int_0^{V_{DS}} W\, \mu_n\, C_{ox}\left(V_{GS} - V_{TN} - V_{CS}\right) dV_{CS}$$

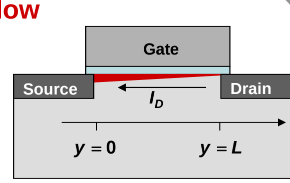


And the result is:

$$I_D = \frac{W}{L}\mu_n\, C_{ox}\left[V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right]V_{DS}$$

Some interpretation is required to understand the range of validity of the above equation. This we do next ……..

NMOS Transistor: Current Flow

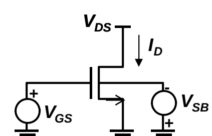


First note that:

when $V_{DS} = 0$

then $I_D = 0$

There can be no current when there is no bias and no electric field in the channel to drive the current



Also note that:

The inversion layer charge is maximum at the source end and is given by:

$$Q_N(y=0) = -C_{ox}\left(V_{GS} - V_{TN} - V_{CS}(y=0)\right)$$
$$= -C_{ox}\left(V_{GS} - V_{TN}\right)$$

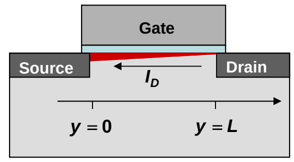
So when $V_{GS} \leq V_{TN}$ there is no inversion charge anywhere in the channel and therefore $I_D = 0$

Conclusion:

$I_D \neq 0$ only when:

$V_{GS} > V_{TN}$ AND $V_{DS} \neq 0$

NMOS Transistor: Current Flow

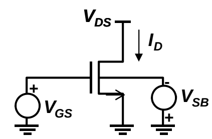


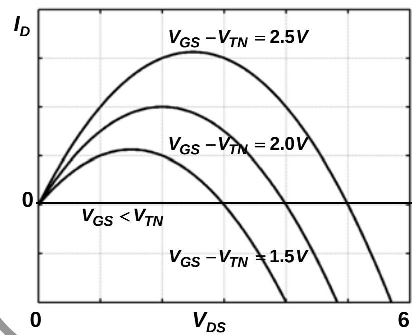
Suppose now:

$$V_{GS} > V_{TN} \quad \text{and} \quad V_{DS} > 0$$

First plot the I_D-V_{DS} curve from the result:

$$I_D = \frac{W}{L} \mu_n C_{ox} \left[V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right] V_{DS}$$





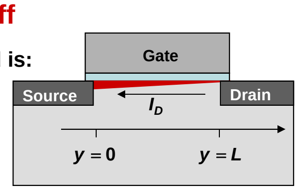
As V_{DS} is increased the current increases ……… but then it decreases !??

This decrease is unphysical !
A mathematical artifact !

Note that current is maximum when:

$$V_{DS} = V_{GS} - V_{TN}$$

NMOS Transistor: Pinch-Off



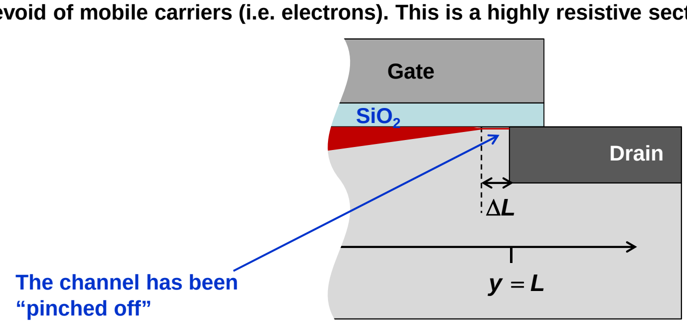
The inversion charge in the channel near the drain end is:

$$\begin{aligned} Q_N(y = L) &= -C_{ox}(V_{GS} - V_{TN} - V_{CS}(y = L)) \\ &= -C_{ox}(V_{GS} - V_{TN} - V_{DS}) \end{aligned}$$

When V_{DS} approaches V_{GS} - V_{TN} the inversion layer charge just near the drain end approaches zero

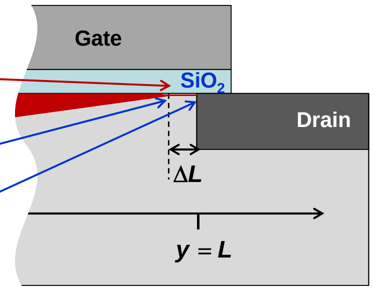
This condition is called “pinch-off”

For V_{DS} > V_{GS} - V_{TN} there is a small section of channel just near the drain end that is almost devoid of mobile carriers (i.e. electrons). This is a highly resistive section.



NMOS Transistor: Pinch-Off and Current Saturation

The channel has been "pinched off"



For $V_{DS} \geq V_{GS} - V_{TN}$:

Channel potential: $V_{CS}(y) = V_{GS} - V_{TN}$

Channel potential: $V_{CS}(y) = V_{DS}$

Any increase in V_{DS} beyond V_{GS} - V_{TN} completely falls across this small resistive section

For V_{DS} > V_{GS} - V_{TN} , integrate the current equation from y=0 to y=L-ΔL:

$$\int_0^{L-\Delta L} I_D \, dy = \int_0^{V_{GS}-V_{TN}} W \mu_n C_{ox} (V_{GS} - V_{TN} - V_{CS}) dV_{CS}$$

$$\Rightarrow I_D = \frac{W}{2(L-\Delta L)} \mu_n C_{ox} (V_{GS} - V_{TN})^2 \approx \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_{TN})^2$$

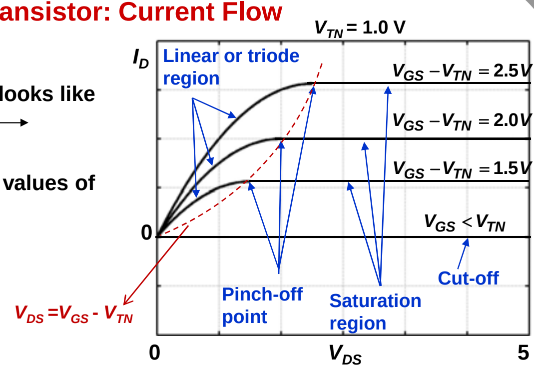
So for V_{DS} > V_{GS} - V_{TN} the current is what it was when V_{DS} was equal to V_{GS} - V_{TN}

Thus for large value of V_{DS} (> V_{GS} – V_{TN}) the current saturates!

NMOS Transistor: Current Flow

The I_D - V_{DS} curves for an NMOS looks like as shown in the figure

The three curves are for different values of V_{GS} - V_{TN}

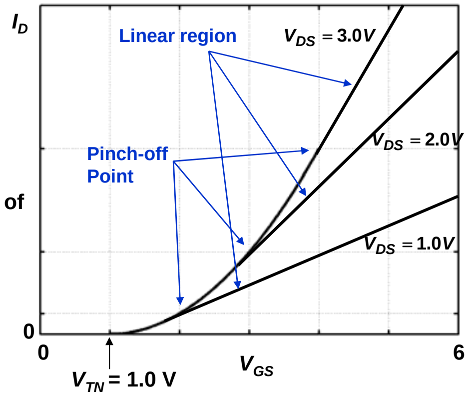


$$I_D = \begin{cases} 0 & \text{For } V_{GS} < V_{TN} \text{ (Cut-off region)} \\ \frac{W}{L} \mu_n C_{ox} \left[V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right] V_{DS} & \text{For } 0 \leq V_{DS} \leq V_{GS} - V_{TN} \text{ (Linear or triode region)} \\ \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_{TN})^2 & \text{For } 0 \leq V_{GS} - V_{TN} \leq V_{DS} \text{ (Saturation region)} \end{cases}$$

NMOS Transistor: Current Flow

I_D - V_{GS} curves for an NMOS are shown in the figure →

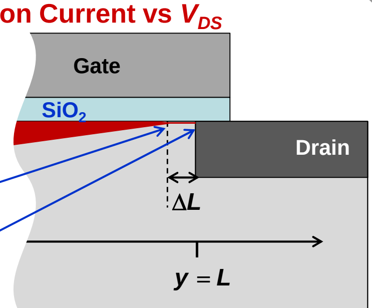
The three curves are for different values of V_{DS}



$$I_D = \begin{cases} 0 & \text{For } V_{GS} < V_{TN} \quad \text{(Cut-off region)} \\ \frac{W}{L}\mu_n C_{ox}\left[V_{GS}-V_{TN}-\frac{V_{DS}}{2}\right]V_{DS} & \text{For } 0 \le V_{DS} \le V_{GS}-V_{TN} \quad \text{(Linear or triode region)} \\ \frac{W}{2L}\mu_n C_{ox}\left(V_{GS}-V_{TN}\right)^2 & \text{For } 0 \le V_{GS}-V_{TN} \le V_{DS} \quad \text{(Saturation region)} \end{cases}$$

NMOS Transistor: Saturation Current vs V_{DS}

For $V_{DS} > V_{GS} - V_{TN}$ (in the saturation region) there is a small section of the channel just near the drain end that is almost devoid of mobile carriers (i.e. electrons).



Channel potential: $V_{CS}(y) = V_{GS} - V_{TN}$

Channel potential: $V_{CS}(y) = V_{DS}$

In saturation, for $V_{DS} > V_{GS} - V_{TN}$, integrate the current equation from y=0 to $y=L-\Delta L$:

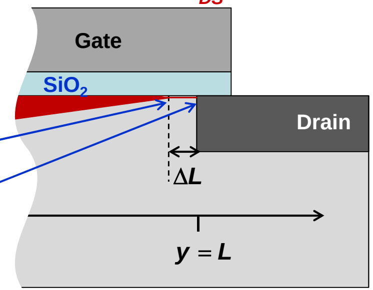
$$\int_0^{L-\Delta L} I_D\, dy = \int_0^{V_{GS}-V_{TN}} W \mu_n C_{ox}\left(V_{GS}-V_{TN}-V_{CS}\right) dV_{CS}$$

$$\Rightarrow I_D = \frac{W}{2(L-\Delta L)}\mu_n C_{ox}\left(V_{GS}-V_{TN}\right)^2 \approx \frac{W}{2L\left(1-\frac{\Delta L}{L}\right)}\mu_n C_{ox}\left(V_{GS}-V_{TN}\right)^2$$

$$\approx \frac{W}{2L}\mu_n C_{ox}\left(V_{GS}-V_{TN}\right)^2\left(1+\frac{\Delta L}{L}\right)$$

NMOS Transistor: Saturation Current vs V_{DS}

For $V_{DS} > V_{GS} - V_{TN}$ (in the saturation region) there is a small section of the channel just near the drain end that is almost devoid of mobile carriers (i.e. electrons).



Channel potential: $V_{CS}(y) = V_{GS} - V_{TN}$

Channel potential: $V_{CS}(y) = V_{DS}$

To a very good approximation:

$$\frac{\Delta L}{L} \propto V_{DS}$$

$$\Rightarrow \frac{\Delta L}{L} \approx \lambda_n V_{DS}$$

$$\lambda_n \approx \frac{10^{-7}}{L(\text{in meters})} \; 1/V \approx \frac{0.1}{L(\text{in } \mu\text{m})} \; 1/V$$

So for $0 \leq V_{GS} - V_{TN} \leq V_{DS}$ (saturation region):

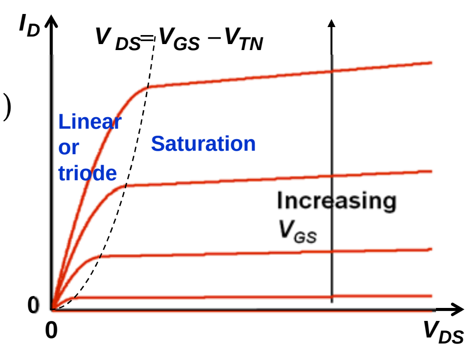
$$I_D \approx \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_{TN})^2 (1 + \lambda_n V_{DS})$$

NMOS Transistor: Saturation Current vs V_{DS}

For $0 \leq V_{GS} - V_{TN} \leq V_{DS}$

(In saturation region):

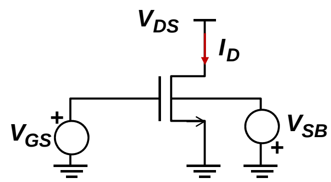
$$I_D \approx \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_{TN})^2 (1 + \lambda_n V_{DS})$$

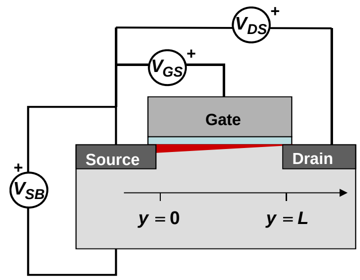


A better NFET current model is:

$$I_D = \begin{cases} 0 & \text{For } V_{GS} < V_{TN} \text{ (Cut-off region)} \\ \frac{W}{L} \mu_n C_{ox} \left[V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right] V_{DS} (1 + \lambda_n V_{DS}) & \text{For } 0 \leq V_{DS} \leq V_{GS} - V_{TN} \text{ (Linear or triode region)} \\ \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_{TN})^2 (1 + \lambda_n V_{DS}) & \text{For } 0 \leq V_{GS} - V_{TN} \leq V_{DS} \text{ (Saturation region)} \end{cases}$$

NMOS Transistor: The Backgate Effect or the Body Effect





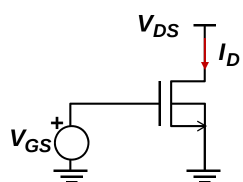
The NMOS transistor threshold voltage depends on the applied source to bulk potential difference:

$$V_{TN} = V_{FB} - 2\phi_p + \frac{\sqrt{2\,\varepsilon_s q N_a \left(-2\phi_p + V_{SB}\right)}}{C_{ox}}$$

$$\Rightarrow V_{TN} = V_{TN}(V_{SB} = 0) + \gamma_n \left(\sqrt{-2\phi_p + V_{SB}} - \sqrt{-2\phi_p}\right)$$

$$\gamma_n = \frac{\sqrt{2\,\varepsilon_s q N_a}}{C_{ox}}$$ = Backgate effect parameter

NMOS Transistor: The Backgate Effect or the Body Effect



To get rid of the body effect, one can short the bulk (or the backgate) to the source such that V_{SB} =0

$$V_{TN} = V_{TN}(V_{SB} = 0) + \gamma_n \left(\sqrt{-2\phi_p + V_{SB}} - \sqrt{-2\phi_p}\right)$$

(0)

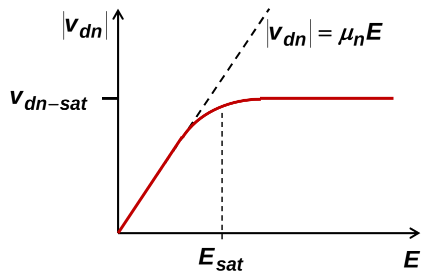
However, depending on the technology used, this may not always be possible……..

NMOS Transistor: Velocity Saturation

The drift velocity vs field curve for almost all materials is not linear and therefore

$$v_{dn} = -\mu_n E$$

does not really hold



Velocity saturates at high fields!

A better approximation is:

$$v_{dn} = -\frac{\mu_n E}{1 + \frac{|E|}{E_{sat}}}$$

In Silicon: $E_{sat} \sim 5 \times 10^4$ V/cm

Current in the inversion channel at the location y is:

$$I_D = W\, Q_N(y) \frac{\mu_n E(y)}{1 + \frac{|E|}{E_{sat}}} = W\, C_{ox} \left(V_{GS} - V_{TN} - V_{CS}\right) \frac{\mu_n \frac{dV_{CS}(y)}{dy}}{1 + \frac{1}{E_{sat}} \left|\frac{dV_{CS}(y)}{dy}\right|}$$

NMOS Transistor: Velocity Saturation

Current in the inversion channel at the location y is:

$$I_D = W\, Q_N(y) \frac{\mu_n E(y)}{1 + \frac{|E|}{E_{sat}}} = W\, C_{ox} \left(V_{GS} - V_{TN} - V_{CS}\right) \frac{\mu_n \frac{dV_{CS}(y)}{dy}}{1 + \frac{1}{E_{sat}} \left|\frac{dV_{CS}(y)}{dy}\right|}$$

Integrate the above equation from y=0 to y=L:

$$\int_0^L I_D \left(1 + \frac{1}{E_{sat}} \left|\frac{dV_{CS}(y)}{dy}\right|\right) dy = \int_0^{V_{DS}} W\, \mu_n C_{ox} \left(V_{GS} - V_{TN} - V_{CS}\right) dV_{CS}$$

Answer is (in linear region):

$$I_D = \frac{W}{L} \mu_n C_{ox} \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right) \frac{V_{DS}}{\left(1 + \frac{V_{DS}}{V_{sat}}\right)}$$

$$V_{sat} = E_{sat} L$$

Answer is (in saturation region):

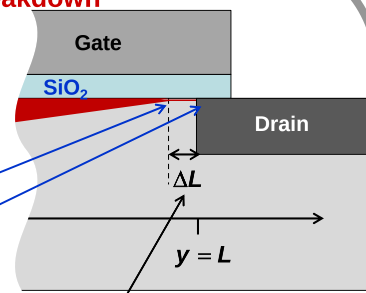
$$I_D = \frac{W}{2L} \frac{\mu_n}{\left(1 + \frac{V_{GS} - V_{TN}}{V_{sat}}\right)} C_{ox} \left(V_{GS} - V_{TN}\right)^2$$

Velocity saturation decreases the current

NMOS Transistor: Breakdown

Large fields near the drain end in saturation can lead to breakdown

Breakdown limits the maximum value of V_{DS}



Channel potential: $V_{CS}(y) = V_{GS} - V_{TN}$

Channel potential: $V_{CS}(y) = V_{DS}$

Potential drop in this region:

$$V_{DS} - (V_{GS} - V_{TN})$$

Field in this region:

$$\frac{V_{DS} - (V_{GS} - V_{TN})}{\Delta L}$$