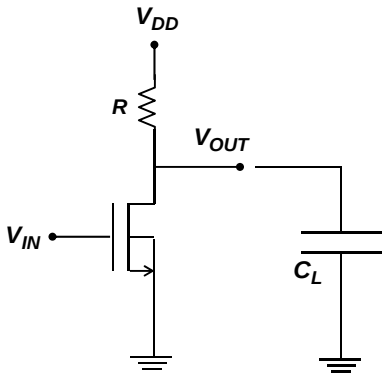
Lecture 23

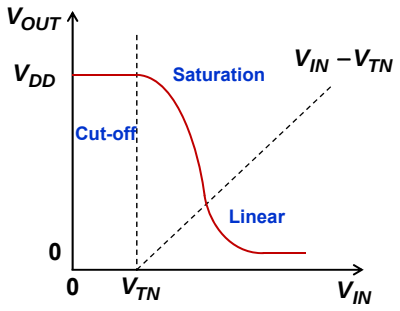
CMOS Logic Gates and Digital VLSI – I

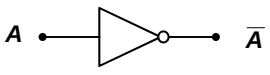
In this lecture you will learn:

- The CMOS Inverter
- Charge and Discharge Dynamics
- Power Dissipation
- Digital Levels and Noise

A NFET Inverter

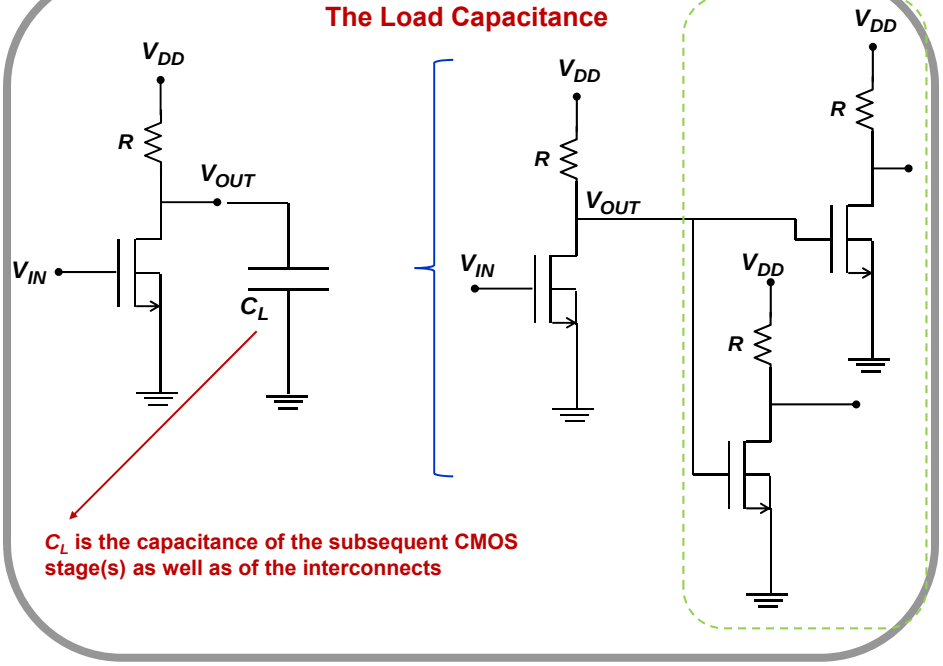






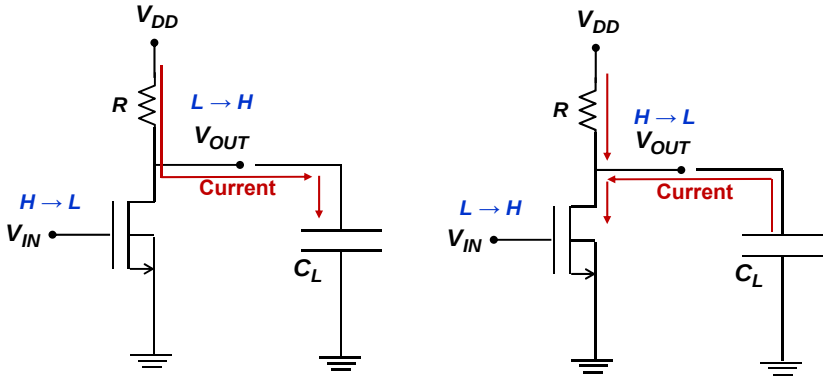
A	X
0	1
1	0

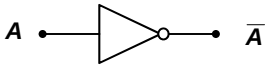
The Load Capacitance



C_L is the capacitance of the subsequent CMOS stage(s) as well as of the interconnects

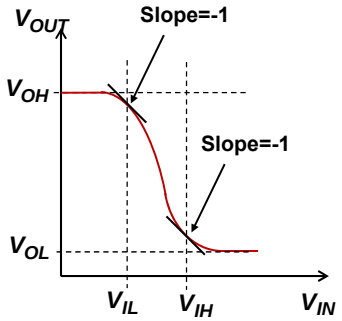
A NFET Inverter: Charging and Discharging Dynamics

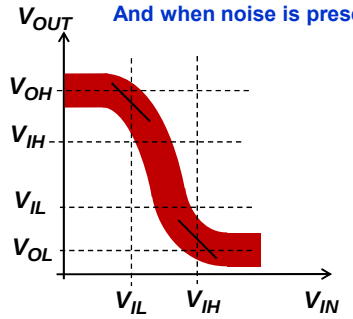




A	X
0	1
1	0

Digital Signal Levels and Noise





And when noise is present……

One must have:

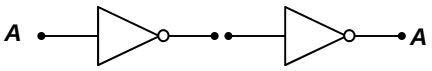
$$V_{OL} + noise < V_{IL}$$

$$V_{OH} - noise > V_{IH}$$

Noise margins:

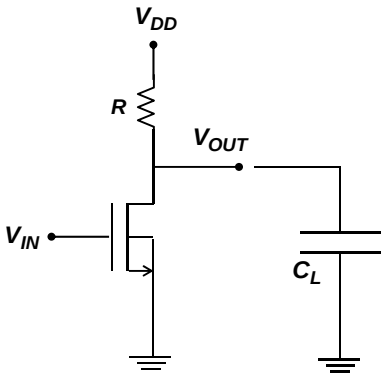
$$V_{IL} - V_{OL}$$

$$V_{OH} - V_{IH}$$



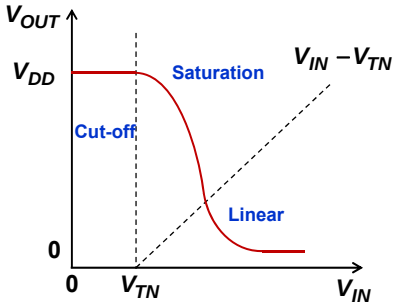
Noise and device variations sets the minimum V_{DD} one can use

A NFET Inverter: Noise Margins



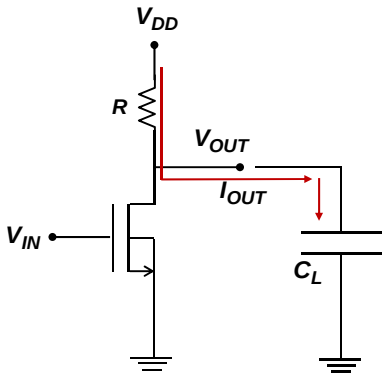
Problem:

The input/output characteristics are not symmetric



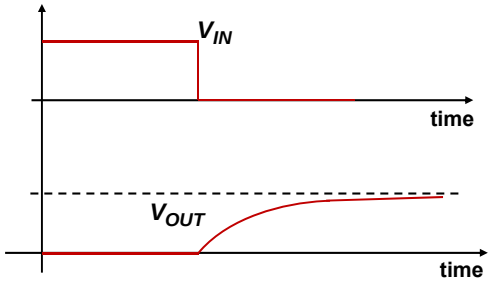
Noise margins are good but not excellent

A NFET Inverter: Charging Dynamics



Problem:

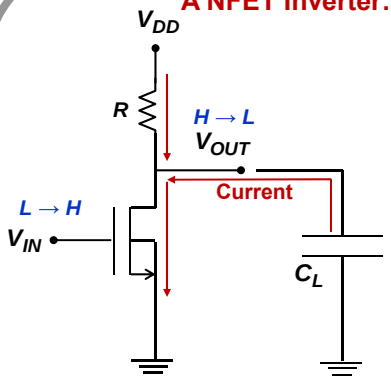
When the output is LOW, charging of the output to HIGH is slow because charging current is not uniform



$$I_{OUT} = \frac{V_{DD} - V_{OUT}}{R} = C_L \frac{dV_{OUT}}{dt}$$

$$\Rightarrow V_{OUT}(t) = V_{DD}\left[1 - e^{-\frac{t}{RC_L}}\right]$$

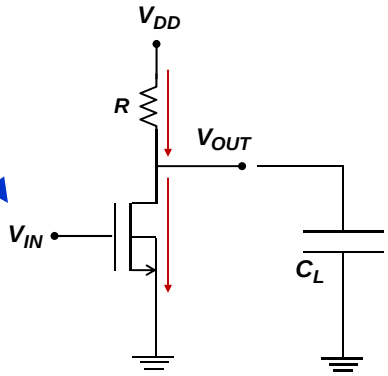
A NFET Inverter: Static Power Dissipation



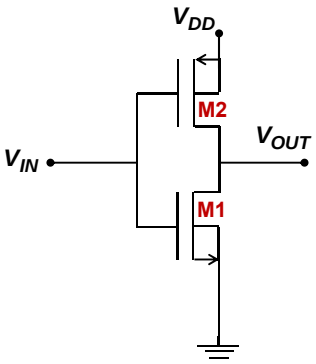
Problem:

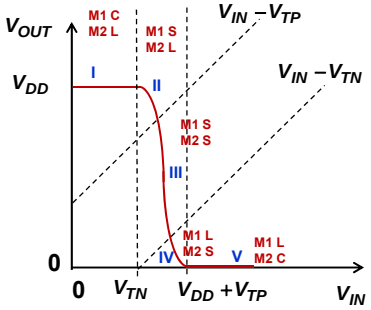
When the input is HIGH, and the output is LOW, current keeps flowing through the FET and the resistor forever!!

This is an example of static power dissipation – extremely bad!



A CMOS Inverter: Noise Margins

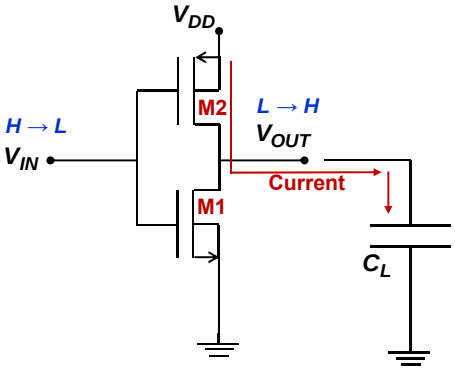


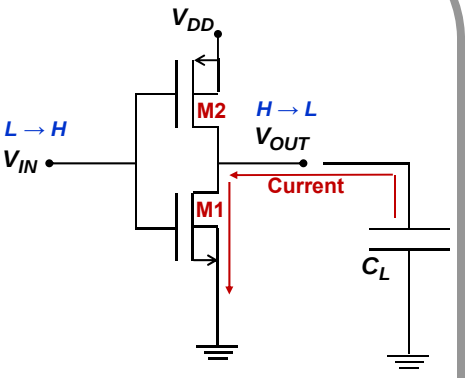


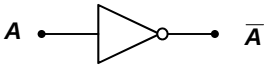
If V_{TN} and $V_{DD}+V_{TP}$ are close to each other, the transition region can be made narrow and sharp

→The noise margins can be very wide!!

A CMOS Inverter: Charging and Discharging Dynamics

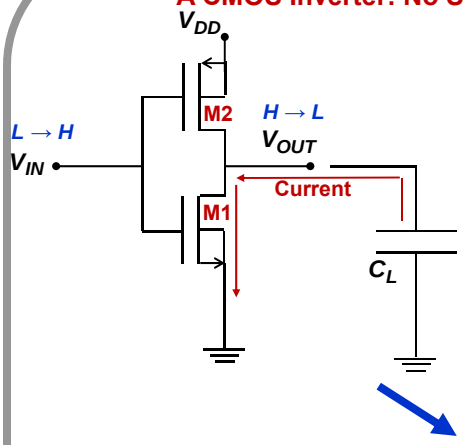






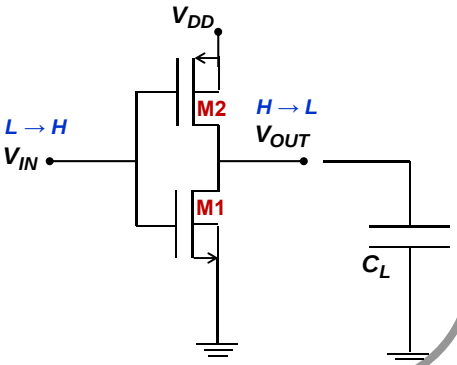
A	X
0	1
1	0

A CMOS Inverter: No Static Power Dissipation

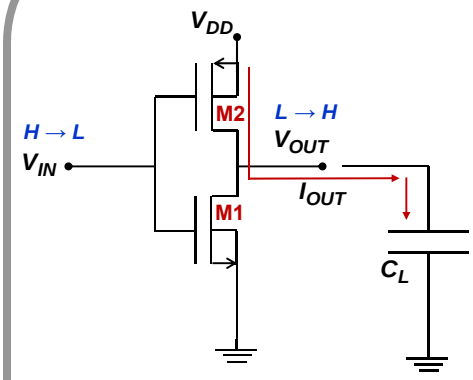


When the input goes HIGH or LOW, power is only dissipated during the time when the output makes the transition – after this period, there is no power dissipation

There is no static power dissipation (ideally!), only dynamic power dissipation!!



A CMOS Inverter: Charging Dynamics



When the output is LOW, initial charging of the output to HIGH is done with a uniform current supplied by the PFET in saturation:

$$I_{OUT} = C_L \frac{dV_{OUT}}{dt}$$

$$\Rightarrow \frac{k_p}{2}(V_{IN} - V_{DD} - V_{TP})^2 = C_L \frac{dV_{OUT}}{dt}$$

$$\Rightarrow \frac{k_p}{2}(V_{DD} + V_{TP})^2 = C_L \frac{dV_{OUT}}{dt}$$

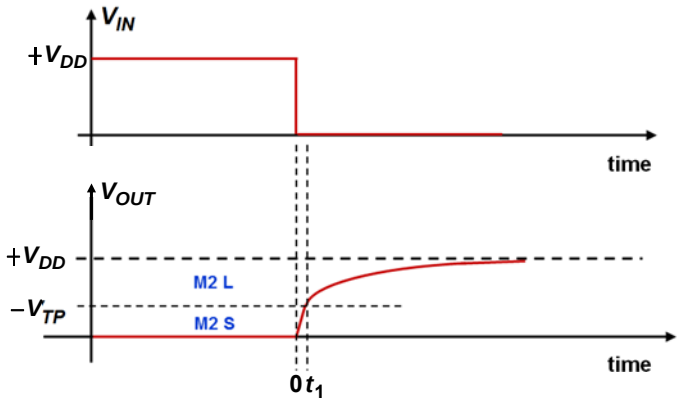
$$\Rightarrow V_{OUT}(t) = \frac{k_p}{2C_L}(V_{DD} + V_{TP})^2 t$$

Condition for the PFET to be in saturation:

$$V_{DS} < V_{GS} - V_{TP}$$
$$\Rightarrow V_{OUT} - V_{DD} < V_{IN} - V_{DD} - V_{TP}$$
$$\Rightarrow V_{OUT} < V_{IN} - V_{TP} \approx -V_{TP}$$

When V_{OUT} becomes larger than $-V_{TP}$ then the PFET goes into the linear region….

A CMOS Inverter: Charging Dynamics



For times $0 < t < t_1$ when the PFET (M2) is in saturation:

$$V_{OUT}(t) = \frac{k_p}{2C_L}(V_{DD} + V_{TP})^2 t$$

$$\Rightarrow t_1 = -V_{TP}\frac{2C_L}{k_p(V_{DD}+V_{TP})^2} = \frac{-2V_{TP}}{(V_{DD}+V_{TP})}\tau \qquad \left\{ \tau = \frac{C_L}{k_p(V_{DD}+V_{TP})} \right.$$

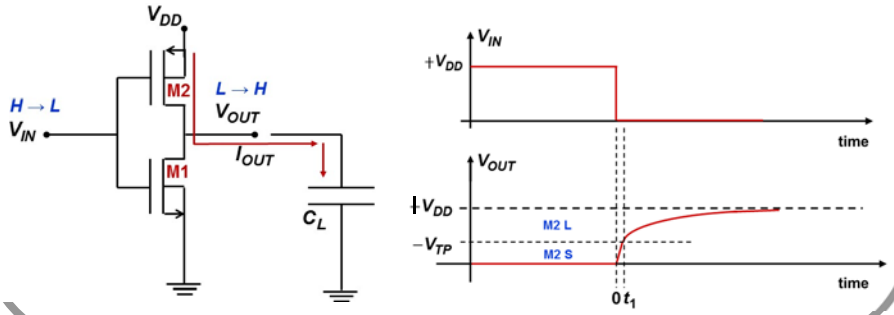
A CMOS Inverter: Charging Dynamics

When V_{OUT} becomes larger than $-V_{TP}$ then the PFET goes into the linear region, and from then onwards:

$$I_{OUT} = C_L\frac{dV_{OUT}}{dt}$$

$$\Rightarrow k_p\left(V_{IN} - V_{DD} - V_{TP} - \frac{(V_{OUT}-V_{DD})}{2}\right)(V_{OUT}-V_{DD}) = C_L\frac{dV_{OUT}}{dt}$$

$$\Rightarrow -k_p\left(V_{DD} + V_{TP} + \frac{(V_{OUT}-V_{DD})}{2}\right)(V_{OUT}-V_{DD}) = C_L\frac{dV_{OUT}}{dt}$$



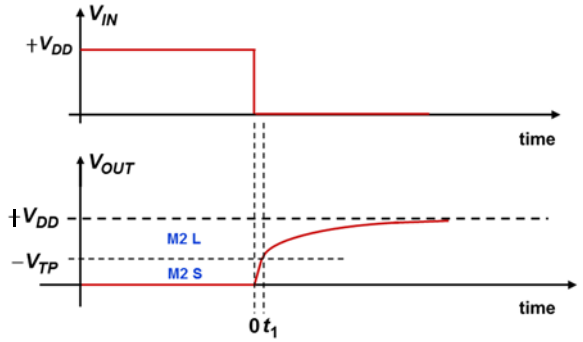
One can obtain faster charging compared to a resistor in place of a PFET!

A CMOS Inverter: Charging Dynamics

$$-k_p\left(V_{DD}+V_{TP}+\frac{(V_{OUT}-V_{DD})}{2}\right)(V_{OUT}-V_{DD})=C_L\frac{dV_{OUT}}{dt}$$

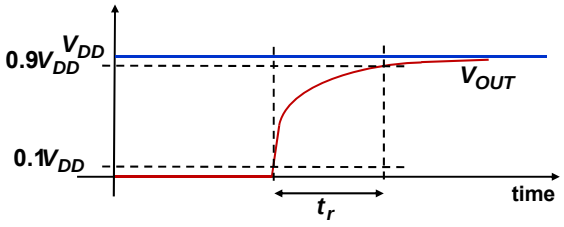
$$\Rightarrow \int_{-V_{TP}}^{V_{OUT}} \frac{dV_{OUT}}{\left(V_{DD}+V_{TP}+\frac{(V_{OUT}-V_{DD})}{2}\right)(V_{OUT}-V_{DD})}=-\frac{k_p}{C_L}\int_{t_1}^{t} dt=-\frac{k_p}{C_L}t$$

$$\Rightarrow V_{OUT}(t>t_1)=\frac{V_{DD}\left(1-e^{-(t-t_1)/\tau}\right)-2V_{TP}\,e^{-(t-t_1)/\tau}}{1+e^{-(t-t_1)/\tau}} \qquad \tau=\frac{C_L}{k_p(V_{DD}+V_{TP})}$$

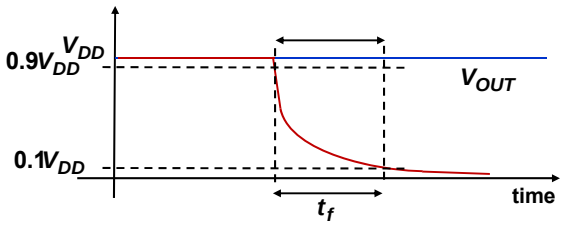


Rise Times and Fall Times

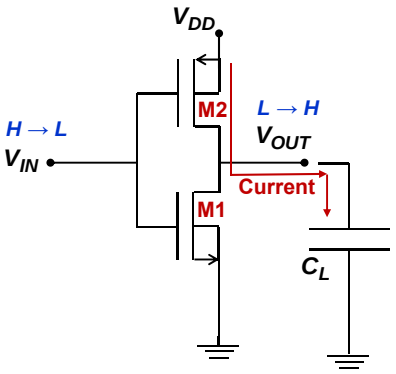
Rise Time: The time it takes the output to increase from 10% to 90% of the HIGH value



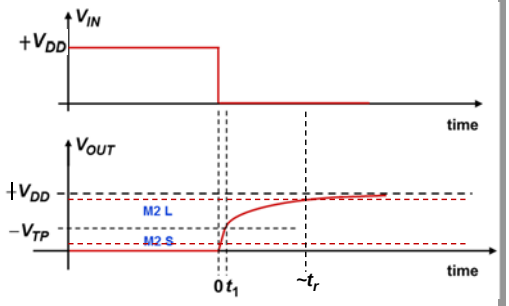
Fall Time: The time it takes the output to decrease from 90% to 10% of the HIGH value



A CMOS Inverter: Charging Dynamics



One can obtain faster charging compared to a resistor



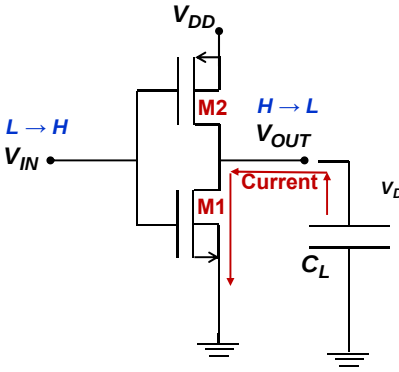
$$t_r \approx \frac{2C_L}{k_p(V_{DD}+V_{TP})}\left\{\frac{-V_{TP}}{V_{DD}+V_{TP}}-\frac{1}{2}\ln\left[\frac{0.1V_{DD}}{2(V_{DD}+V_{TP})-0.1V_{DD}}\right]\right\}$$

$$\propto \frac{L^2}{\mu_h V_{DD}} \sim \tau_t \quad \{ \text{if } C_L \propto C_{gs}$$

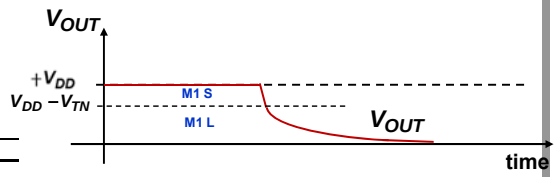
FET transit time

In reality, the load capacitance is not just due to the next FET gate - it also includes the interconnect capacitances

A CMOS Inverter: Discharging Dynamics



One can obtain faster charging compared to a resistor



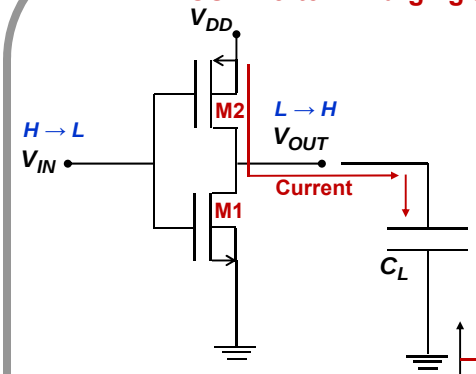
$$t_f \approx \frac{2C_L}{k_n(V_{DD}-V_{TN})}\left\{\frac{V_{TN}}{V_{DD}-V_{TN}}-\frac{1}{2}\ln\left[\frac{0.1V_{DD}}{2(V_{DD}-V_{TN})-0.1V_{DD}}\right]\right\}$$

$$\propto \frac{L^2}{\mu_n V_{DD}} \sim \tau_t \quad \{ \text{if } C_L \propto C_{gs}$$

FET transit time

In reality, the load capacitance is not just due to the next FET gate - it also includes the interconnect capacitances

A CMOS Inverter: Charging and Discharging Dynamics



How to charge and discharge faster?

- Increase k_n and k_p of FETs
- Decrease C_L
- Increase charging current

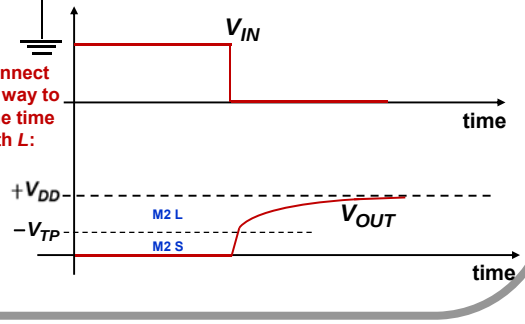
→ Increase supply voltage V_{DD}

At what price?

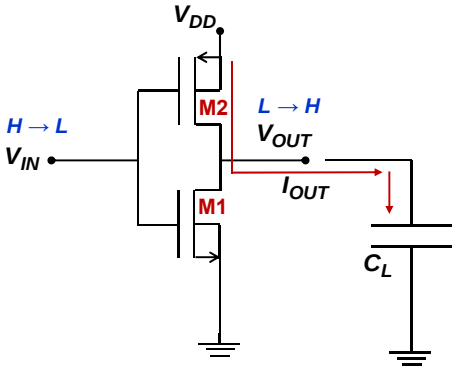
Assuming C_L is not dominated by interconnect capacitance (not generally true), the only way to increase k_n and k_p of FETs and at the same time decrease C_{gs} is to decrease the FET length L:

$$t_r \propto \frac{L^2}{\mu_h V_{DD}}$$

$$t_f \propto \frac{L^2}{\mu_n V_{DD}}$$



A CMOS Inverter: Dynamic Power Dissipation

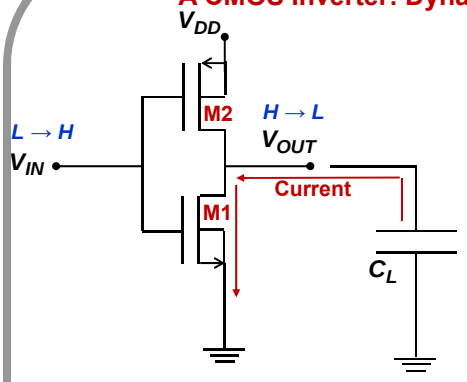


Q: How much energy is dissipated (in the PFET and the wires) in charging the capacitor to HIGH from LOW?

A: Irrespective of how it is charged, the net energy dissipation in charging a capacitor equals the energy stored in the capacitor after charging!

$$E_D = \frac{1}{2} C_L V_{DD}^2$$

A CMOS Inverter: Dynamic Power Dissipation



Q: How much energy is dissipated (in the NFET and the wires) in discharging the capacitor from HIGH to LOW?

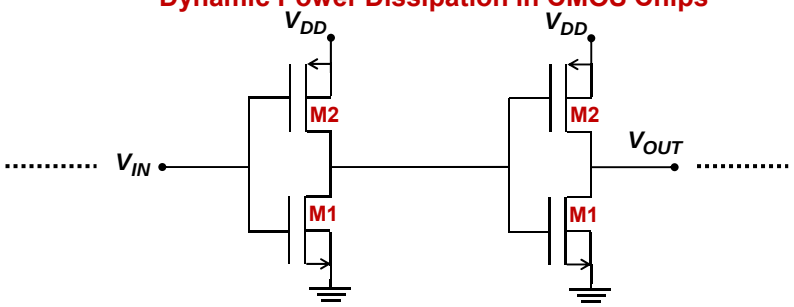
A: Irrespective of how it is discharged, the net energy dissipation in discharging a capacitor equals the energy stored in the capacitor before discharging!

$$E_D = \frac{1}{2} C_L V_{DD}^2$$

Total energy dissipation in one charge and discharge cycle:

$$E_D = C_L V_{DD}^2$$

Dynamic Power Dissipation in CMOS Chips



Total energy dissipation in one charge and discharge cycle per FET:

$$E_D = C_{gs} V_{DD}^2$$ → Ignoring interconnect capacitance

Total energy dissipation in one charge and discharge cycle if N_{FET} FETs in the chip are active:

$$E_D = N_{FET} C_{gs} V_{DD}^2$$

Total power dissipation (energy dissipation per second) if N_{FET} FETs are active:

$$P_D = N_{FET} f_{CLK} C_{gs} V_{DD}^2$$

Number of cycles per second ~ f_{CLK}

Dynamic Power Dissipation in CMOS Chips

E8500 45 nm Chipset

Clock speed = 3.16 GHz
Gate length: 45 nm = .045 μm
Number of FETs in the chip = 410 X 10^6
Power supply voltage ~ 2 V

$$P_D = N_{FET} f_{CLK} C_{gs} V_{DD}^2$$

Fraction of active FETs at any instant on the average (~0.4%)

$N_{FET} = .004 \times 410e6 = 1.64e6$

$f_{CLK} = 3.1e9$

$t_{ox} = 10A$ (equivalent low-κ thickness)

$W = 2\ \mu m$

$L = .045\ \mu m$

$$C_{gs} = \frac{2}{3}\frac{\varepsilon_{ox}}{t_{ox}} WL = 2\ \text{femto} - \text{F}$$

$V_{DD} = 2\ V$

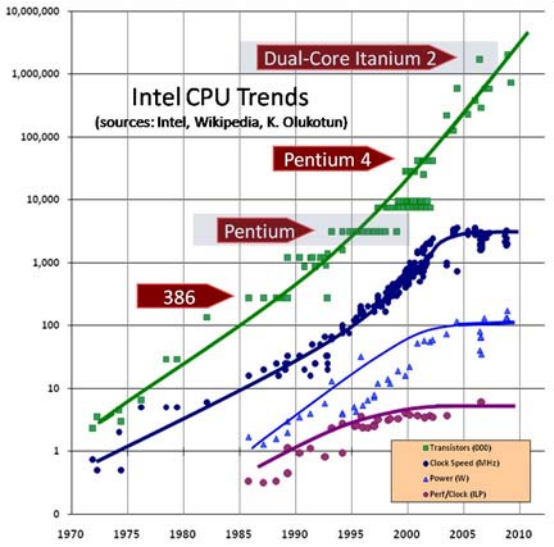
Our power dissipation estimate:

$$P_D = N_{FET} f_{CLK} C_{gs} V_{DD}^2$$
$$= 42\ \text{Watts!!}$$

Actual published number:

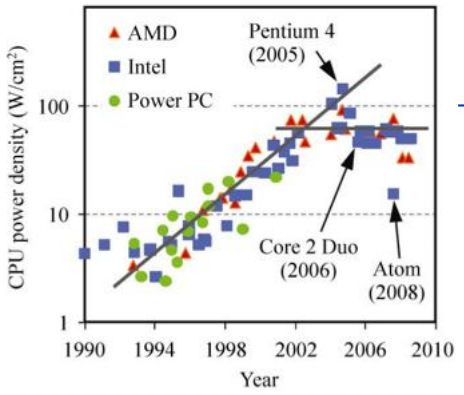
$$P_T = 65\ \text{Watts!!}$$
$$= P_D + P_S$$

Power Dissipation in CMOS Chips



→ 100 W/cm²

Power Dissipation in CMOS Chips



→ 100 W/cm²