Lecture 22

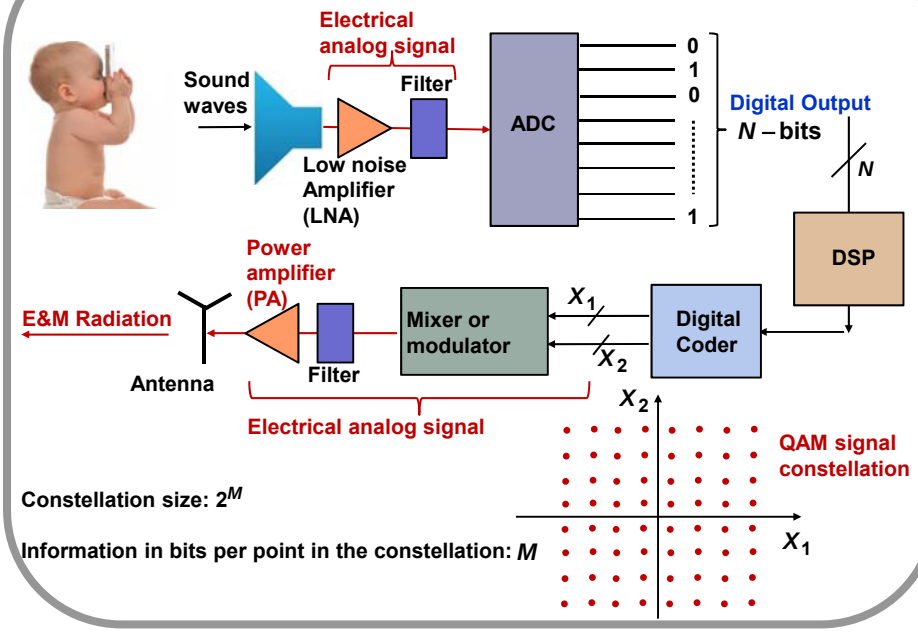
Circuit Design Techniques and Applications – II

Wireless Communications

In this lecture you will learn:

- Circuits for wireless communications
- Signal multipliers and mixers
- Single-balanced and double-balanced mixers
- Sample and hold circuits
- Analog to digital converters
- Digital to analog converters

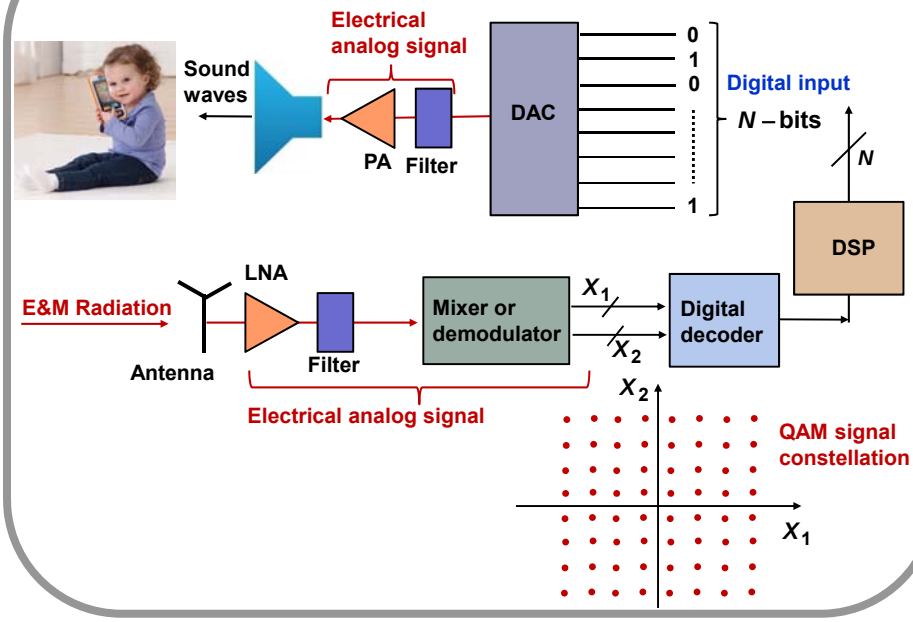
Signal Transmission in Wireless Communications



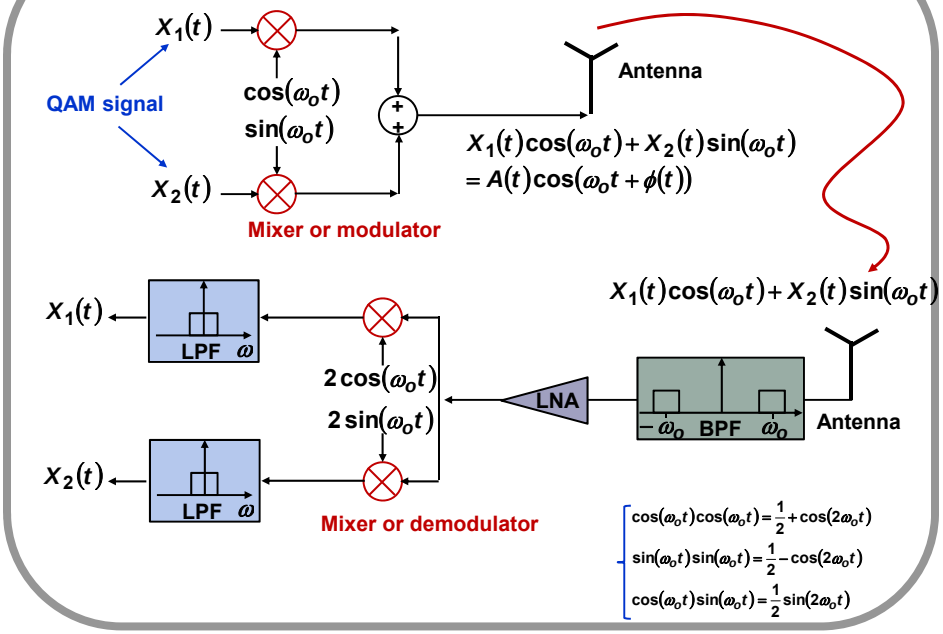
Constellation size: 2^M

Information in bits per point in the constellation: M

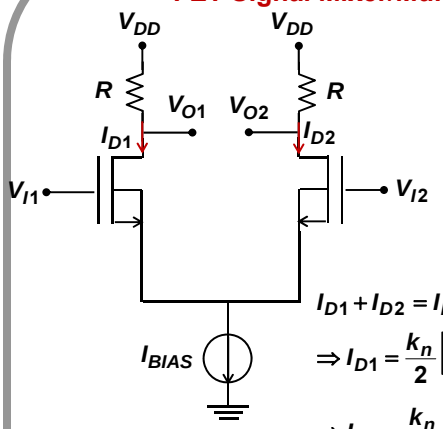
Signal Reception in Wireless Communications

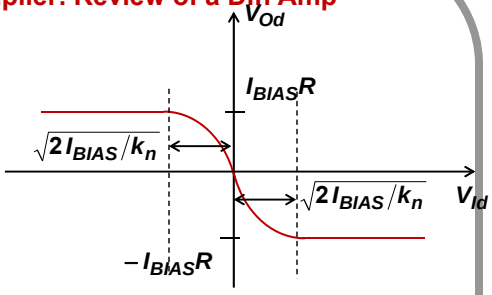


RF Mixer or Modulator/Demodulator



FET Signal Mixer/Multiplier: Review of a Diff Amp





$$I_{D1}+I_{D2}=I_{BIAS}$$

$$\Rightarrow I_{D1}=\frac{k_n}{2}\left[(V_{GS1}-V_{TN})^2\right]=\frac{I_{BIAS}}{2}+k_n\frac{V_{Id}}{4}\sqrt{4\frac{I_{BIAS}}{k_n}-V_{Id}^2}$$

$$\Rightarrow I_{D2}=\frac{k_n}{2}\left[(V_{GS2}-V_{TN})^2\right]=\frac{I_{BIAS}}{2}-k_n\frac{V_{Id}}{4}\sqrt{4\frac{I_{BIAS}}{k_n}-V_{Id}^2}$$

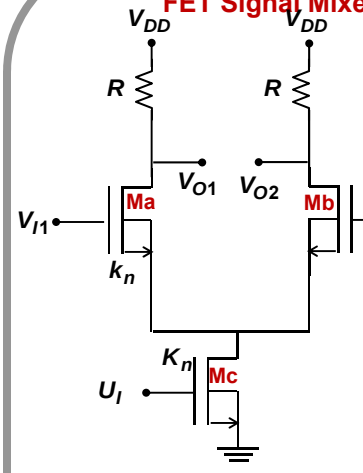
$$V_{Od}=V_{O1}-V_{O2}=-Rk_n\frac{(V_{I1}-V_{I2})}{2}\sqrt{4\frac{I_{BIAS}}{k_n}-(V_{I1}-V_{I2})^2}$$

Assume small

Provided: $\sqrt{\frac{2I_{BIAS}}{k_n}} >> (V_{I1}-V_{I2})$

$$\approx -Rk_n\frac{(V_{I1}-V_{I2})}{2}\sqrt{4\frac{I_{BIAS}}{k_n}}$$

FET Signal Mixer/Multiplier: Single-Balanced Mixer



A single-balanced mixer:

$$V_{Od}=V_{O1}-V_{O2}\approx -Rk_n\frac{(V_{I1}-V_{I2})}{2}\sqrt{4\frac{I_{BIAS}}{k_n}}$$

$$I_{BIAS}\approx\frac{K_n}{2}(U_I-V_{TN})^2$$

Product terms

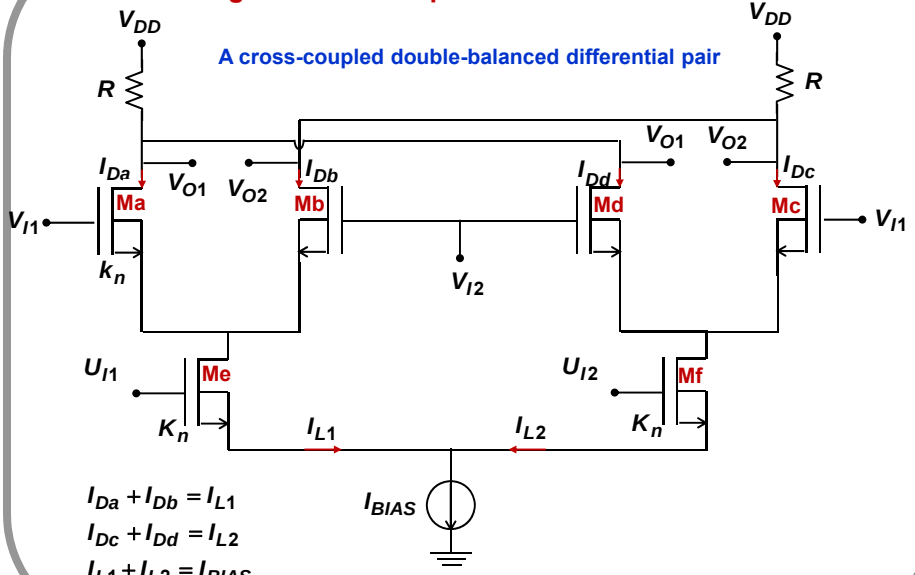
$$V_{Od}=V_{O1}-V_{O2}\approx -Rk_n\frac{(V_{I1}-V_{I2})}{2}\sqrt{2\frac{K_n}{k_n}}(U_I-V_{TN})$$

But still not quite what one would want……..

i) The input voltage U_I is not differential…….
ii) The two input voltages being multiplied don't appear symmetrically in the final answer
iii) There is an additional term proportional only to V_{I1}-V_{I2} in the output

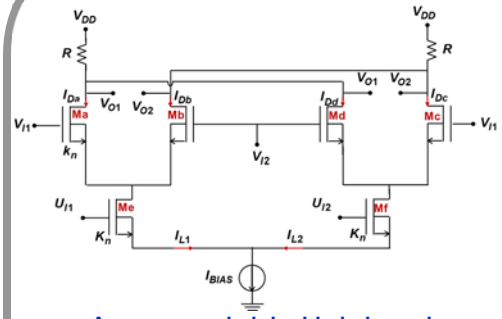
FET Signal Mixer/Multiplier: A Double-Balanced Mixer

A cross-coupled double-balanced differential pair



$$I_{Da} + I_{Db} = I_{L1}$$
$$I_{Dc} + I_{Dd} = I_{L2}$$
$$I_{L1} + I_{L2} = I_{BIAS}$$

FET Signal Mixer/Multiplier: A Double-Balanced Mixer



A cross-coupled double-balanced differential pair

$$I_{Da} + I_{Db} = I_{L1}$$
$$I_{Dc} + I_{Dd} = I_{L2}$$
$$I_{L1} + I_{L2} = I_{BIAS}$$

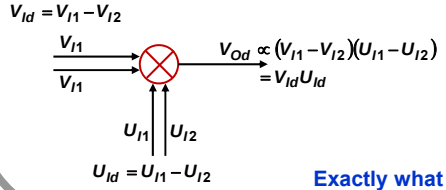
$$I_{Da} = \frac{k_n}{2}\left[(V_{GSa} - V_{TN})^2\right] \approx \frac{I_{L1}}{2} + k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L1}}{k_n}}$$

$$I_{Db} = \frac{k_n}{2}\left[(V_{GSb} - V_{TN})^2\right] = \frac{I_{L1}}{2} - k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L1}}{k_n}}$$

$$I_{Dc} = \frac{k_n}{2}\left[(V_{GSc} - V_{TN})^2\right] \approx \frac{I_{L2}}{2} + k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L2}}{k_n}}$$

$$I_{Dd} = \frac{k_n}{2}\left[(V_{GSd} - V_{TN})^2\right] \approx \frac{I_{L2}}{2} - k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L2}}{k_n}}$$

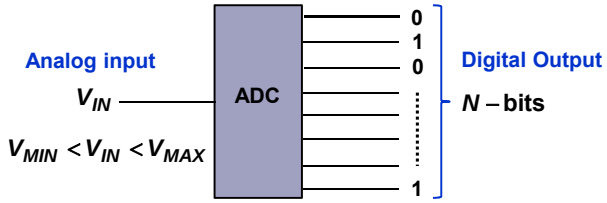
$$V_{Id} = V_{I1} - V_{I2}$$



$$V_{Od} = V_{O1} - V_{O2} = -(I_{Da} + I_{Dd})R + (I_{Dc} + I_{Db})R$$
$$\approx -Rk_n \frac{(V_{I1} - V_{I2})}{2}\left(\sqrt{4\frac{I_{L1}}{k_n}} - \sqrt{4\frac{I_{L2}}{k_n}}\right)$$
$$= -Rk_n \frac{(V_{I1} - V_{I2})}{2}\sqrt{2\frac{K_n}{k_n}}(U_{I1} - U_{I2})$$
$$= -R\sqrt{\frac{k_n K_n}{2}}(V_{I1} - V_{I2})(U_{I1} - U_{I2})$$

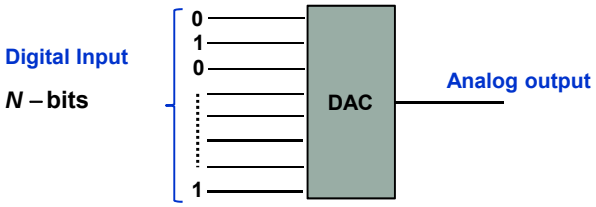
Exactly what one would want! → Product terms

Analog-to-Digital Converters(ADCs) and Digital-to-Analog Converters (DACs)

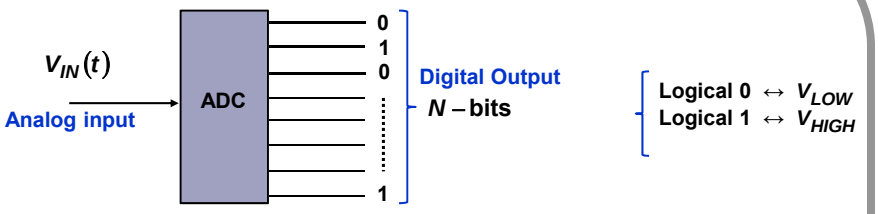


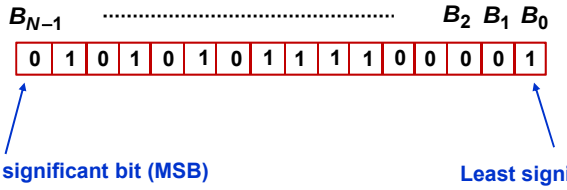
Resolution: $\dfrac{|V_{MAX} - V_{MIN}|}{2^N - 1}$

Dynamic Range: $20\log_{10}\left(\dfrac{|V_{MAX}|}{|V_{MIN}|}\right)$



Analog-to-Digital Converters (ADCs)

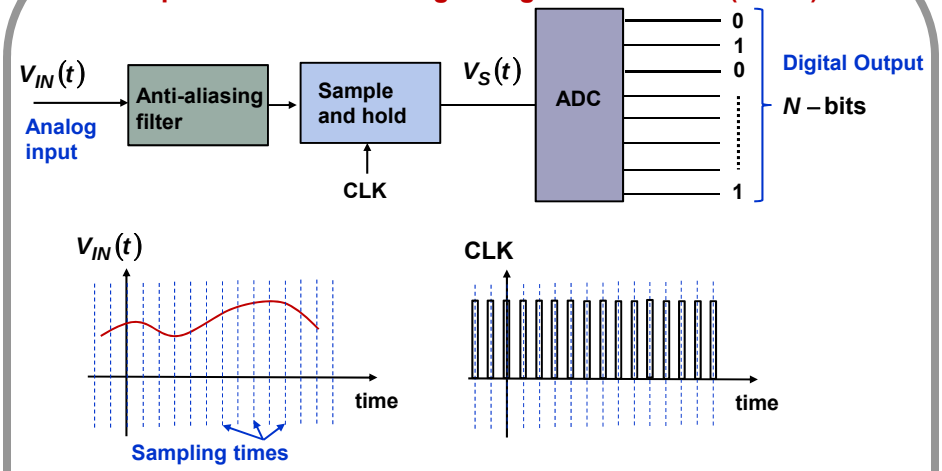




Analog value, corresponding to a digital value, is:

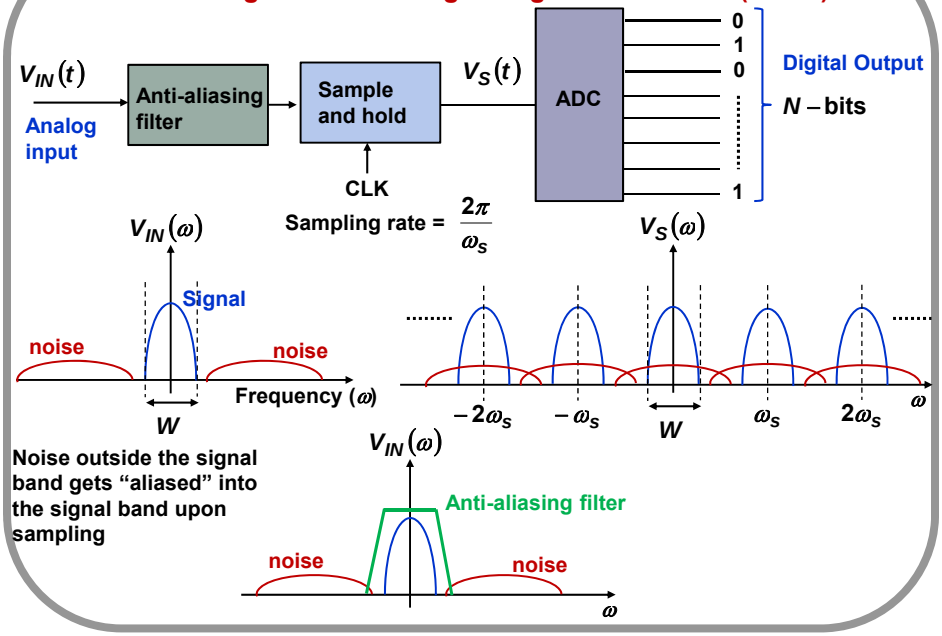
$$V_{MIN} + \frac{(V_{MAX} - V_{MIN})}{(2^N - 1)}\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots\ldots 2^2 B_2 + 2^1 B_1 + B_0\right]$$

Sample and Hold in Analog-to-Digital Converters (ADCs)



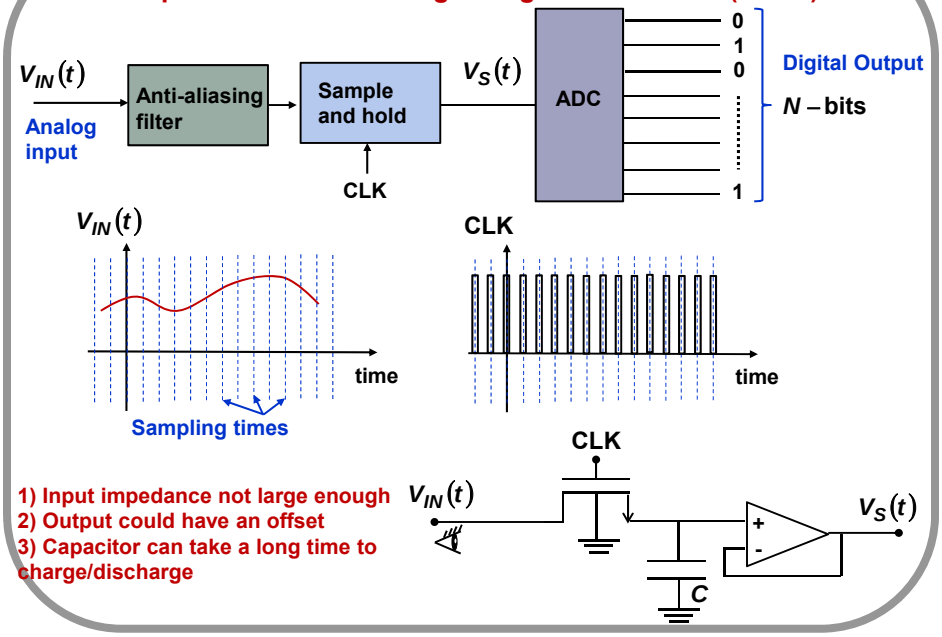
Sample the input waveform periodically and hold the sampled value in place till the next sampling event

Anti-Aliasing Filter in Analog-to-Digital Converters (ADCs)



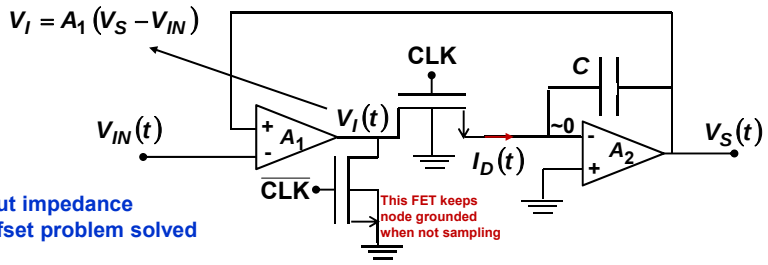
Noise outside the signal band gets "aliased" into the signal band upon sampling

Sample and Hold in Analog-to-Digital Converters (ADCs)



1) Input impedance not large enough
2) Output could have an offset
3) Capacitor can take a long time to charge/discharge

A Better Sample and Hold Circuit



Large input impedance
Output offset problem solved

Suppose when the CLK is HIGH the current through the FET is (assuming linear region):

$$I_D = k_n\left(V_{GS} - V_{TN} - \underbrace{\frac{V_{DS}}{2}}_{\text{small}}\right)V_{DS} \approx k_n(V_{CLK} - V_{TN})V_I = \frac{V_I}{R_n}$$

Then:

$$C\frac{d(0-V_S)}{dt} = I_D = \frac{V_I}{R_n} = \frac{A_1(V_S - V_{IN})}{R_n}$$

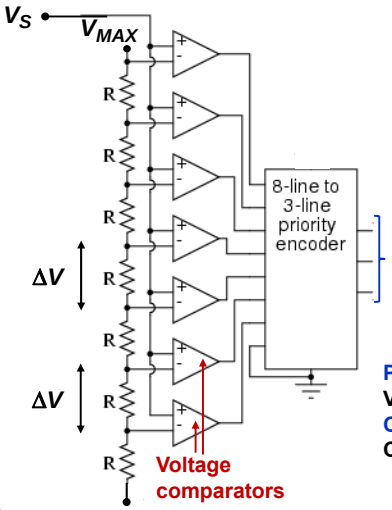
$$\Rightarrow \frac{dV_S}{dt} + \frac{A_1}{R_nC}V_S = \frac{A_1}{R_nC}V_{IN}$$

$$\Rightarrow V_S(t) = V_S(0)e^{-\frac{A_1}{R_nC}t} + V_{IN}\left(1 - e^{-\frac{A_1}{R_nC}t}\right)$$

V_S is pulled to V_{IN} and V_I is pulled to ~0 V within a very short time after CLK goes HIGH

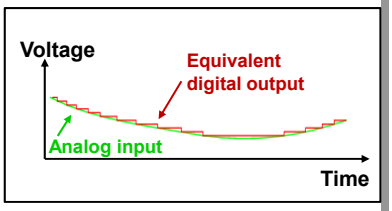
Flash Analog-to-Digital Converters (ADCs)

3-bit Flash ADC



Voltage resolution:

$$\Delta V = \frac{V_{MAX} - V_{MIN}}{2^N - 1}$$

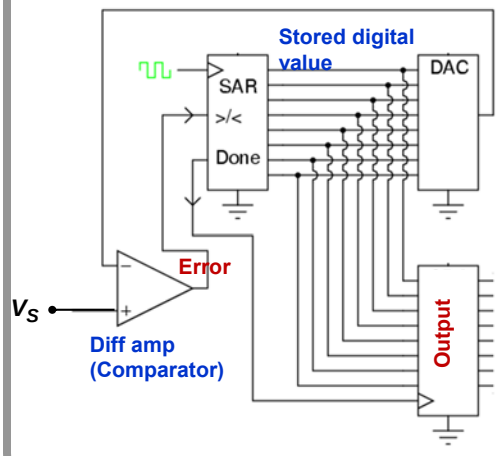


Pros:
Very high speed architecture

Cons:
Component intensive (requires 2^N-1 comparators)

Voltage comparators are essentially diff amps that have very low voltage offset errors; the input voltage offset error needs to be much less than the resolution of the ADC

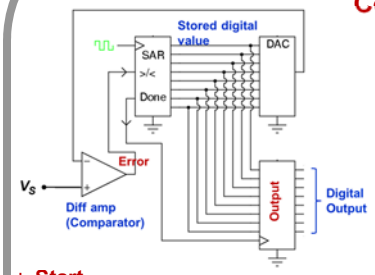
Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs)



Internal register keeps updating the stored digital value, compares the resulting analog value obtained from this digital value to the input analog value, until the stored value matches the input value

And then the stored value is placed in the output register

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs)



Consider a 4-bit SAR-ADC with a 0-3 V input range

0000 => 0 Volts 1111 => 3 Volts

Resolution = 0.2 Volt

Suppose the input is 1.70 Volts

Start

SAR = 1000 → DAC = 1.60 V → Error = +1 → Stored value is smaller

SAR = 1111 → DAC = 3.00 V → Error = -1 → Stored value is larger

SAR = 1100 → DAC = 2.40 V → Error = +1 → Stored value is larger

SAR = 1010 → DAC = 2.00 V → Error = +1 → Stored value is larger

SAR = 1001 → DAC = 1.80 V → Error = +1 → Stored value is larger

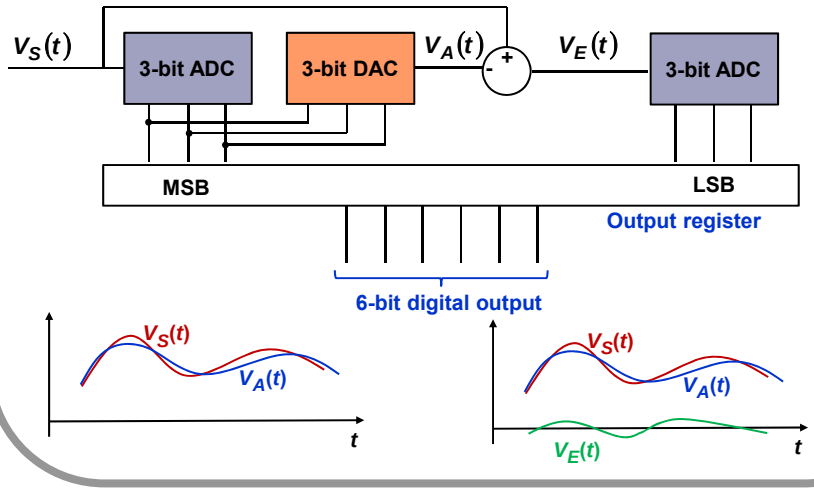
Produce output

Pros: Scalable to high resolutions Cons: Slower than flash

Pipelined Analog-to-Digital Converters (ADCs)

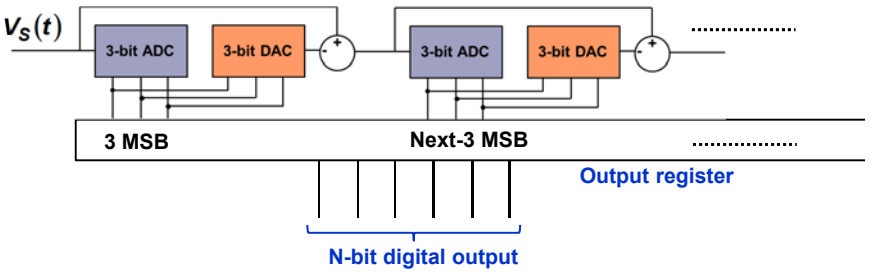
Main Idea: Use features of the flash architecture but scale to higher resolutions

Example: Build a 6-bit pipelined ADC from two 3-bit Flash ADCs



Pipelined Analog-to-Digital Converters (ADCs)

Can easily generalize:

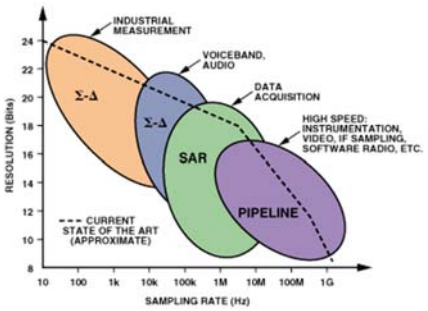


Pros:
Scalable to high resolutions
Fast

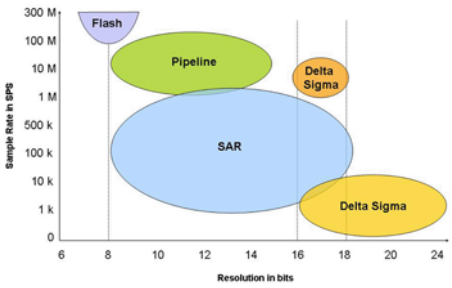
Cons:
Large power dissipation

Analog-to-Digital Converters (ADCs): State of the Art

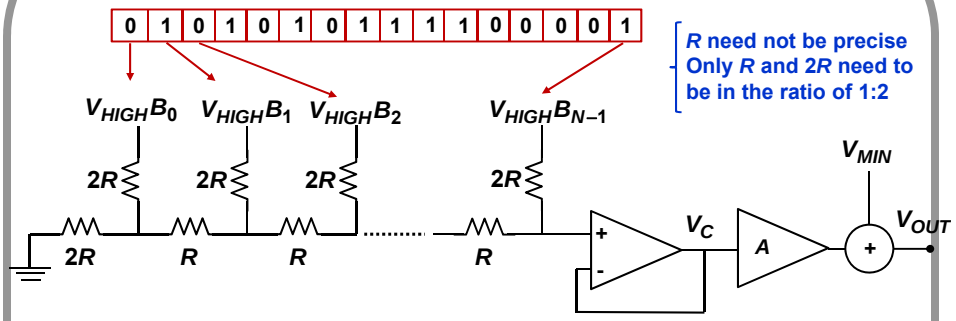
Walt Kester, Analog devices (2005)



William Klein, Texas Instruments (2007)



R/2R Ladder Digital-to-Analog Converters (DACs)



$$V_C = V_{HIGH}\left\{\frac{B_{N-1}}{2} + \frac{B_{N-2}}{4} + \frac{B_{N-3}}{8} + \ldots\ldots\ldots \frac{B_2}{2^{N-2}} + \frac{B_1}{2^{N-1}} + \frac{B_0}{2^N}\right\}$$

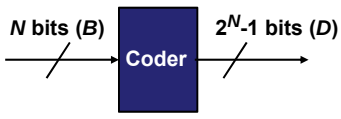
If:

$$A = \frac{(V_{MAX} - V_{MIN})}{2^N - 1}\frac{2^N}{V_{HIGH}}$$

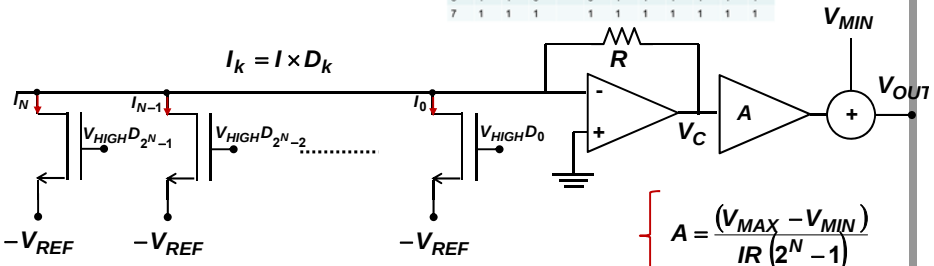
Then the output will be the desired analog output:

$$V_{OUT} = V_{MIN} + \frac{(V_{MAX} - V_{MIN})}{(2^N - 1)}\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots\ldots 2^2 B_2 + 2^1 B_1 + B_0\right]$$

Thermometer Code Digital-to-Analog Converters (DACs)



Dec	B2	B1	B0	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1



$$A = \frac{(V_{MAX} - V_{MIN})}{IR\left(2^N - 1\right)}$$

$$V_C = IR\left(D_{2^N-1} + D_{2^N-2} + \ldots\ldots\ldots + D_1 + D_0\right)$$

$$V_C = IR\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots\ldots + 2^2 B_2 + 2^1 B_1 + B_0\right]$$

$$V_{OUT} = V_{MIN} + \frac{(V_{MAX} - V_{MIN})}{(2^N - 1)}\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots\ldots 2^2 B_2 + 2^1 B_1 + B_0\right]$$

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