Lecture 15

Multistage FET Amplifiers

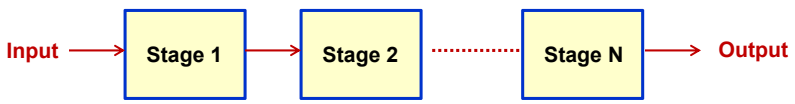
In this lecture you will learn:

- **Multistage FET Amplifiers**
- **The Cascade Design**
- **The Cascode Design**

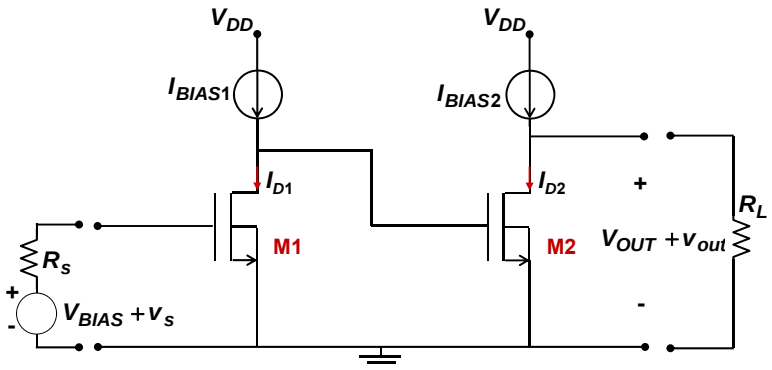
The Need for Multistage Amplifiers

Most modern amplifiers have multiple stage in order to:

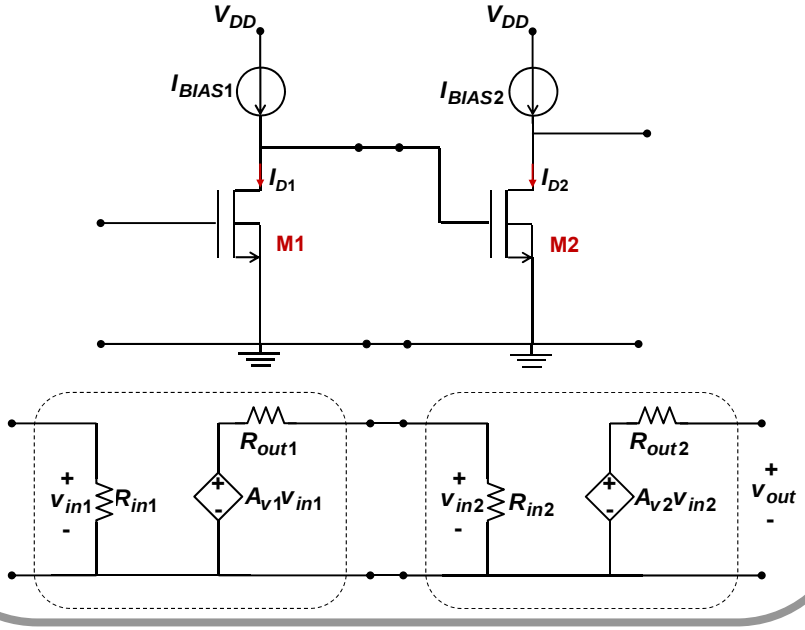
1) **Increase the amplifier gain (voltage gain or current gain or transimpedance gain or transconductance gain)**
2) **Transform the input resistance to match the source**
3) **Transform the output resistance to match the load**



A Cascade of Two CS Stages for a Voltage Amplifier

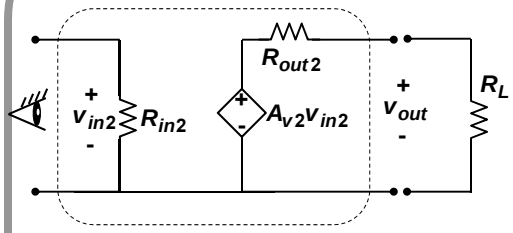


A Cascade of Two CS Stages for a Voltage Amplifier



A Cascade of Two CS Stages: Finding Input Resistances

1)



1) First find R_{in2} (input resistance of the last stage):

Make sure R_L is in place!!

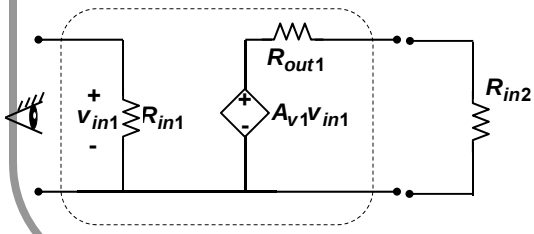
$$R_{in2} = \infty$$

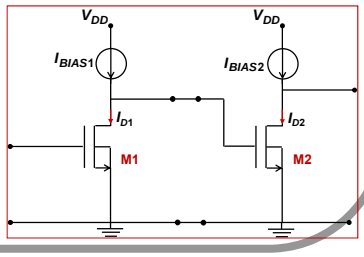
2) Then find R_{in1} (input resistance of the second last stage):

Make sure R_{in2} is in place!!

$$R_{in1} = \infty$$

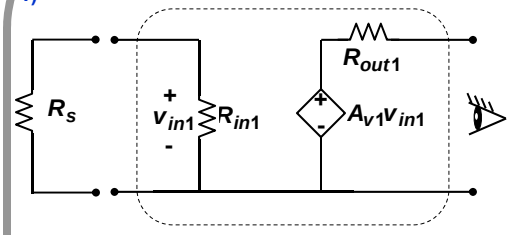
2)





A Cascade of Two CS Stages: Finding Output Resistances

1)



1) First find R_{out1} (output resistance of the first stage):

Make sure R_S is in place!!

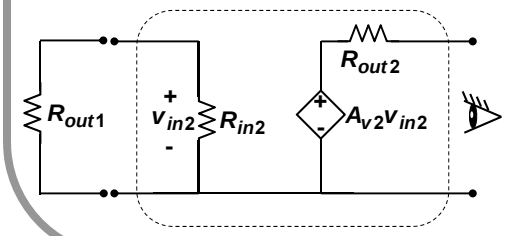
$$R_{out1} = (r_{o1} \,||\, r_{oc1})$$

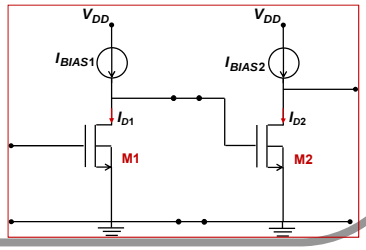
2) Then find R_{out2} (output resistance of the second stage):

Make sure R_{out1} is in place!!

$$R_{out2} = (r_{o2} \,||\, r_{oc2})$$

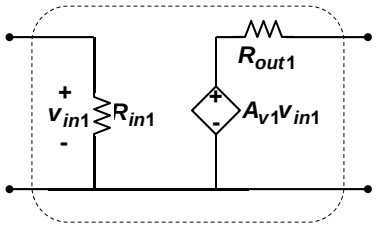
2)





A Cascade of Two CS Stages: Finding Voltage Gains

1)

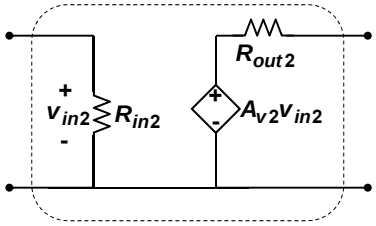


Open circuit voltage gains of CS stages do not depend on how the stages are connected (i.e. on source or load resistances)

Stage 1 Parameters:

$$R_{in1} = \infty$$
$$R_{out1} = (r_{o1} \,||\, r_{oc1})$$
$$A_{v1} = -g_{m1}(r_{o1} \,||\, r_{oc1})$$

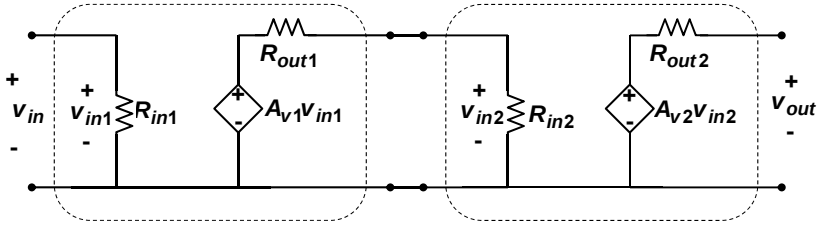
2)



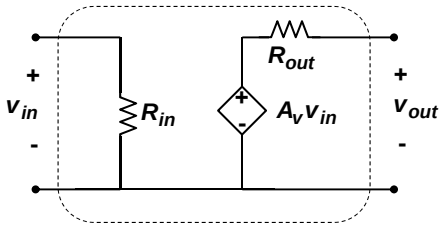
Stage 2 Parameters:

$$R_{in2} = \infty$$
$$R_{out2} = (r_{o2} \,||\, r_{oc2})$$
$$A_{v2} = -g_{m2}(r_{o2} \,||\, r_{oc2})$$

A Cascade of Two Amplifiers



The two stages can be combined into a single stage:



Input resistance:

$$R_{in} = R_{in1}$$

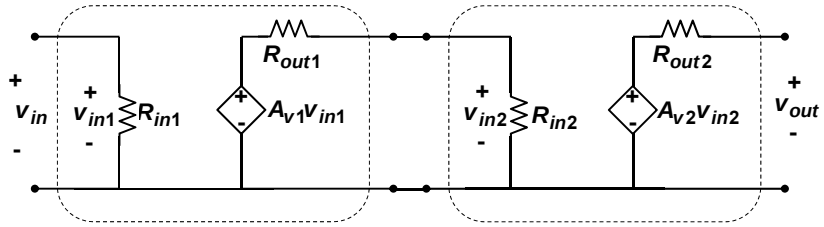
Output resistance:

$$R_{out} = R_{out2}$$

Open circuit voltage gain:

$$A_v = ?$$

A Cascade of Two Amplifiers



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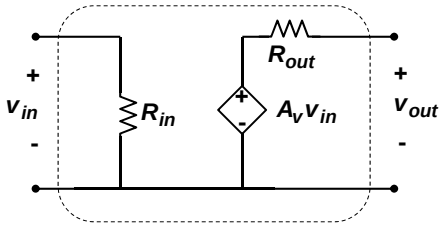


Open circuit voltage gain:

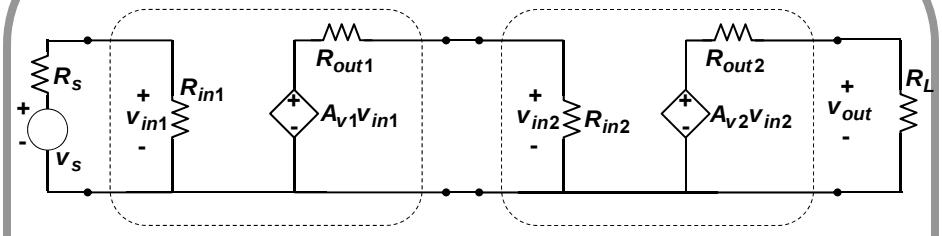
$$v_{out} = A_{v2}v_{in2} = A_{v2}A_{v1}v_{in1}\frac{R_{in2}}{R_{out1}+R_{in2}}$$

$$= A_{v2}A_{v1}v_{in}\frac{R_{in2}}{R_{out1}+R_{in2}}$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1}\underbrace{\frac{R_{in2}}{R_{out1}+R_{in2}}}$$

Inter-stage voltage divider

A Cascade of Two Amplifiers with a Source Resistor



Voltage gain:

$$v_{out} = A_{v2}v_{in2}\frac{R_L}{R_{out2}+R_L} = A_{v2}A_{v1}v_{in1}\frac{R_{in2}}{R_{out1}+R_{in2}}\frac{R_L}{R_{out2}+R_L}$$

$$= A_{v2}A_{v1}v_{in1}\frac{R_{in2}}{R_{out1}+R_{in2}}\frac{R_L}{R_{out2}+R_L}$$

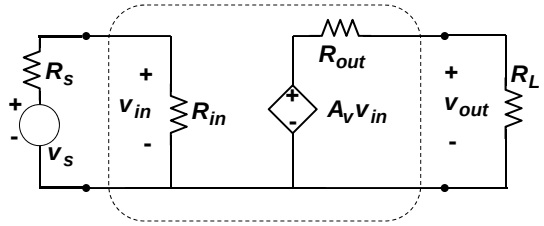
$$= A_{v2}A_{v1}v_s\frac{R_{in1}}{R_s+R_{in1}}\frac{R_{in2}}{R_{out1}+R_{in2}}\frac{R_L}{R_{out2}+R_L}$$

$$\Rightarrow \frac{v_{out}}{v_s} = A_{v2}A_{v1}\underbrace{\frac{R_{in1}}{R_s+R_{in1}}}\underbrace{\frac{R_{in2}}{R_{out1}+R_{in2}}}\underbrace{\frac{R_L}{R_{out2}+R_L}}$$

For the CS FET stages:
$R_{in1} = R_{in2} = \infty$

Input voltage divider | Inter-stage voltage divider | Output voltage divider

A Cascade of Two Amplifiers with a Source Resistor



Voltage gain:

$$v_{out} = A_v v_{in} \frac{R_L}{R_{out} + R_L}$$

$$= A_v v_s \frac{R_{in}}{R_s + R_{in}} \frac{R_L}{R_{out} + R_L}$$

$$\Rightarrow \frac{v_{out}}{v_s} = A_v \frac{R_{in}}{R_s + R_{in}} \frac{R_L}{R_{out} + R_L}$$

Input voltage divider

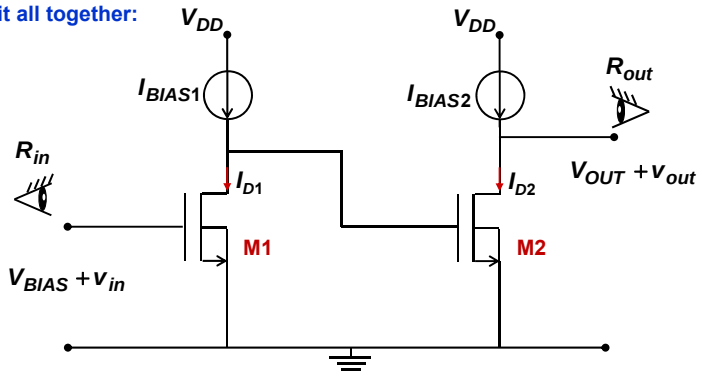
Output voltage divider

It is easier to use the single-stage model

The expression is the same as the one on the previous slide

A Cascade of Two CS Stages for a Voltage Amplifier

Putting it all together:



Input resistance:

$$R_{in} = \infty$$

Output resistance:

$$R_{out} = r_{o2} \| r_{oc2}$$

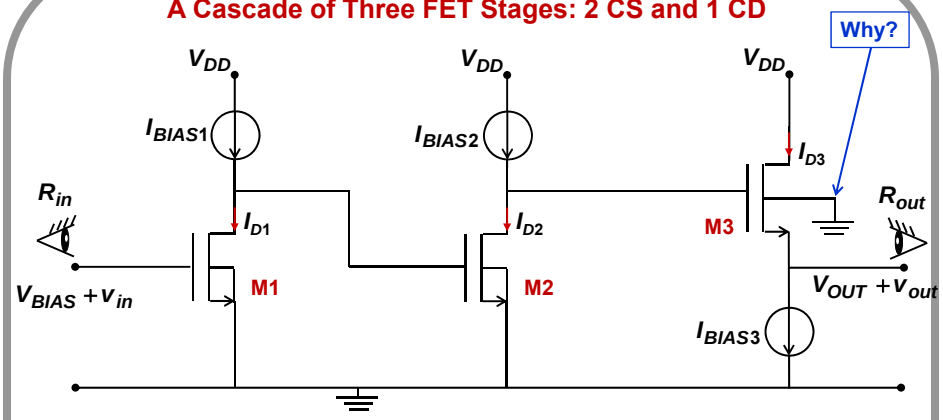
Open circuit voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = A_{v1} A_{v2}$$

$$= [-g_{m1}(r_{o1} \| r_{oc1})][-g_{m2}(r_{o2} \| r_{oc2})]$$

Not really a good voltage amplifier – output resistance is too large – but a decent transconductance amplifier

A Cascade of Three FET Stages: 2 CS and 1 CD



Input resistance:

$$R_{in} = \infty$$

Output resistance:

$$\frac{1}{R_{out}} \approx \frac{1}{r_{oc3}} + (g_{m3} + g_{mb3}) \approx (g_{m3} + g_{mb3})$$

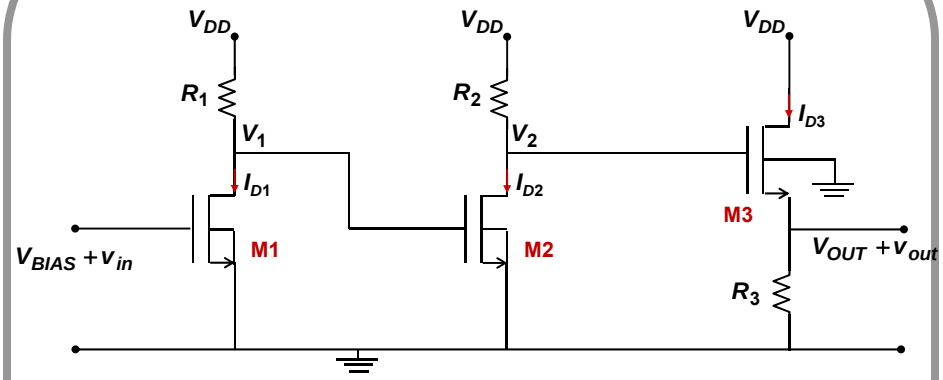
Small

Open circuit voltage gain:

$$A_v = A_{v1}A_{v2}A_{v3}$$
$$\approx [-g_{m1}(r_{o1} \| r_{oc1})][-g_{m2}(r_{o2} \| r_{oc2})][\sim 1]$$

Now it is a better voltage amplifier!

A Cascade of Three FET Stages: Direct Coupling and DC Biasing

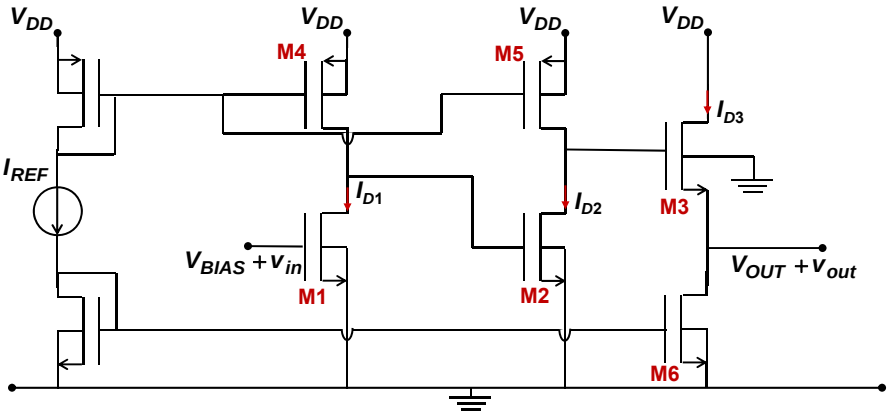


In a direct-coupled scheme, as above, the DC bias of one stage affects the DC bias of other stages

Need to ensure appropriate DC bias of every stage such that:

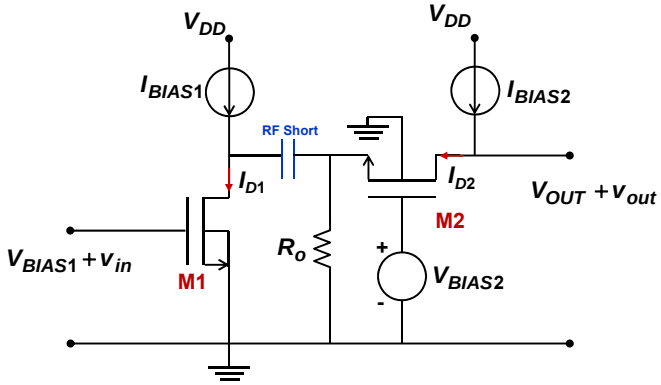
i) The FETs are operating in saturation
ii) The desired voltage swing does not cause problems (e.g. cause some FET to go out of saturation)

A Cascade of Three FET Stages: A Better DC Biasing



The sizes (*W*/*L* ratios) of M4, M5, and M6 can be adjusted to get the desired bias currents for the three amplifier stages

A Cascade of CS and CG: A Capacitively-Coupled Cascode

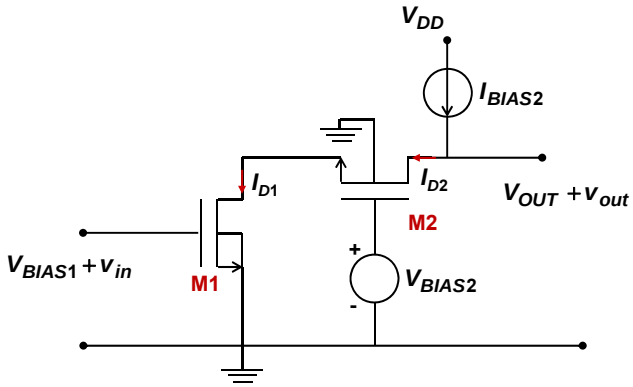


The FET cascode has a large input resistance, a very large output resistance, and a large gain

But it is much better than a CS-CS cascade in terms of the frequency performance, as we will see later in the course

The above topology can be simplified……

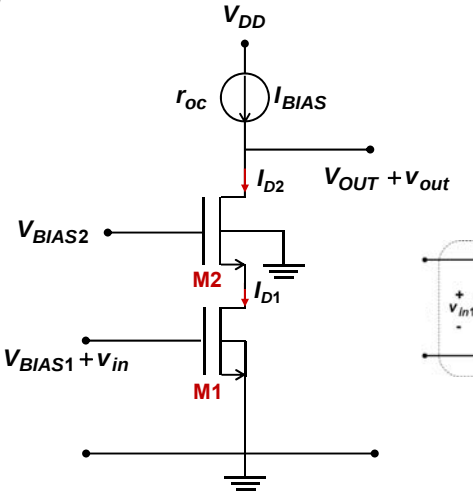
A Cascade of CS and CG: A Direct-Coupled Cascode

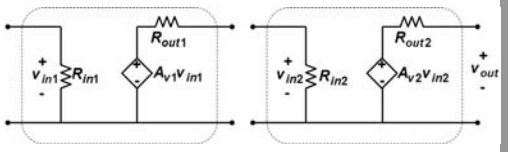


One current source can bias both the stages in a direct-coupling topology….!

This is the preferred way for on-chip designs

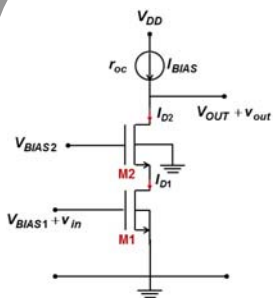
A Cascade of CS and CG: The Cascode

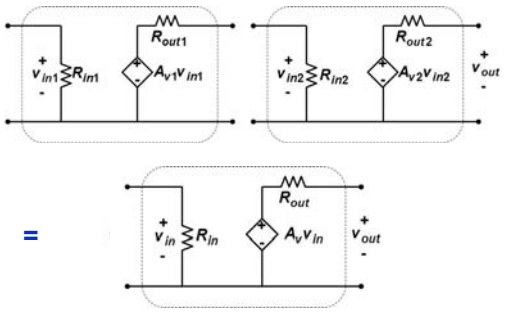




A different way to draw the same circuit

The FET Cascode: Input and Output Resistances of Each Stage





Input resistances:

$$R_{in2} \approx \frac{1}{g_{m2}+g_{mb2}}\left(1+\frac{r_{oc}}{r_{o2}}\right)$$

Assuming $R_L = \infty$

$$R_{in1} = \infty$$

$$\Rightarrow R_{in} = R_{in1} = \infty$$

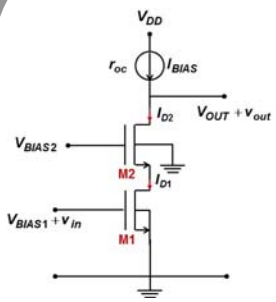
Output resistances:

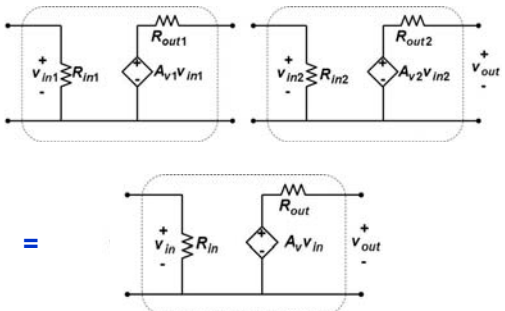
$$R_{out1} = r_{o1}$$

$$R_{out2} = r_{oc} \,||\, [r_{o2} + R_{out1} + r_{o2}(g_{m2}+g_{mb2})R_{out1}]$$
$$\approx r_{oc} \,||\, [(g_{m2}+g_{mb2})r_{o1}r_{o2}]$$

$$\Rightarrow R_{out} = R_{out2} \approx r_{oc} \,||\, [(g_{m2}+g_{mb2})r_{o1}r_{o2}]$$

The FET Cascode: Voltage Gains of Each Stage





Voltage Gains:

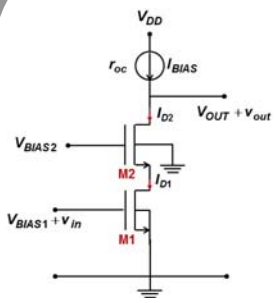
$$A_{v1} = -g_{m1}r_{o1} \qquad A_{v2} = (g_{m2}+g_{mb2})(r_{o2} \,||\, r_{oc})$$

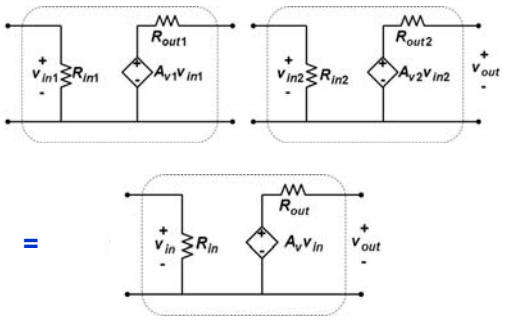
$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1}\frac{R_{in2}}{R_{out1}+R_{in2}} = (-g_{m1}r_{o1})\left((g_{m2}+g_{mb2})\frac{r_{o2}r_{oc}}{r_{o2}+r_{oc}}\right)\frac{1}{(g_{m2}+g_{mb2})r_{o1}\dfrac{r_{o2}}{r_{o2}+r_{oc}}+1}$$

If $r_{oc} >>>> r_{o2}, r_{o1}$:

$$\Rightarrow A_v \approx [-g_{m1}r_{o1}][(g_{m2}+g_{m2b})r_{o2}] \longrightarrow \text{Very large}$$

The FET Cascode: Voltage Gains of Each Stage





Voltage Gains:

$$A_{v1} = -g_{m1}r_{o1} \qquad A_{v2} = (g_{m2} + g_{mb2})(r_{o2} \,||\, r_{oc})$$

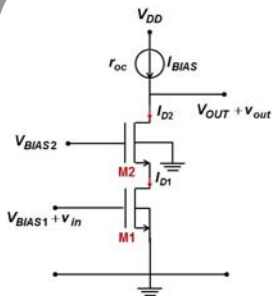
$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1}\frac{R_{in2}}{R_{out1} + R_{in2}} = (-g_{m1}r_{o1})\left((g_{m2} + g_{mb2})\frac{r_{o2}r_{oc}}{r_{o2} + r_{oc}}\right)\frac{1}{(g_{m2} + g_{mb2})r_{o1}\dfrac{r_{o2}}{r_{o2} + r_{oc}} + 1}$$

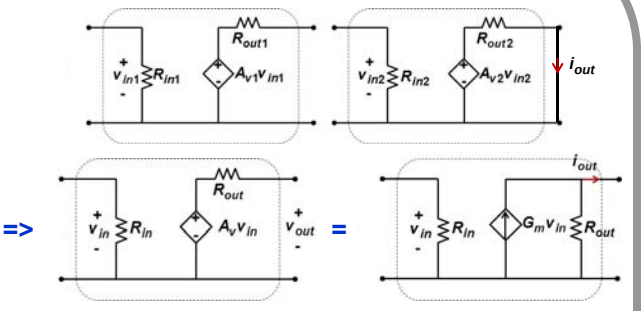
If $r_{oc} \sim r_{o2}$, r_{o1} :

$$\Rightarrow A_v \approx (-g_{m1}r_{o1})\left((g_{m2} + g_{mb2})\frac{r_{o2}r_{oc}}{r_{o2} + r_{oc}}\right)\frac{1}{(g_{m2} + g_{mb2})r_{o1}\dfrac{r_{o2}}{r_{o2} + r_{oc}}}$$

$$\Rightarrow A_v \approx -g_{m1}r_{oc} \longrightarrow \text{Can still be large}$$

The FET Cascode: Transconductance Gain





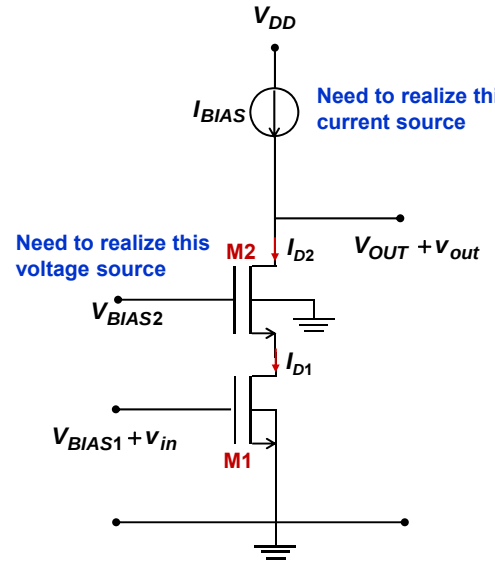
Transconductance Gain (with output shorted):

$$G_m = \frac{i_{out}}{v_{in}} = \frac{A_v}{R_{out}} \approx -g_{m1}$$

Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

$I_{D1} = I_{D2} = I_{BIAS}$



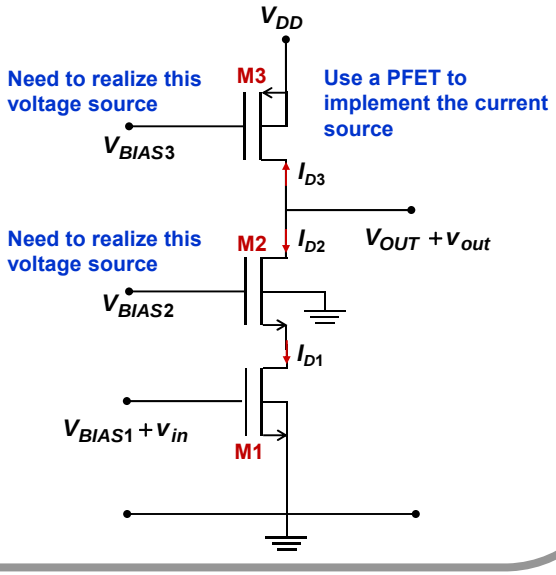
Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

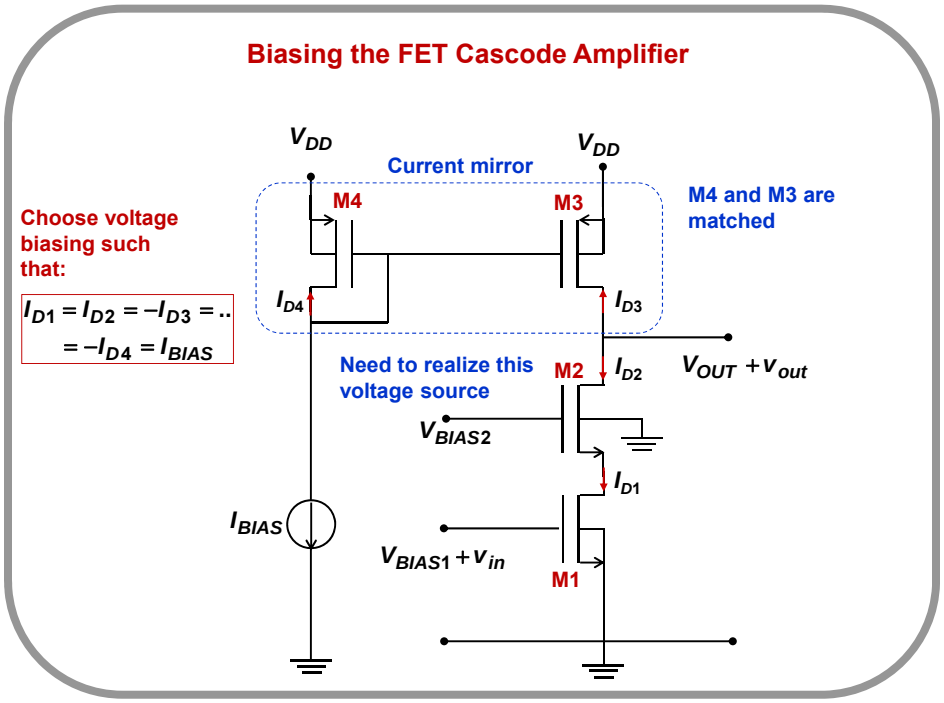
$I_{D1} = I_{D2} = -I_{D3}$

Problem: To be accurate with voltage biasing, one needs to know the characteristics (i.e. k_n, k_p, etc) of the FETs accurately, and this information is usually not available to the circuit designer

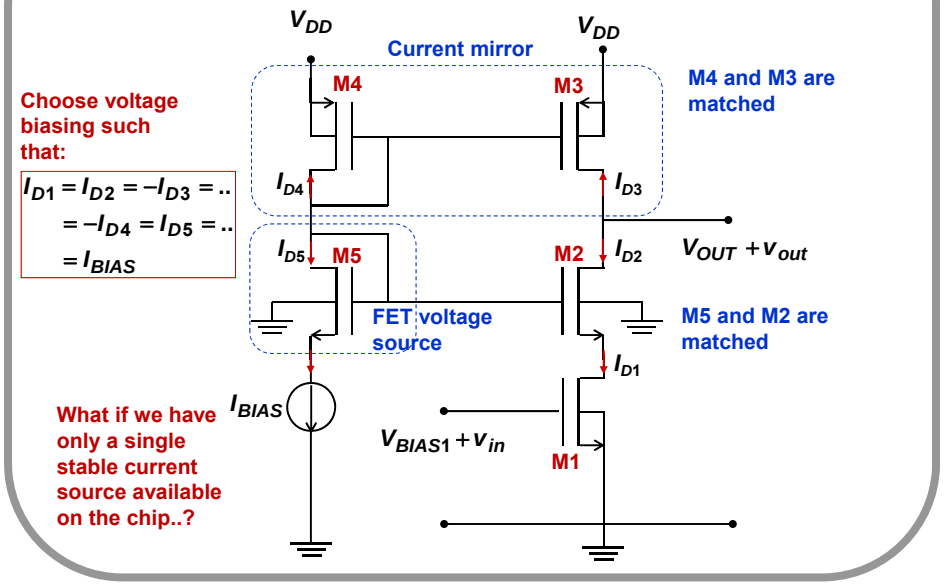
Solution: Use circuit biasing schemes that are not too sensitive to the circuit designer's detailed knowledge of the FETs!



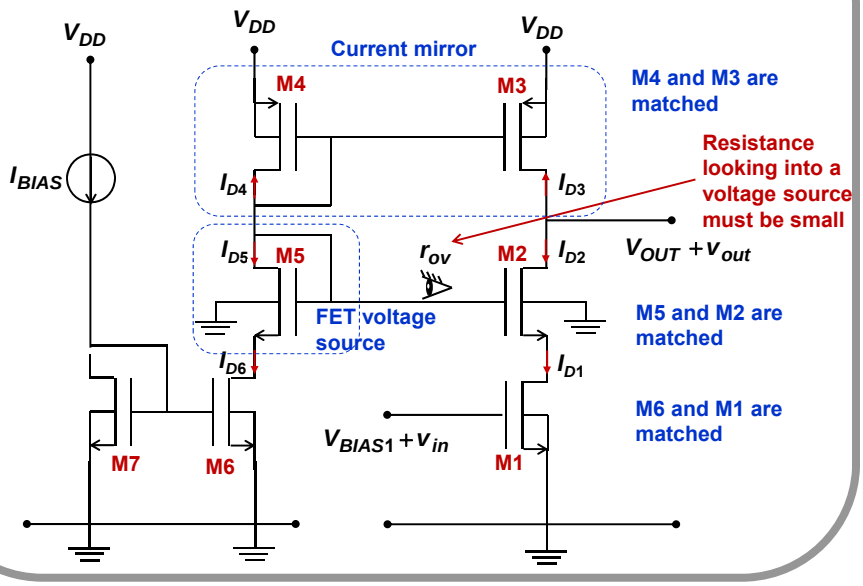
Biasing the FET Cascode Amplifier



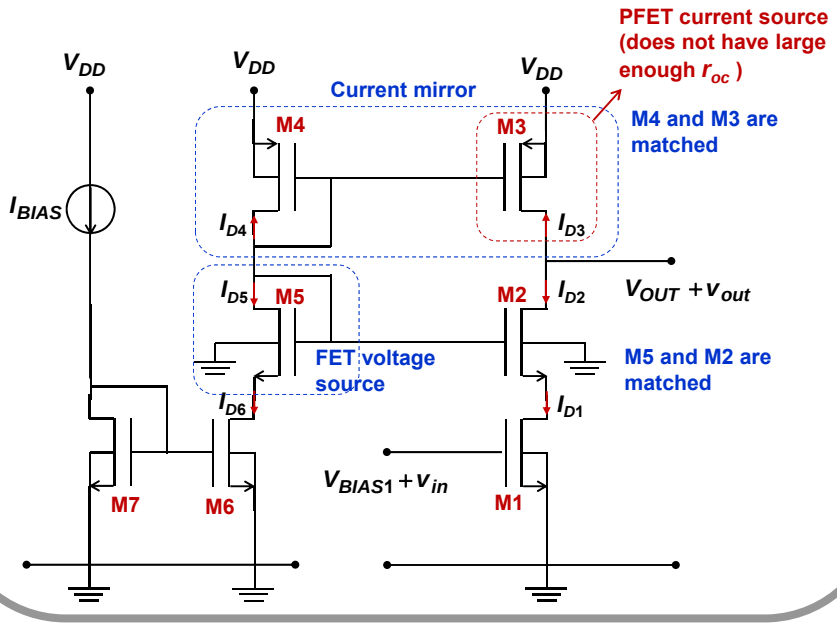
Biasing the FET Cascode Amplifier

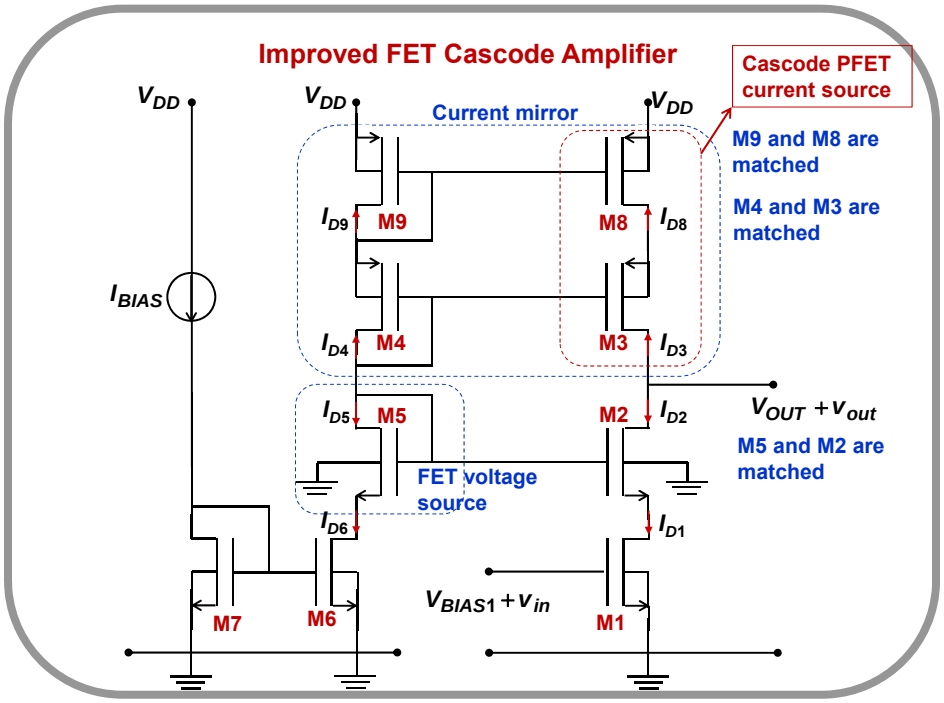


Biasing the FET Cascode Amplifier



Biasing the FET Cascode Amplifier




Improved FET Cascode Amplifier
Cascode PFET current source
M9 and M8 are matched
M4 and M3 are matched
M5 and M2 are matched
Current mirror
FET voltage source
V_{DD}
V_{DD}
V_{DD}
I_{BIAS}
I_{D9}
M9
M8
I_{D8}
I_{D4}
M4
M3
I_{D3}
I_{D5}
M5
M2
I_{D2}
$V_{OUT} + v_{out}$
I_{D6}
I_{D1}
$V_{BIAS1} + v_{in}$
M7
M6
M1