Lecture 14

FET Current and Voltage Sources and Current Mirrors

The Building Blocks of Analog Circuits - IV

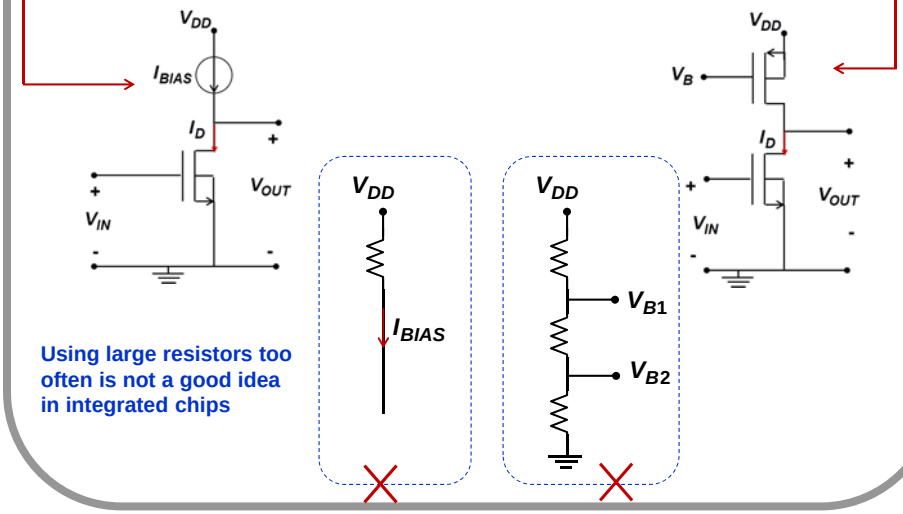
In this lecture you will learn:

- Current and voltage sources using FETs
- FET current mirrors
- Cascode current mirror
- Double Wilson current mirror
- Active biasing schemes

Motivation

Questions:

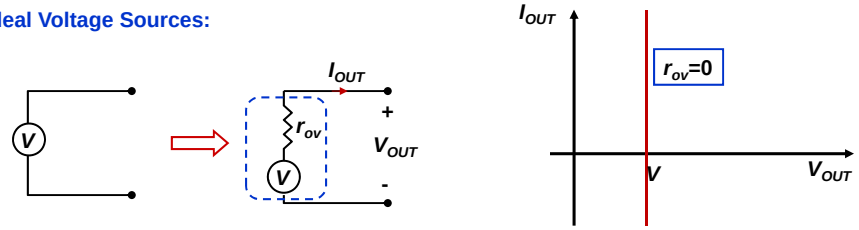
- Are there better ways to realize on-chip current sources to bias circuits?
- Are there good ways to generate on-chip voltage levels to bias circuits?



Using large resistors too often is not a good idea in integrated chips

Characteristics of Ideal Voltage Sources

Ideal Voltage Sources:

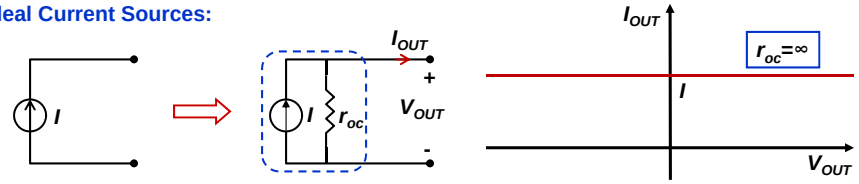


One can draw any current from an ideal voltage source and the voltage at the output terminals will remain constant

The output resistance of an ideal voltage source is zero

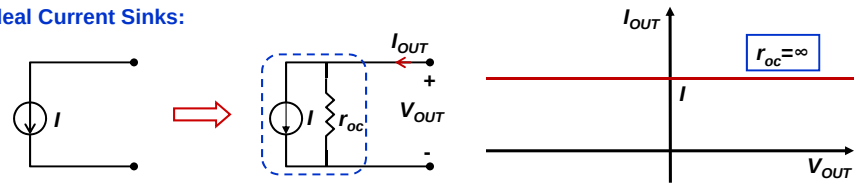
Characteristics of Ideal Current Sources and Sinks

Ideal Current Sources:



One can have any voltage at the at the output terminals of an ideal current source and the current delivered will remain constant
The output resistance of an ideal current source is infinity

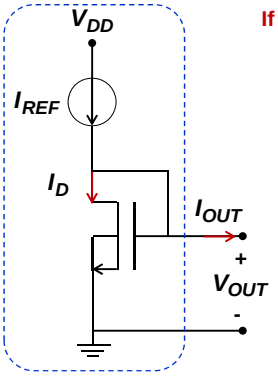
Ideal Current Sinks:



One can have any voltage at the at the output terminals of an ideal current sink and the current sinked will remain constant
The output resistance of an ideal current sink is infinity

A FET Voltage Source: Large Signal Analysis

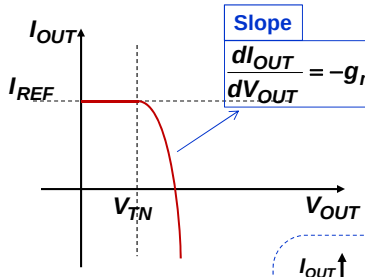
• Assume for the moment that we have a current source I_{REF}



If $V_{OUT} > V_{TN}$:

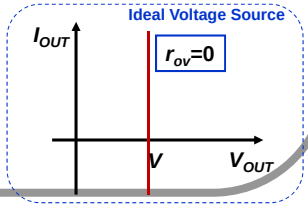
$$I_{REF} = I_D + I_{OUT} = \frac{k_n}{2}(V_{OUT} - V_{TN})^2(1+\lambda_n V_{OUT}) + I_{OUT}$$

$$\Rightarrow \quad V_{OUT} \approx V_{TN} + \sqrt{\frac{2(I_{REF} - I_{OUT})}{k_n}} \qquad \left\{ \text{if } \lambda_n V_{OUT} << 1 \right)$$



Slope

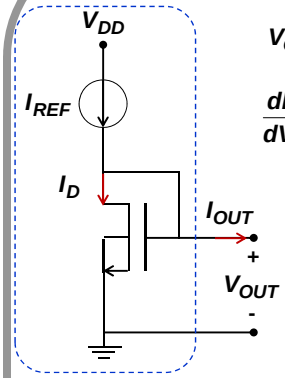
$$\frac{dI_{OUT}}{dV_{OUT}} = -g_m = -k_n(V_{OUT} - V_{TN})$$



• Not exactly the vertical line of an ideal voltage source but good enough for many practical applications

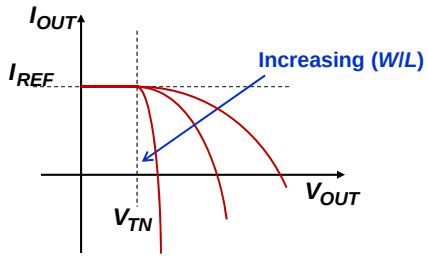
• The line can be made more vertical and the voltage source more ideal by increasing the value of g_m

A FET Voltage Source: Large Signal Analysis



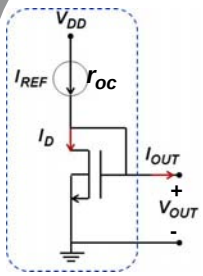
$$V_{OUT} \approx V_{TN} + \sqrt{\frac{2(I_{REF} - I_{OUT})}{(W/L)\mu_n C_{ox}}}$$

$$\frac{dI_{OUT}}{dV_{OUT}} = -g_m = -\frac{W}{L}\mu_n C_{ox}(V_{OUT} - V_{TN})$$

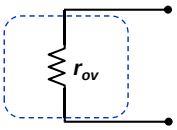


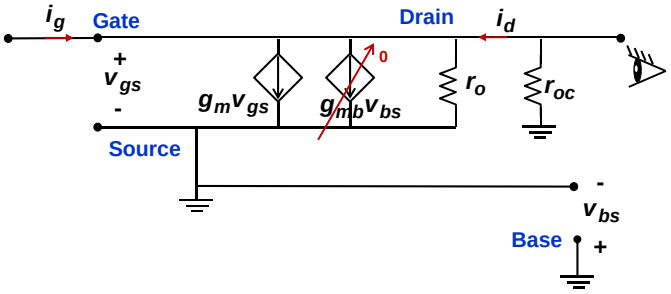
• If the (W/L) ratio of the FET is made very large, the output voltage V_{OUT} is fixed at approximately V_{TN} for all values of the current I_{OUT} drawn from the source (provided $I_{OUT} < I_{REF}$)

A FET Voltage Source: Small Signal Analysis



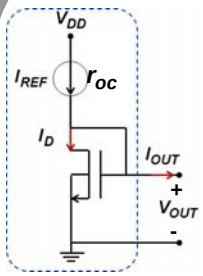
Small signal model

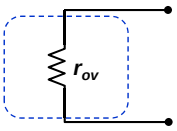


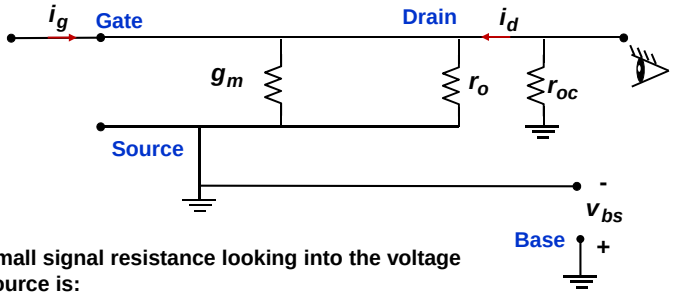


Need to find the resistance r_{ov} looking into from the output terminals

A FET Voltage Source: Small Signal Analysis







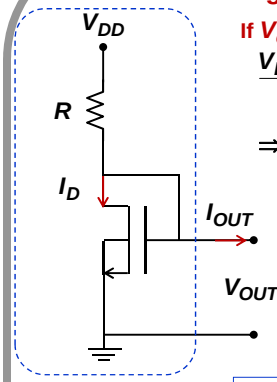
Small signal resistance looking into the voltage source is:

$$r_{ov} = (1/g_m) \,||\, r_o \,||\, r_{oc} \approx \frac{1}{g_m}$$ → Generally small if g_m is large

We have a voltage source that:

- Gives a DC voltage V_{OUT} adjustable by changing the value of I_{REF} , and
- Has an incremental or small signal resistance r_{ov} approximately equal to $1/g_m$ (which can be pretty small)

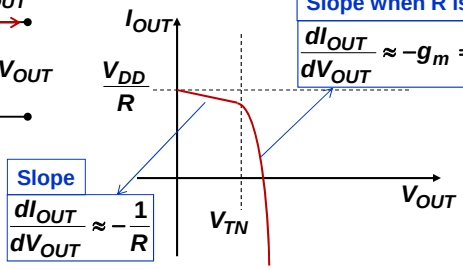
A FET Voltage Source: Simplest Implementation of I_{REF}



If $V_{OUT} > V_{TN}$:

$$\frac{V_{DD} - V_{OUT}}{R} = I_D + I_{OUT} \approx \frac{k_n}{2}(V_{OUT} - V_{TN})^2 + I_{OUT}$$

$$\Rightarrow \quad V_{OUT} = V_{TN} + \sqrt{\frac{1}{k_n^2 R^2} + \frac{2[(V_{DD} - V_{TN})/R - I_{OUT}]}{k_n}} - \frac{1}{k_n R}$$



Slope when R is much larger than $1/g_m$

$$\frac{dI_{OUT}}{dV_{OUT}} \approx -g_m = -k_n(V_{OUT} - V_{TN})$$

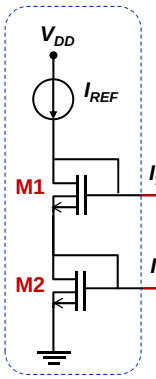
Slope

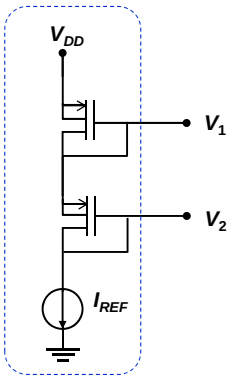
$$\frac{dI_{OUT}}{dV_{OUT}} \approx -\frac{1}{R}$$

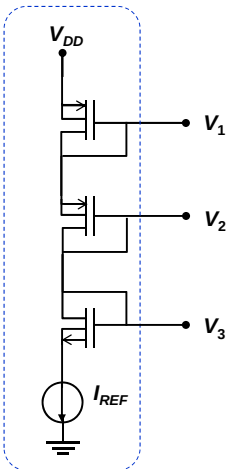
• If the (W/L) ratio of the FET is made very large and R is much larger than $1/g_m$, the output voltage V_{OUT} is fixed at approximately V_{TN} for all values of the current I_{OUT} drawn from the source - provided $I_{OUT} < (V_{DD} - V_{TN})/R$

FET Voltage Sources

One can produce multiple voltage levels from the same structure using NMOS FETs, PMOS FETs, and combination of both NMOS and PMOS FETs





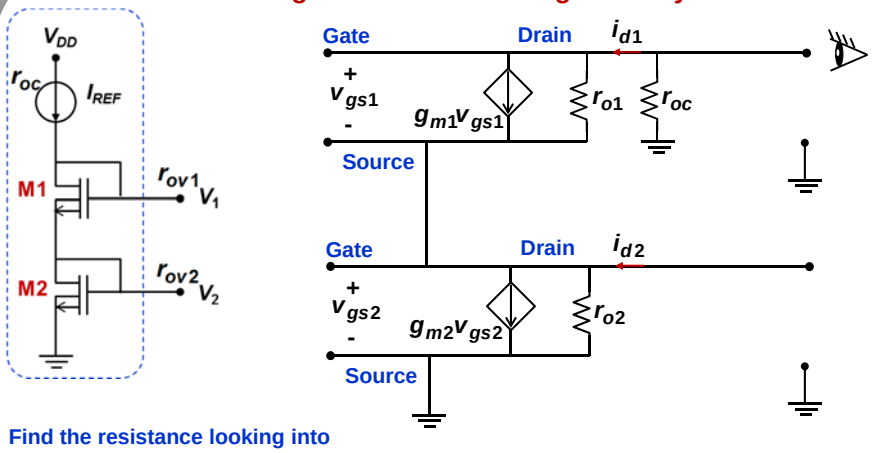


$$V_1 \approx V_2 + V_{TN1} + \sqrt{\frac{2(I_{REF} - I_1)}{k_{n1}}}$$

$$V_2 \approx V_{TN2} + \sqrt{\frac{2(I_{REF} - I_1 - I_2)}{k_{n2}}}$$

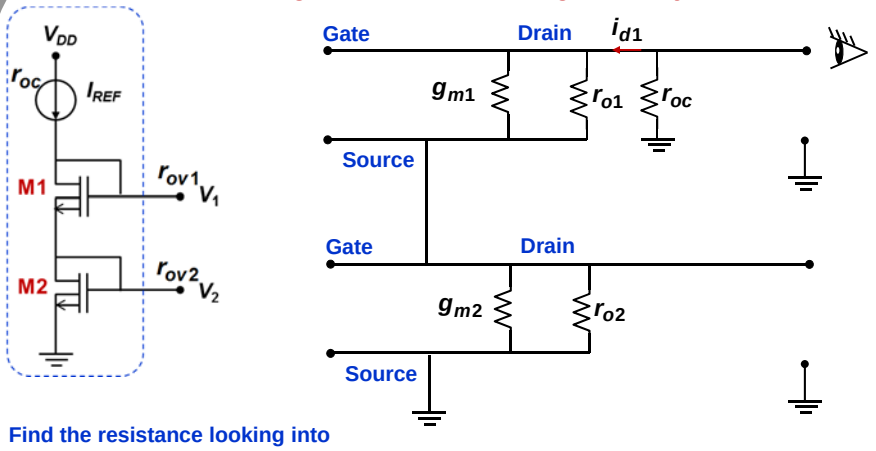
But ……..need to be careful about the small signal resistances associated with each voltage output!

FET Voltage Sources: Small Signal Analysis



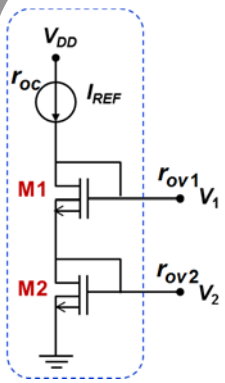
Find the resistance looking into the first voltage source assuming the second one is incrementally open (why?)

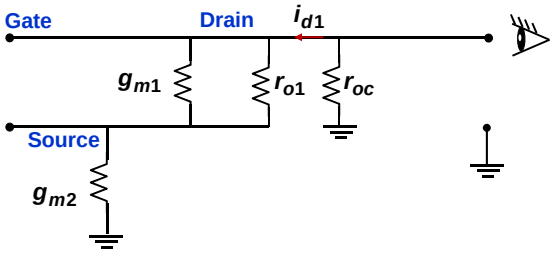
FET Voltage Sources: Small Signal Analysis



Find the resistance looking into the first voltage source assuming the second one is incrementally open (why?)

FET Voltage Sources: Small Signal Analysis

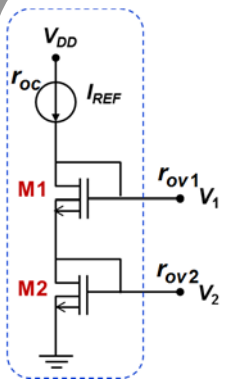


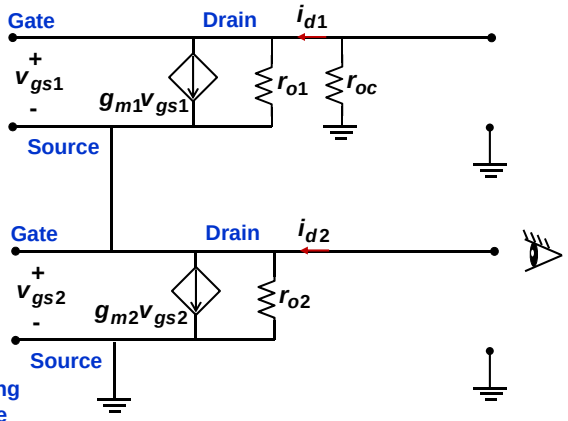


$$r_{ov1} \approx \frac{1}{g_{m1}} + \frac{1}{g_{m2}} \longrightarrow \text{Small}$$

Find the resistance looking into the first voltage source assuming the second one is incrementally open (why?)

FET Voltage Sources: Small Signal Analysis



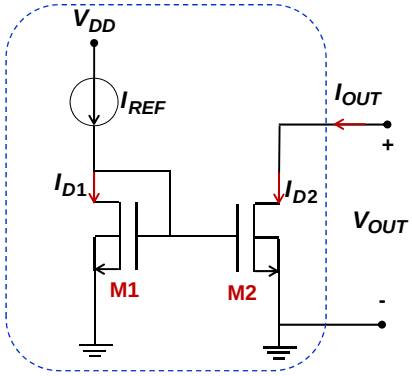


Then find the resistance looking into the second voltage source assuming the first one is incrementally open (why?)

$$r_{ov2} \approx \frac{1}{g_{m2}} \longrightarrow \text{Small}$$

A FET Current Sink: Large Signal Analysis

• Assume that we have a single current source I_{REF} - but we want more……



$$V_{GS2} = V_{GS1}$$

$$\Rightarrow I_{D2} \approx \frac{k_{n2}}{k_{n1}} I_{D1} = \frac{(W/L)_2}{(W/L)_1} I_{D1}$$

$$\Rightarrow I_{OUT} \approx \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

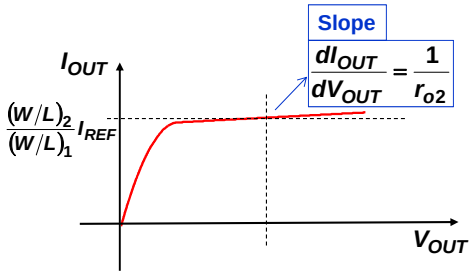
Assuming M2 is in saturation

In saturation:

$$I_D = \frac{k_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda_n V_{DS})$$

Small

$$k_n = \frac{W}{L}\mu_n C_{ox}$$

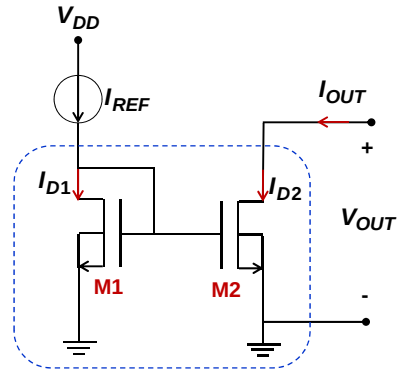


• Not exactly the horizontal line of an ideal current source but good enough for many practical applications

A FET Current Mirror

• A ideal current mirror duplicates the current:

$$I_{OUT} = I_{REF}$$

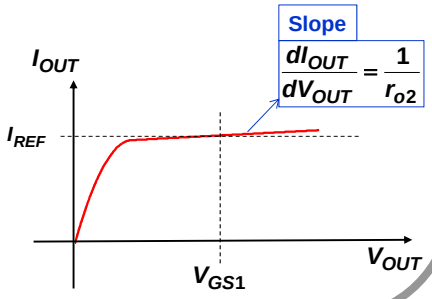


A matched transistor pair

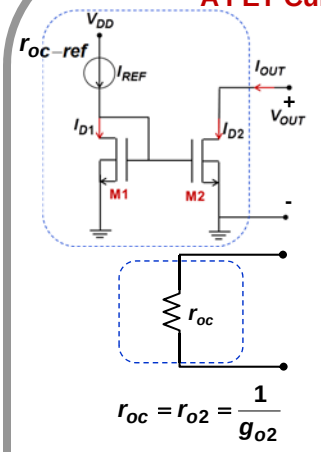
$$V_{GS2} = V_{GS1}$$

$$(W/L)_2 = (W/L)_1 \rightarrow$$ Matched Transistors

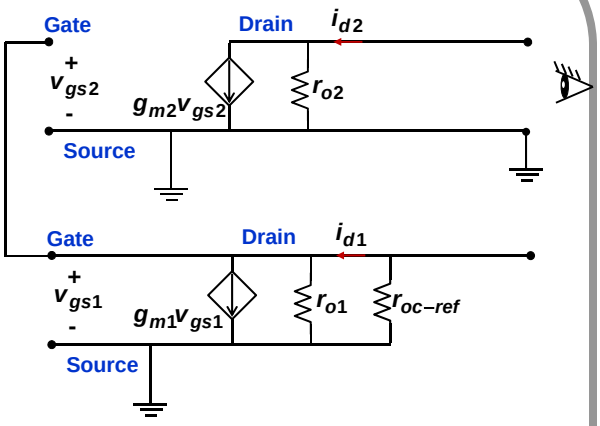
$$\Rightarrow I_{OUT} \approx I_{REF}$$



A FET Current Sink: Small Signal Analysis



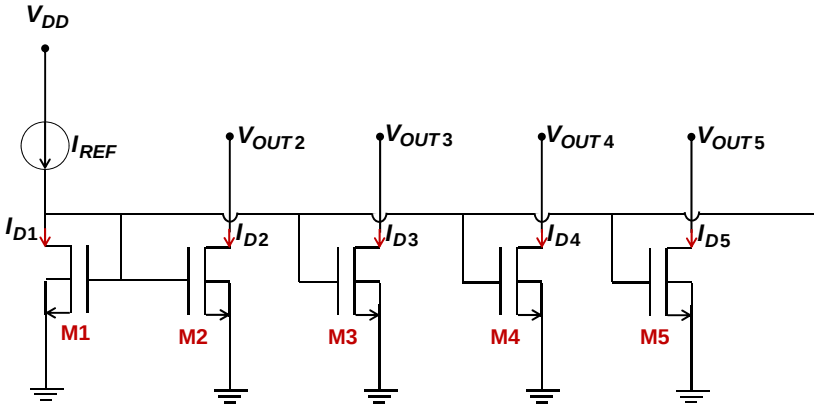
$$r_{oc} = r_{o2} = \frac{1}{g_{o2}}$$



We have a current sink that:

- Provides a DC current I_{OUT} adjustable by changing the value of I_{REF} , and
- Has an incremental or small signal resistance r_{oc} approximately equal to r_{o2} (which can be pretty large)
- The resistance r_{oc} will become small if M2 goes into the linear region

Multiple NFET Current Sinks



One can realize multiple current sinks for biasing applications from the same structure using NMOS devices with different (*W*/*L*) ratios:

$$I_{Dk} \approx \frac{(W/L)_k}{(W/L)_1} I_{REF}$$

Note that V_{OUTk} needs to be always large enough such that Mk remains in saturation

A PFET Current Source and Current Mirror

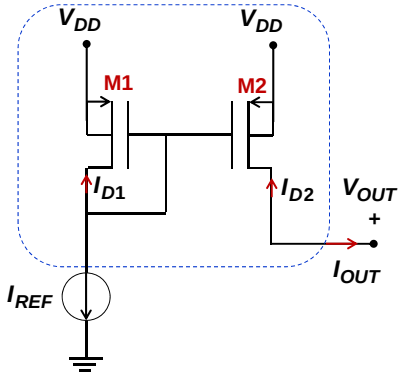
• A current mirror duplicates the current:

$$I_{OUT} = I_{REF}$$

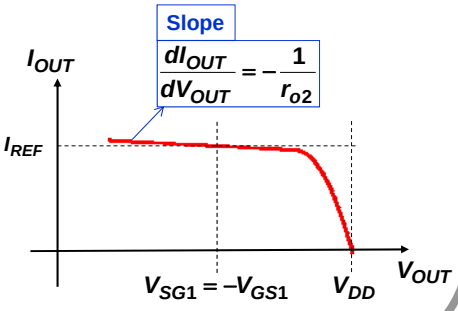
$$V_{GS2} = V_{GS1}$$

$$(W/L)_2 = (W/L)_1 \rightarrow \text{Matched Transistors}$$

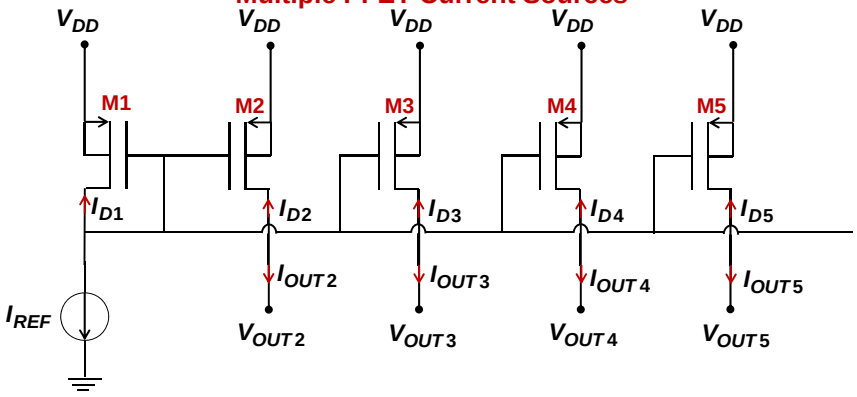
$$\Rightarrow I_{OUT} \approx I_{REF}$$



A matched transistor pair



Multiple PFET Current Sources

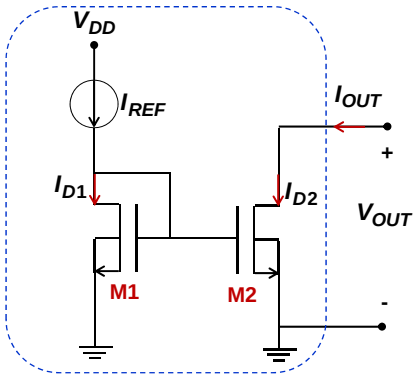


One can realize multiple current sources for biasing applications from the same structure using PMOS devices with different (*W*/*L*) ratios:

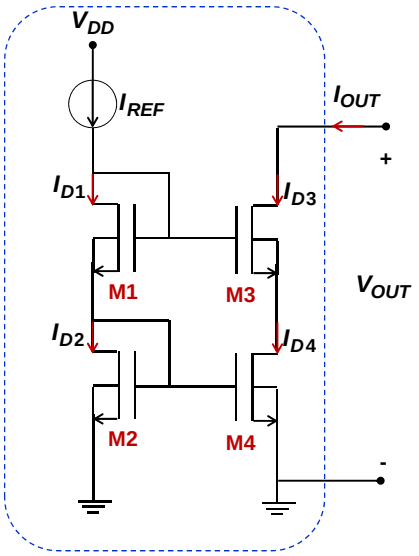
$$I_{OUTk} \approx \frac{(W/L)_k}{(W/L)_1} I_{REF}$$

Note that V_{OUTk} needs to be always small enough such that Mk remains in saturation

A Current Sink with Large Output Resistance: The Cascode Design



$$r_{oc} = r_{o2} = \frac{1}{g_{o2}}$$

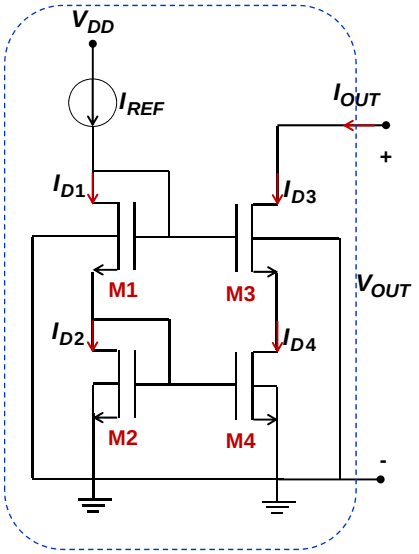


$$r_{oc} = r_{o3} + r_{o4}\left(1 + g_{m3}r_{o3}\right) \approx g_{m3}r_{o3}r_{o4}$$

A Current Sink with Large Output Resistance: The Cascode Design

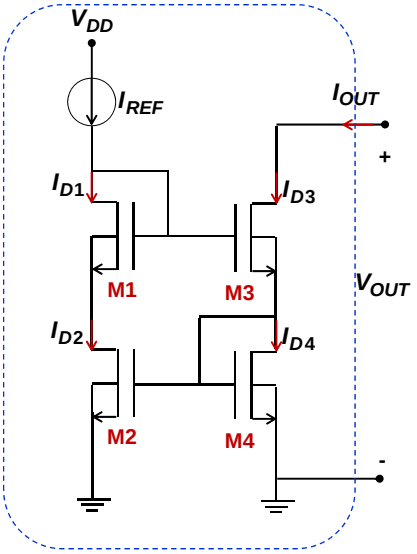
Usually the substrate contact of all NFETs in the stack are tied to the ground in CMOS technologies in which all NFETs share the same substrate

Need to account for the body effect (due to non-zero V_{SB}) in M3

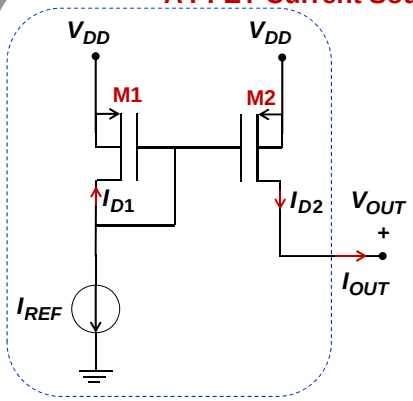


The Double Wilson Current Mirror

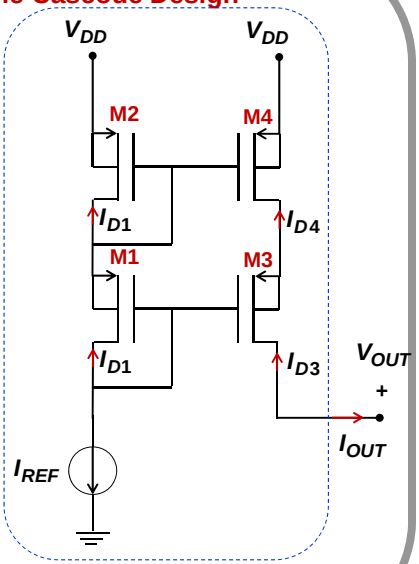
More immune to systemic errors in the fabrication process than the cascode design



A PFET Current Source: The Cascode Design



$$r_{oc} = r_{o2} = \frac{1}{g_{o2}}$$



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A PFET Current Source: The Cascode Design

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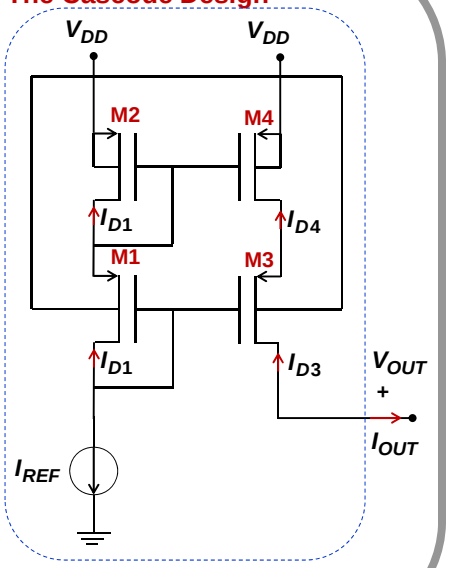
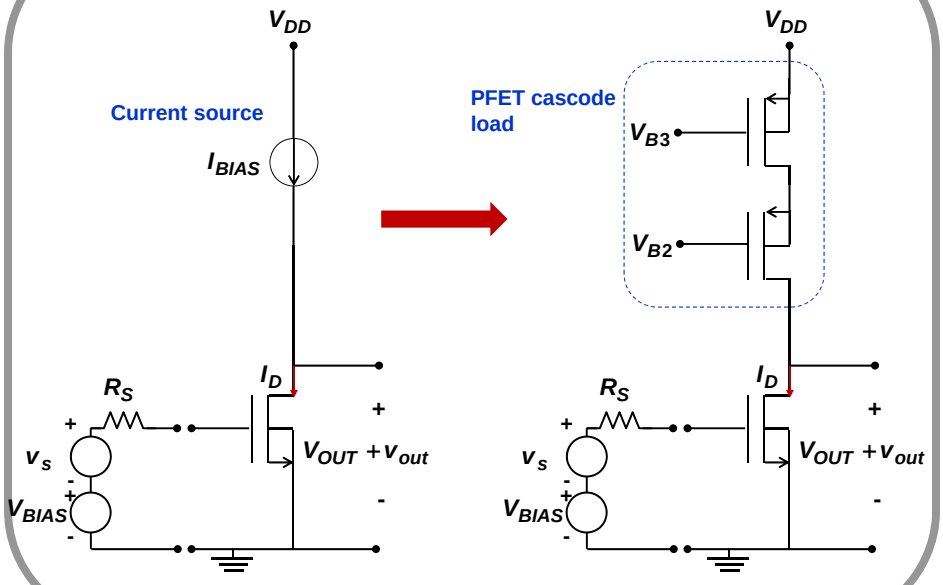
Need to account for the body effect (due to non-zero V_{SB}) in M3



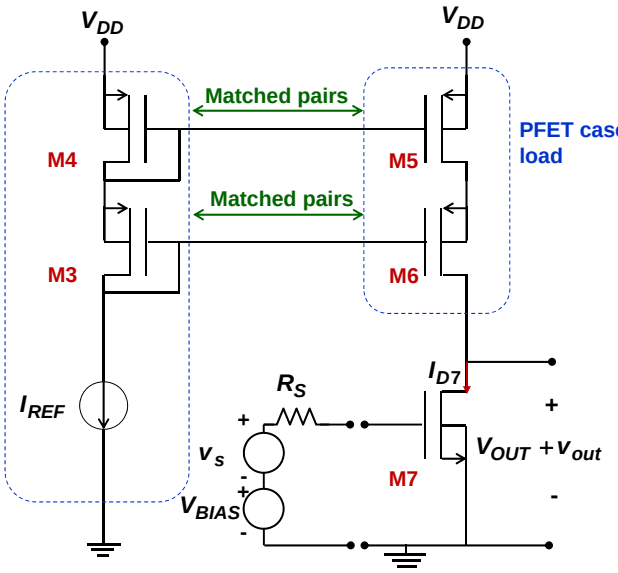
Biasing the PFET Loaded NFET CS Amplifier



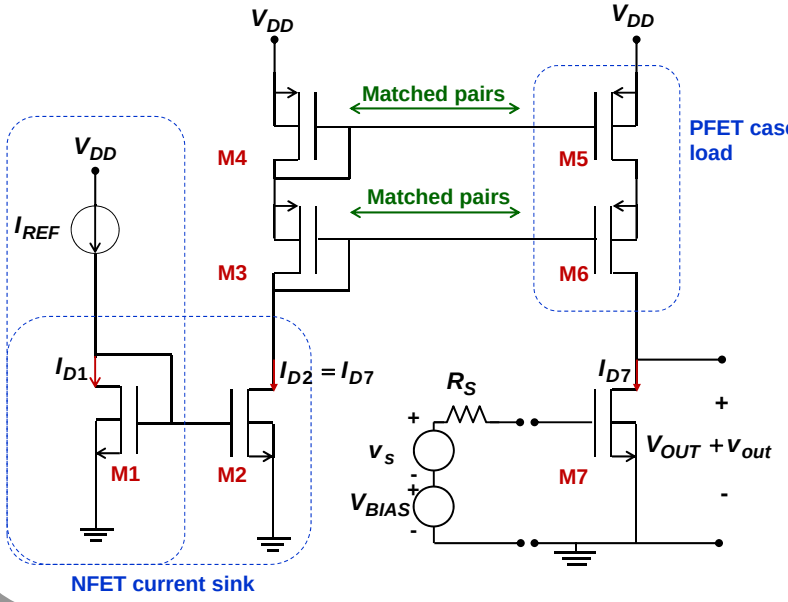
Biasing the PFET Loaded NFET CS Amplifier

Voltage biasing network

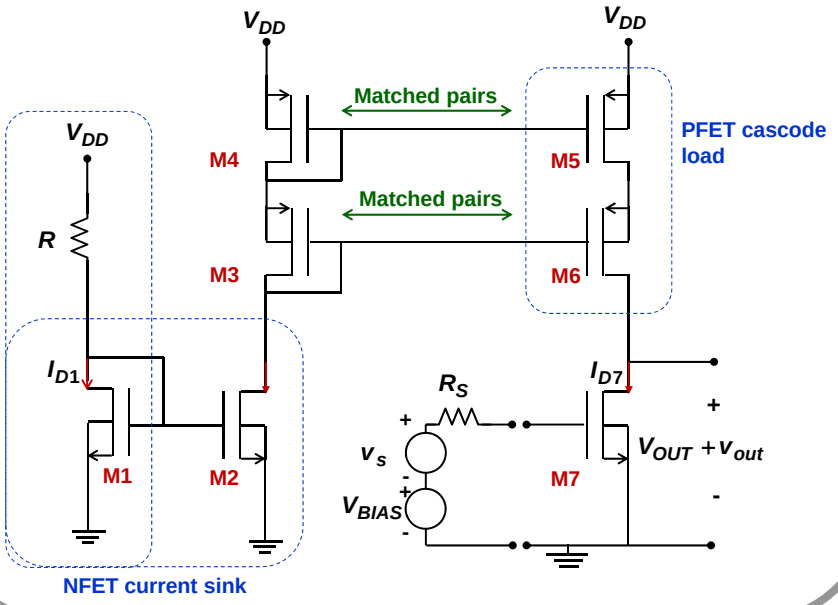
If M4 and M5 are identical and M3 and M6 are identical (matched pairs) then I_{D7} will equal I_{REF} and the gate voltages needed for M5 and M6 will be automatically generated on the chip without exact knowledge of the k_p and V_{TP} of the PFETs



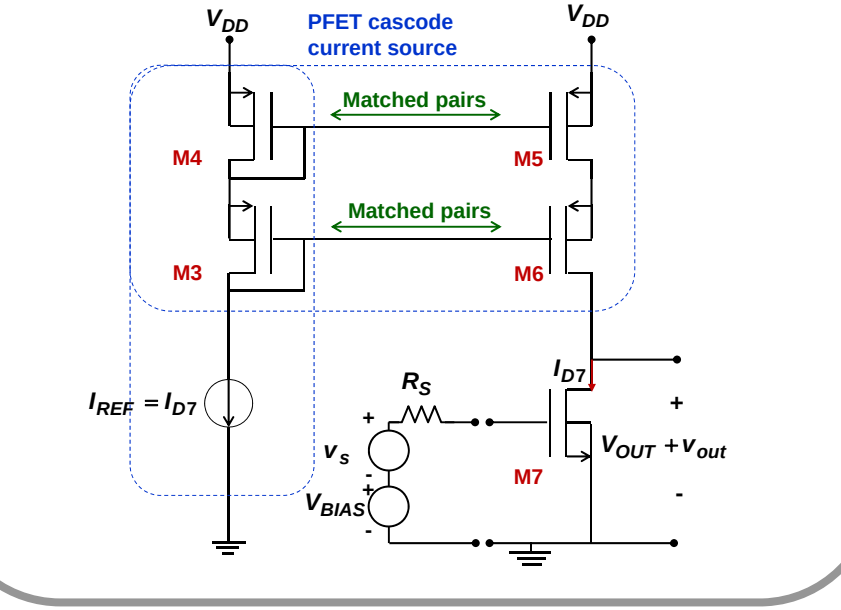
Biasing the PFET Loaded NFET CS Amplifier



Biasing the PFET Loaded NFET CS Amplifier



Biasing the PFET Loaded NFET CS Amplifier



Biasing the PFET Loaded NFET CS Amplifier

So we implemented a current source load using the PFETs in a cascode configuration