Department of Electrical and Computer Engineering, Cornell University

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ECE 3150: Microelectronics

Spring 2016

Final Exam ` **May 18, 2016**

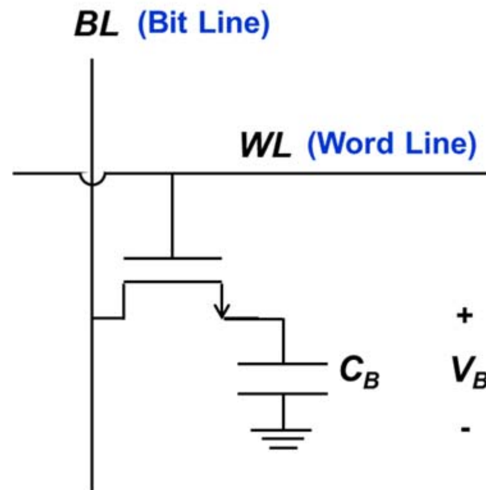
INSTRUCTIONS:

- **Every problem must be done in the separate booklet**
- **Only work done on the exam booklets will be graded – do not attach your own sheets to the exam booklets under any circumstances**
- **To get partial credit you must show all the relevant work**
- **Correct answers with wrong reasoning will not get points**
- **All questions do not carry equal points**
- **All questions do not have the same level of difficulty**
- **TOTAL POINTS: 100**
- **Unless specified otherwise, assume room temperature**

DO NOT WRITE IN THIS SPACE

Problem 1 (DRAM Dynamics) – 20 points

Consider the following DRAM cell:



The NFET characteristics and the digital logic characteristics are as follows:

$k_n = 400\ \mu A/V^2 \quad V_H = 3\ V \quad V_L = 0\ V \quad V_{TN} = 0.5\ V \quad \lambda_n = 0 \quad C_B = 70\ fF$

$m = \text{subthreshold slope factor} = 2$

During the memory write operation, the word line WL is connected to V_H and the bit line BL is either at V_H or at V_L depending on whether a logical "1" or "0", respectively, needs to be written to the memory cell capacitor C_B.

a) Assume that the memory capacitor C_B is initially full discharged ($V_B(t=0) = V_L$). A logical "1" is to be written to the memory cell. So at time $t = 0$ the word line WL is connected to V_H and the bit line BL is also at V_H. What is the final voltage $V_B(t=\infty)$ across the memory cell capacitor at time $t = \infty$. Need an answer in Volts. This final voltage value is the highest voltage V_{BH} that can be stored on the capacitor. (5 points)

b) Assuming the same scenario as in part (a), set up differential equation(s) for the time dependent voltage $V_B(t)$ across the memory cell capacitor. Pay particular attention to the regimes of operation of the NFET. The solution of the differential equation(s) should give $V_B(t)$ changing from V_L to V_{BH}. (5 points)

c) Solve the differential equation in part (b) and drive an expression for the time $t_{0\to1}$ it takes to write the memory cell by finding the time it takes to charge the capacitor from $V_B(t=0) = V_L$ to 90% of its final value V_{BH} at time $t \to \infty$ (i.e. to $0.9\ V_{BH}$). (5 points)

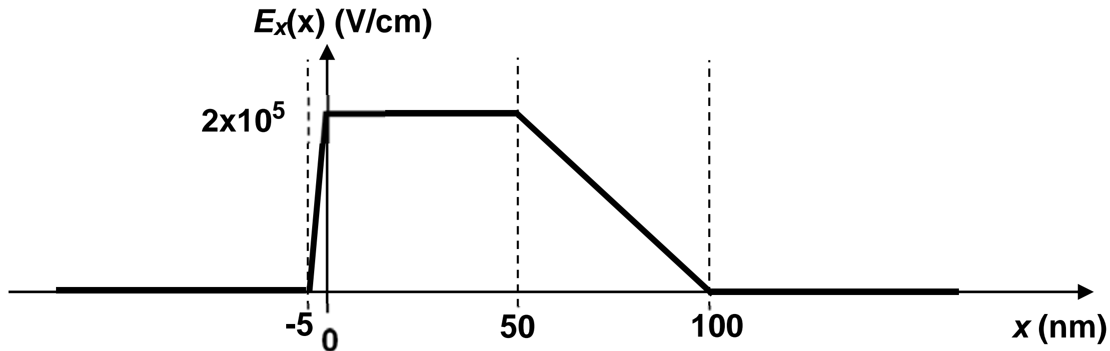
d) Suppose a logical "1" has been written to the memory cell capacitor and the capacitor is charged to the voltage value V_{BH} found in part (a). After the capacitor has been charged, the word line WL is connected to V_L and the bit line BL is also at V_L. Under ideal circumstances the charge should remain on the memory cell capacitor forever. But due to subthreshold current, the charge on the capacitor leaks through the NFET and over time the capacitor discharges and the voltage V_B decreases. Find the time t_L (in

seconds) it takes for the voltage on the capacitor to decrease from the fully charged value of V_{BH} by 1 Volt. A numerical value for t_L is needed. (5 points)

(To preserve the integrity of the stored data bit, the DRAM cell would need to be "refreshed" periodically on time periods shorter than t_L.)

Problem 2 (Basic Device Physics) – 30 points

Parts (a)-(d): Consider a silicon PN junction that was fabricated in the lab. The fabrication did not quite go as planned (as is always the case in the lab). After fabrication, the electric field profile in the PN junction was experimentally measured at a 0.8 Volts applied reverse bias. The curve obtained from this measurement is shown below.



a) What is the built-in potential ϕ_B of this PN junction? Need a numerical value. (3 points)

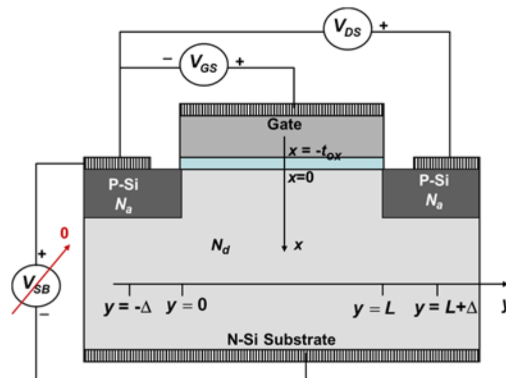
b) What is the small signal capacitance (per unit area) of this junction at the 0.8 Volts applied reverse bias? Need a numerical value. (3 points)

c) What can you say about the doping in the region $0\,\text{nm} < x < 50\,\text{nm}$? Can you indicate the doping type (i.e. N-type or P-type) and magnitude? (3 points)

d) What can you say about the doping in the region $-5\,\text{nm} < x < 0\,\text{nm}$? Can you indicate the doping type and magnitude? (4 points)

Parts (e)-(h): Consider the following PFET at room temperature. The substrate doping is $N_d = 10^{17}$ cm^{-3}. The source and drain regions are doped $N_a = 10^{18}$ cm^{-3}. The device width and length are W and L, respectively.

$N_d = 10^{17}$ cm^{-3}
$N_a = 10^{18}$ cm^{-3}
$V_{SB} = 0$



e) Assuming $V_{DS} = 0$, what is the exact hole concentration (in #/cm^3) under the gate at $(x = 0, y = L/2)$ (i.e. at the silicon oxide interface) at flatband? (3 points)

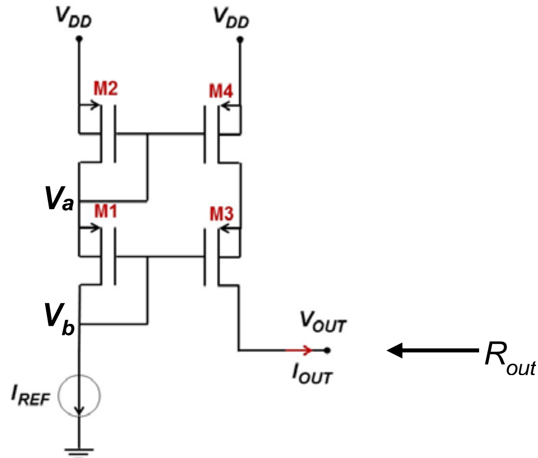
f) Assuming $V_{DS} = 0$ and flatband condition, sketch and label the electrostatic potential at $x = 0$ (i.e. at the silicon oxide interface) as a function of the horizontal coordinate y in the range $-\Delta < y < L + \Delta$ (the range is indicated in the Figure). (4 points)

g) Assuming $V_{DS} = 0$, what is the exact electron concentration (in #/cm^3) under the gate at $(x = 0, y = L/2)$ (i.e. at the silicon oxide interface) at threshold? (4 points)

h) For FETs operating in saturation, $C_{gd} \approx 0$ because the inversion layer charge is not affected by the drain voltage (the small non-zero values of C_{gd} in actual FETs in saturation are contributed by parasitic capacitances and we assume these parasitic capacitances to be zero in this problem). In the linear region, $C_{gd} \neq 0$ and C_{gd} depends on the value of V_{DS}. Suppose $V_{GS} << V_{TP}$ and $V_{DS} = 0$. The total inversion layer charge under the gate is Q_P (units: Coulombs). Now suppose the drain voltage is decreased from 0 to a small negative value ΔV_{DS}. The total inversion layer charge would decrease and become $Q_P - \Delta Q_P$. The ratio $-\Delta Q_P / \Delta V_{DS}$ is the capacitance C_{gd} in the limit $V_{DS} \rightarrow 0$. Find this value of C_{gd} in terms of the physical parameters of the structure. (6 points)

Problem 3 (A PFET Source) – 20 points

Consider the following PFET current source.



Assume that the current source I_{REF} is an ideal current source with infinite output resistance. Assume low frequency operation in this problem (i.e. ignore capacitances). Assume that all PFETs are identical and that:

$k_p = 800\ \mu A/V^2 \quad V_{DD} = 6\ V \quad I_{REF} = 100\ \mu A \quad V_{TP} = -0.5\ V \quad \lambda_p = .01\ V^{-1}$

a) What are the values of the voltages V_a and V_b? Need numerical values. (3 points)

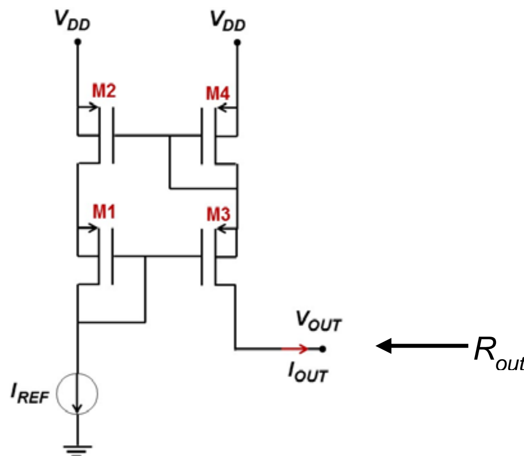
b) At what value of V_{OUT} will the PFET M3 come out of saturation? You may assume that λ_p is zero for this part. Need a numerical value. (4 points)

c) At what value of V_{OUT} will the PFET M4 come out of saturation? You may assume that λ_p is zero for this part. Need a numerical value. (3 points)

d) Plot (and label) the output current I_{OUT} vs the voltage V_{OUT} in the range $0 \le V_{OUT} \le V_{DD}$. You may assume that λ_p is zero for this part. (3 points)

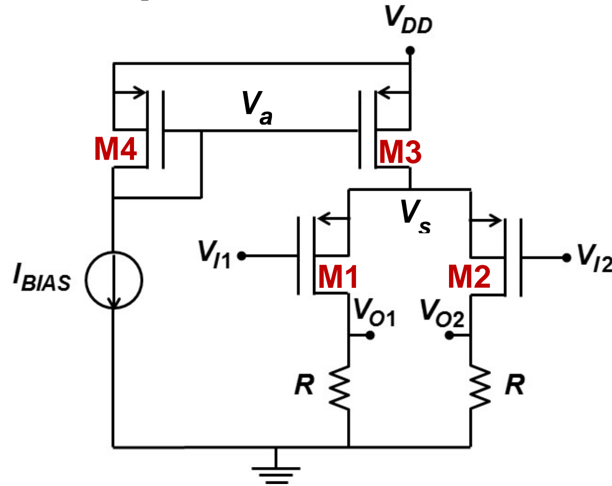
e) Find an expression for the output resistance R_{out} looking in from the output terminal. A numerical value is not required. (4 points)

f) Now assume that the PFETs are connected as shown below (A Double-Wilson PFET source). Find an expression for the output resistance R_{out} looking in from the output terminal. A numerical value is not required. (3 points)



Problem 4 (A Differential Amplifier) – 30 points

Consider the following differential amplifier:



FETs M1 and M2 are identical. FETs M3 and M4 are also identical and are twice as wide as the FETs M1 and M2. Assume low frequency operation in this problem (i.e. ignore capacitances). Assume:

$k_{p1} = k_{p2} = 800\ \mu A/V^2 \qquad k_{p3} = k_{p4} = 1600\ \mu A/V^2 \qquad R = 20\ k\Omega$

$V_{DD} = 5\ V \quad I_{BIAS} = 200\ \mu A \quad V_{TP} = -0.5\ V \quad \lambda_p = .01\ V^{-1}$

a) Assuming every FET is operating in saturation, what is the value of the voltage V_a? A numerical value is needed. (5 points)

b) Assuming a pure common-mode large signal input, $V_{I1} = V_{I2} = V_{Ic}$, what is the maximum value V_{Ic} can have before some FET goes out of the saturation region? A numerical value is needed. (5 points)

c) Assuming a pure common-mode large signal input, $V_{I1} = V_{I2} = V_{Ic}$, what is the minimum value V_{Ic} can have before some FET goes out of the saturation region? A numerical value is needed. (5 points)

d) Assuming $V_{I1} = V_{Ic} + v_{id}/2$ and $V_{I1} = V_{Ic} - v_{id}/2$ and that all FETs are operating in the saturation region, find an expression for the small signal difference-mode gain. Assume:
$V_{O1} = V_{Oc} + v_{od}/2$ and $V_{O2} = V_{Oc} - v_{od}/2$ and $A_{vd} = v_{od}/v_{id}$
(5 points)

e) Again assume that $V_{I1} = V_{Ic} + v_{id}/2$ and $V_{I1} = V_{Ic} - v_{id}/2$ and that all FETs are operating in the saturation region, if the two output nodes shown, are shorted using a wire, find the magnitude and sign of the small signal current that will flow in that wire as a function of the small signal input voltage v_{id}.
(5 points)

For the next part, use the high frequency model for ALL the FETs:

f) Assuming $V_{I1} = V_{Ic} + \mathrm{Re}\{v_{id}(\omega)e^{j\omega t}\}/2$ and $V_{I1} = V_{Ic} - \mathrm{Re}\{v_{id}(\omega)e^{j\omega t}\}/2$ and that all FETs are operating in the saturation region, find an exact expression for the frequency ω_H at which the open circuit gain $A_{vd} = v_{od}(\omega)/v_{id}(\omega)$ (in dB units) drops by ~3 dB from its DC value. (5 points)